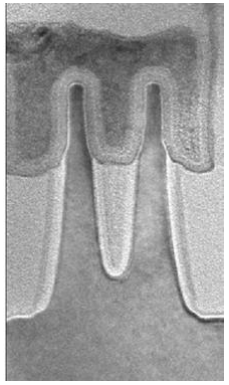
EE-429
Fundamentals of VLSI Design

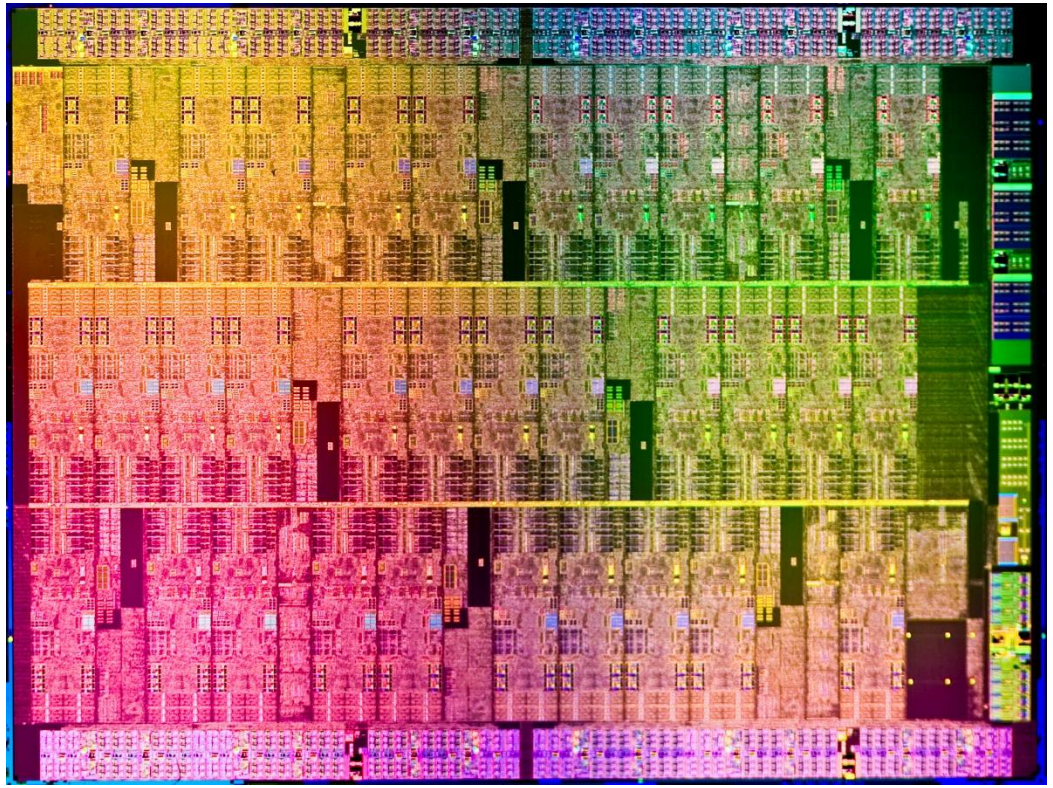
Organization and Outline of the Course

Andreas Burg, Alexandre Levisse

From <10nm Transistors to a Billion Gates



Two trainsistors in
Intel **14nm FinFET** process



INTEL Xeon Phi
8 billion transistors
in 14nm FinFET process

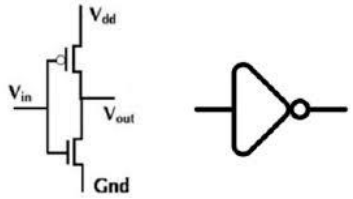
Content and Focus of this Course

Contrary to the Digital Systems Design Course, **we focus on**

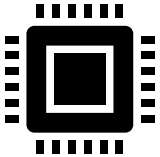
- **Custom** Digital **Integrated Circuits**
  - **Focus on the circuit level** rather than only the architecture level
  - **Consider the electrical characteristics** rather than the functionality and the logic
  - **Account for the physical aspects** of a design (e.g., layout, parasitics, variations, ...)
  - **Understand how to optimize** timing, power, and area **on the gate-level and transistor level**
- and on **Very Large Scale Integration (VLSI)**
  - **Understand how to build a** complex **design from basic building blocks (design flow)**
  - **Prepare the basic building blocks** to be used by the design tools
  - Handle all aspects of a design that are not described by RTL code
  - Perform the physical design
  - Understand and **master and control the design tools** that automate the transition between abstraction levels
  - Understand the chip-level design and integration issues and choices

Specific Topics in Two Parts

- **Introduction to VLSI design**
- **Full custom digital design:** from transistors to digital gates
  - Design of basic gates and memories on transistor level
  - Analyzing and optimizing digital circuits on transistor level
  - Basic models to understand and account for parasitics
  - Technology scaling and impact of variations

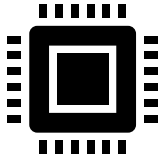


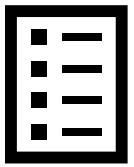
- **Scaling up the complexity:** from gates to a million transistors
  - Economics of VLSI design
  - Compiling complex circuits from basic building blocks
  - The semicustom design flow (front-end and back-end)
  - Circuit and physical design considerations for complex chips



Organization of the Class

- **The class comprises**
  - Theory **lectures** on
    - Principles and methodology of IC design
    - Background on technology and design
  - **Labs with professional ASIC design tools**
    - Guided lab sessions to get familiar with the tools
    - Apply theoretical concepts in real-world settings
  - **Two projects,** in 1st and 2nd half of the semester (graded)
    - Hands on design experience based on lecture and labs
    - Experience the design process
  - **Online questions/exercises** to check your knowledge (graded)
    - Practice what you have learned and check your knowledge
    - Weekly questions on Moodle





Weekly Moodle Quizzes

- **There will be 10 quizzes throughout the semester.**
  - Theory, lab related questions, exercises
- **An excellent opportunity to prepare for the final exam.**
  - Students who did carefully the quizzes (without copying for others) passed the final exam.
- **You have until end of following week (9-10 days) to complete them.**
- **Most of the quizzes will give you only your grade, no intermediate result.**
  - You can retry as many times as you want ! Only your best attempt counts.

- **Use the class forum for your questions.**
- **Don’t hesitate to give a feedback on them.**

Schedule

- 6 ECTS credit course: 6h in class (+ up to 6h homework)

- **Lectures/Labs/Q&A**:
  - Lectures: Thu: CE1 103 / Fri: ELD 020
  - Lab sessions: CO260 & CO6
  - Q&A sessions: during lectures and labs and **on MOODLE**

- **Schedule**: **Thursdays 15:15-18:00**
  Fridays 11:15-14:00
  (ok to bring your lunch)

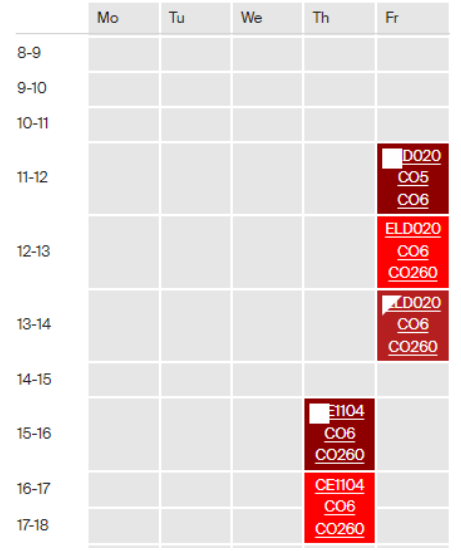
  - **CHECK SCHEDULE** (Lecture/Lab) REGULARLY **ON MOODLE**
  - **ATTEND ALL** LECTURE AND LAB **SESSIONS** as scheduled
  - Don't forget to **complete the Quiz every week (graded)**

Electrical and Electronics Engineering
2024-2025 Master semester 1

- **Semester:** Fall
- **Exam form:** Written (winter session)
- **Subject examined:** Fundamentals of VLSI design
- **Lecture:** 3 Hour(s) per week x 14 weeks
- **Exercises:** 1 Hour(s) per week x 14 weeks
- **Project:** 2 Hour(s) per week x 14 weeks
- **Type:** optional

Electrical and Electronics Engineering
2024-2025 Master semester 3

Micro- and Nanotechnologies for Integrated Systems
2024-2025 Master semester 3



Exams and Grading

- **Grading is based on**
  - 2 projects: during the semester
    - Full custom design project: **due on Thursday 14.11.2024**
    - Semi-custom design project: **due on Friday 20.12.2024**
  - Final exam:
    - Questions on the lectures & labs
    - Pen-and-paper calculations with results to be entered in moodle quiz

	Weight	
• **Weekly quiz**	**10%**	**every week on moodle**
• **2 projects:**	**50%**	**during the semester (reports)** (due dates: 12.11.25 (8pm) & TBA)
• **Final exam**	**40%**	**during the exam session**

Detailed Course Schedule 2024

Week	Day	1st hour	2nd hour	3rd hour
11.9.2024	Thursday	Class	Class	Class
12.9.2024	Friday	Class	Class	Class
18.9.2024	Thursday	FC LAB-1 Tutorisl: Schematic	FC LAB-1 Tutorisl: Schematic	FC LAB-1 Tutorisl: Schematic
19.9.2024	Friday	Class	Class	Class
25.9.2024	Thursday	FC LAB-2 Tutorial: Simulation	FC LAB-2 Tutorial: Simulation	FC LAB-2 Tutorial: Simulation
26.9.2024	Friday	FC LAB-2 Tutorial: Simulation	FC LAB-2 Tutorial: Simulation	FC LAB-2 Tutorial: Simulation
2.10.2024	Thursday	Class	Class	Class
3.10.2024	Friday	Class	Class	Class
09.10.2024	Thursday	Class	FC LAB-3 Tutorial: Layout	FC LAB-3 Tutorial: Layout
10.10.2024	Friday	FC LAB-3 Tutorial: Layout	FC LAB-3 Tutorial: Layout	FC LAB-3 Tutorial: Layout
16.10.2024	Thursday	FC LAB Project	FC LAB Project	FC LAB Project
17.10.2024	Friday	FC LAB Project	FC LAB Project	FC LAB Project
23.10.2024	Thursday			
24.10.2024	Friday			

Detailed Course Schedule 2024

Week	Day	1st hour	2nd hour	3rd hour
30.10.2024	Thursday	Class	Class	Class
31.11.2024	Friday	FC LAB Project	FC LAB Project	FC LAB Project
06.11.2024	Thursday	Class	Class	Class
07.11.2024	Friday	FC LAB Project	FC LAB Project	FC LAB Project
13.11.2024	Thursday	Class	Class	Class
14.11.2024	Friday	LAB Memory / Logical Effort	LAB Memory / Logical Effort	LAB Memory / Logical Effort
20.11.2024	Thursday	Class	Class	Class
21.11.2024	Friday	Class	SC LAB/Project Frontend	SC LAB/Project Frontend
27.11.2024	Thursday	SC LAB/Project Frontend	SC LAB/Project Frontend	SC LAB/Project Frontend
28.11.2024	Friday	SC LAB/Project Frontend	SC LAB/Project Frontend	SC LAB/Project Frontend
04.12.2024	Thursday	Class	Class	Class
05.12.2024	Friday	Class	SC LAB/Project Backend	SC LAB/Project Backend
11.12.2024	Thursday	SC LAB/Project Backend	SC LAB/Project Backend	SC LAB/Project Backend
12.12.2024	Friday	SC LAB/Project Backend	SC LAB/Project Backend	SC LAB/Project Backend
18.12.2024	Thursday	SC LAB/Project Backend	SC LAB/Project Backend	SC LAB/Project Backend
19.12.2024	Friday	SC LAB/Project Backend	SC LAB/Project Backend	SC LAB/Project Backend

Legal considerations

- **The use of EDA tools and design kits is subject to NDAs (Non Disclosure Agreements) between EPFL, the Europractice program, EDA vendors and technology providers.**
- **The use of EDA tools and design kits shall be strictly limited to courses and student projects**
  - All files related to EDA tools and design kits shall be kept in EPFL working locations related to courses or projects
  - Electronic documentation (e.g., pdf files) shall not be printed

- **Filled documents must be uploaded on moodle. No submission means that you cannot continue the labs.**
- **You are strictly forbidden from copying any sensitive data from the servers, or release anything online.**
- **You may be personally liable in case of non-respect of the rules**
- ***Every user of the EPFL information infrastructure agreed on the federal law governing EPFL.***
  - *LEX 6.5.1 the Information Systems Security Policy*

    https://www.epfl.ch/about/overview/wp-content/uploads/2019/09/6.5.1_Politique_securite_SI_an.pdf
  - *LEX 6.1.4 the use of Electronic Infrastructure*

    https://www.epfl.ch/about/overview/wp-content/uploads/2020/01/LEX-6.1.4_EN.pdf
  - *LEX 6.1.5 Use of Software Subject to a License Agreement*

    https://www.epfl.ch/about/overview/wp-content/uploads/2019/09/LEX-6.1.5_EN.pdf
  - *Associated Disciplinary measures*

    Students

    https://www.epfl.ch/about/overview/wp-content/uploads/2019/09/2.4.0.2Disciplinary_Rules_Regulations_ang.pdf

    Employees

    https://www.fedlex.admin.ch/eli/cc/2001/279/fr

In Practice

- **Read and Sign the Statement on EDA from moodle**
- **Submit it on moodle**

- **Respect the rules and enjoy the lab**

EPFL

Statement on the use of EDA Tools and Design Kits for classes in EPFL

The use of EDA tools and design kits is subject to NDAs (Non-Disclosure Agreements) between EPFL, the Europractice initiative, EDA vendors and technology providers. EPFL commits that its users will respect the End User License Agreements (EULA) associated with it. The corresponding EULAs can be freely requested for review to your EDA support team (alexandre.levisse@epfl.ch).

In summary:

- The technologies and EDA tools licenses which I have access through my edauser account are strictly limited to the needs of courses and student projects.
- All files related to EDA tools and design kits as well as outputs of EDA tools shall be kept in EPFL working locations related to courses or projects.
- It is forbidden to copy anything from the server to any non-EPFL device (computer, smartphone, hard-drive, usb key etc.), to any cloud service or email box.
- Only explicitly requested assignments by teachers can be exported for submission on EPFL's Moodle.
- Electronic documentation (e.g., pdf files) shall not be printed or electronically distributed.

By filling and signing this document,

- I declare that I'm aware and I will comply with the above conditions, and acknowledge that I may be personally liable if I do not respect them.
- I agree that I will only use the edauser account for classes and student projects.

Name (last, first, PRINTED CHARACTERS): .....

Section (student) / Unit (researcher): ..... SCIPER nr.: .....

EPFL email: ..... Username: .....

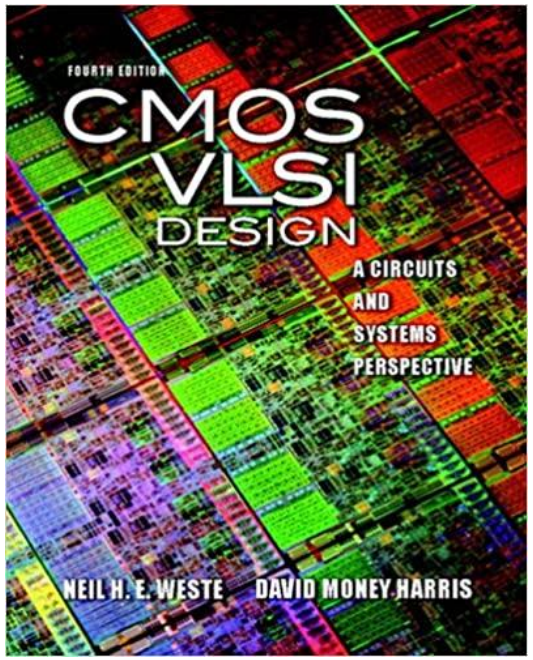
Date: ..... Signature: .....

Literature

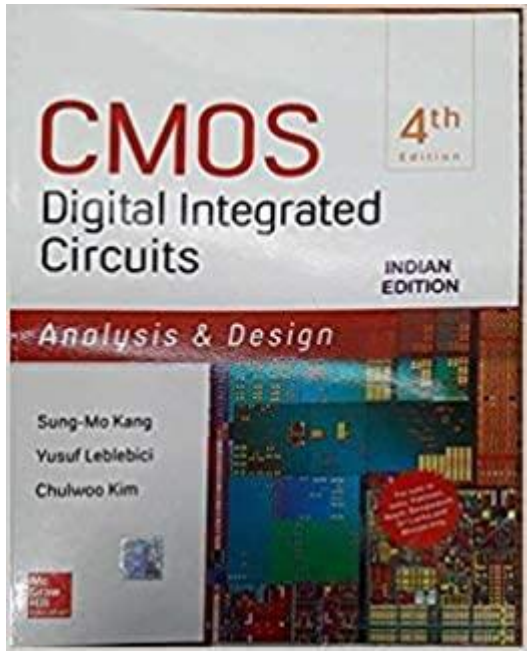
- **Slides and notes from the lecture will be weekly available on Moodle**

- **Class follows loosely two books:**

Also as eText Book



CMOS VLSI Design: A Circuits and Systems Perspective
Neil Weste, David Harris
4th Edition
ISBN-13: 978-0321547743
ISBN-10: 0321547748



CMOS Digital Integrated Circuits
Kang, Leblebici, Kim
4th Edition
ISBN-10 : 9352602145
ISBN-13 : 978-9352602148