SECTION OF ELECTRICAL ENGINEERING

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Fundamentals of VLSI – project Full Custom
SEL October 2025

Full Custom Project
Layout, verification and assignments

1. BASIC RULES OF ENGINEERING – REMINDER

- **Engineers are lazy**

If something takes too long, you are doing something wrong.

- **Divide and Conquer**

Divide complex problems into a collection of smaller simpler problems, solve one by one.

- **Simple and Regular**

Try simple and regular structures, they are easier to design and debug.

- **Engineering is not a religion**

Find the solution that best fits your problem

2. FLOOR PLANNING AND DEFINITION OF THE LAYOUT STRATEGY

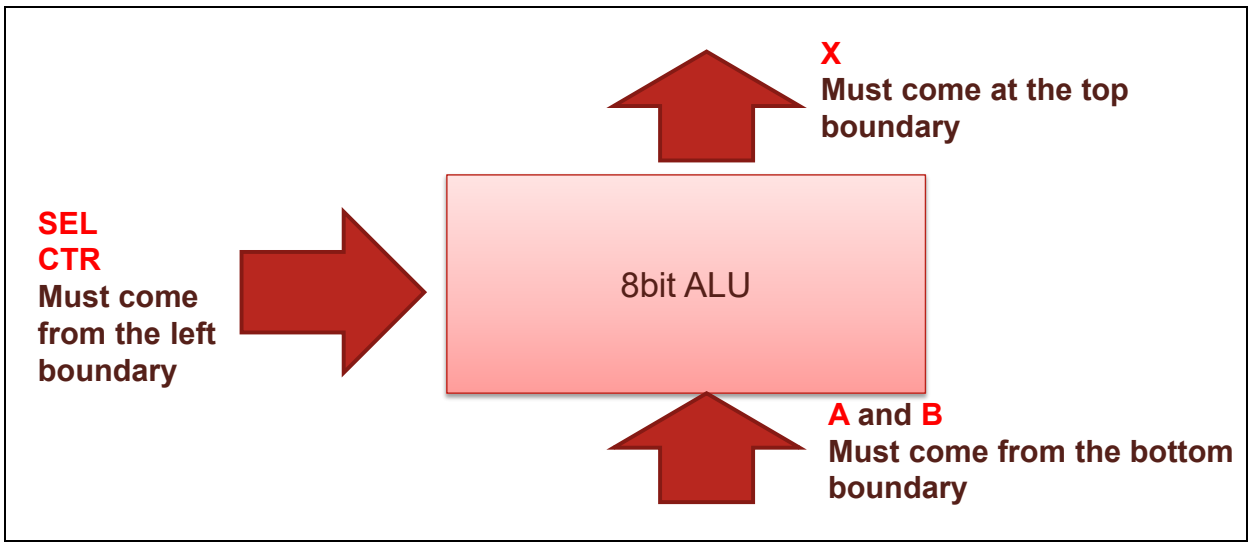
Before drawing the layout of each block, some constrains like block placement, power routing or signal flow need to be determined. Without this initial step, drawing the layout of complex circuits becomes very difficult and inefficient. **At the end of the project, your layout must be smaller than 500um2.**

2.1. DETERMINING THE BLOCK PLACEMENT

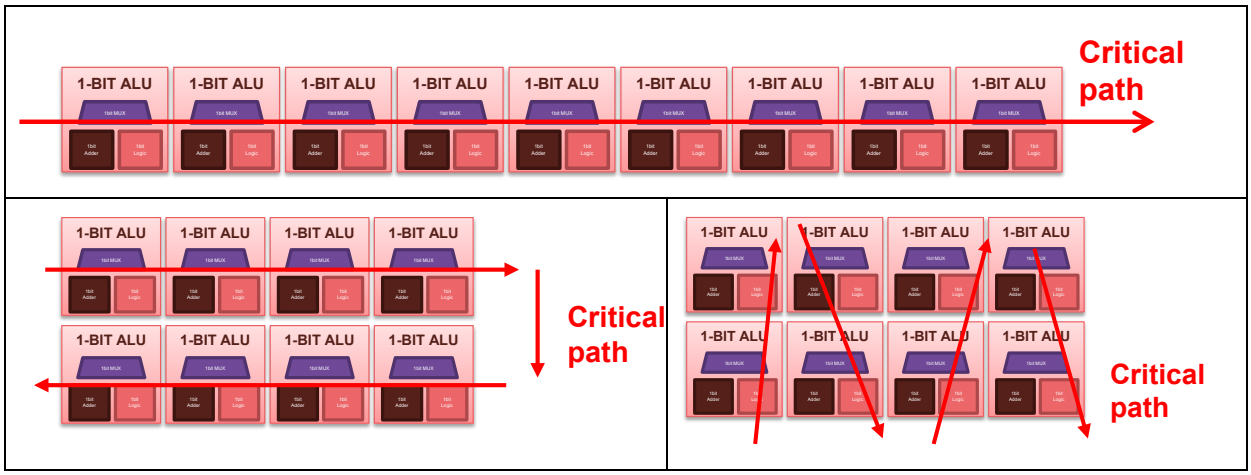
First you must decide on how to place the different blocks of the system. The easiest approach would be to either place the blocks horizontally or vertically as shown in Figure 13. You can also choose some other approach or the order in which you want to place the blocks. Your choice should strongly depend on the interconnection between the blocks in order to have as easy as possible routing. Note that the final shape

of your design **has to be rectangular**. It may be that you have dead spaces in your floorplan, if so, you still have to count them in the final area.

The block placement depends on the global signal flow. Your signal flow must be as follow for the top 8bit ALU. Input signals come from the bottom boundary, outputs are expected on the top boundary. And control signals come from the left.

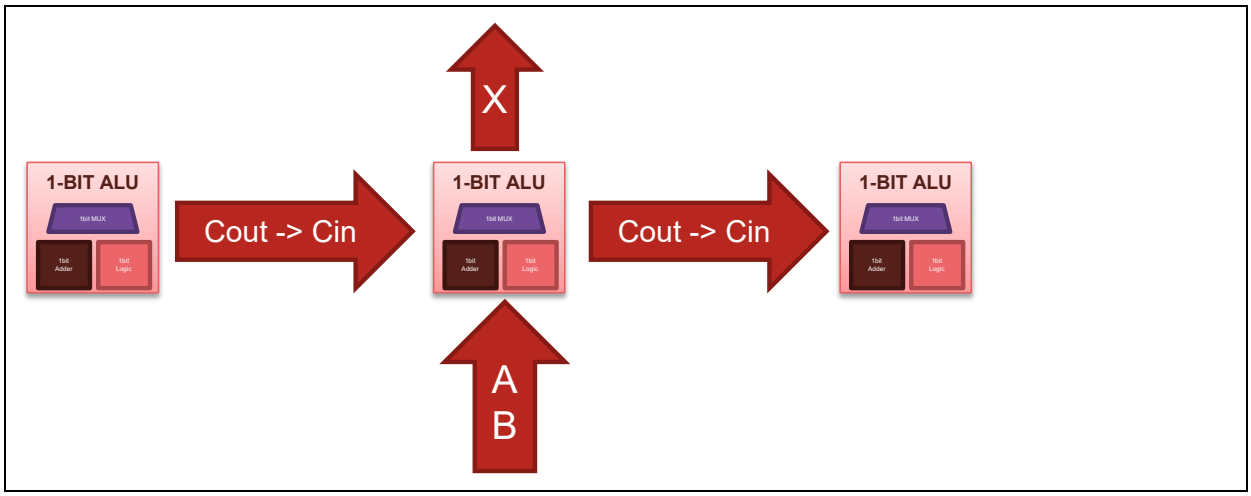


Inside the 8bit alu, you are quite free on how to place the 1bit alu cells. Along one line, along two lines ? vertically ? horizontally ?



Feel free to explore one possible physical organization. The ones shown here are just some examples. Remember that, in order to minimize timing, you may want to minimize the distance between the output of the block and the boundary. Also remember that, as the signal propagate, not all the 1bit ALU have strong constraints on their outputs. Same for the inputs.

Propagate this mindset down the circuit hierarchy. This will help you figure out how to place the 1bit adder, mux, and logic blocks.



Make a drawing, on paper of the floorplan for your circuit.

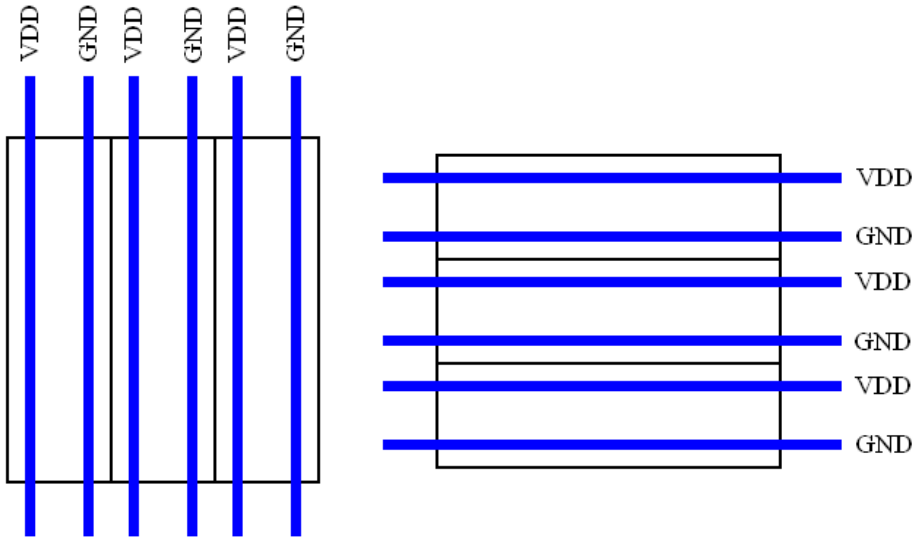
- For the 1bit ALU
- For the 8bit ALU

2.2. POWER PLANNING AND POWER DIRECTION

Define the power directions of your design. Will the power rails be horizontal or vertical ? Keep it consistent. Generally, try not to mix horizontal and vertical gates.

On the top level, the power must come from two ME4 1um wide vertical or horizontal wires, one for VDD, one for GND. Think about a plan for bringing the power to the ME1 lines inside the standard cells.

How will you organize the power grid?



Two Examples of Power Supply Line Directions

2.3. INTRODUCING TAP CELLS

Substrate biasing is one of the most important part of the design. Make sure that you leave enough space to bias the NWELL and P-substrate. DRC will issue errors and LVS will not be able to recognize your transistors if you miss substrate biasing. A good practice consists in including regularly TAP cell and have one cell at each end of a line to sure good transistor biasing.

In this technology, tap cells should be added every 30um. If not respected, the DRC or LVS will complain.

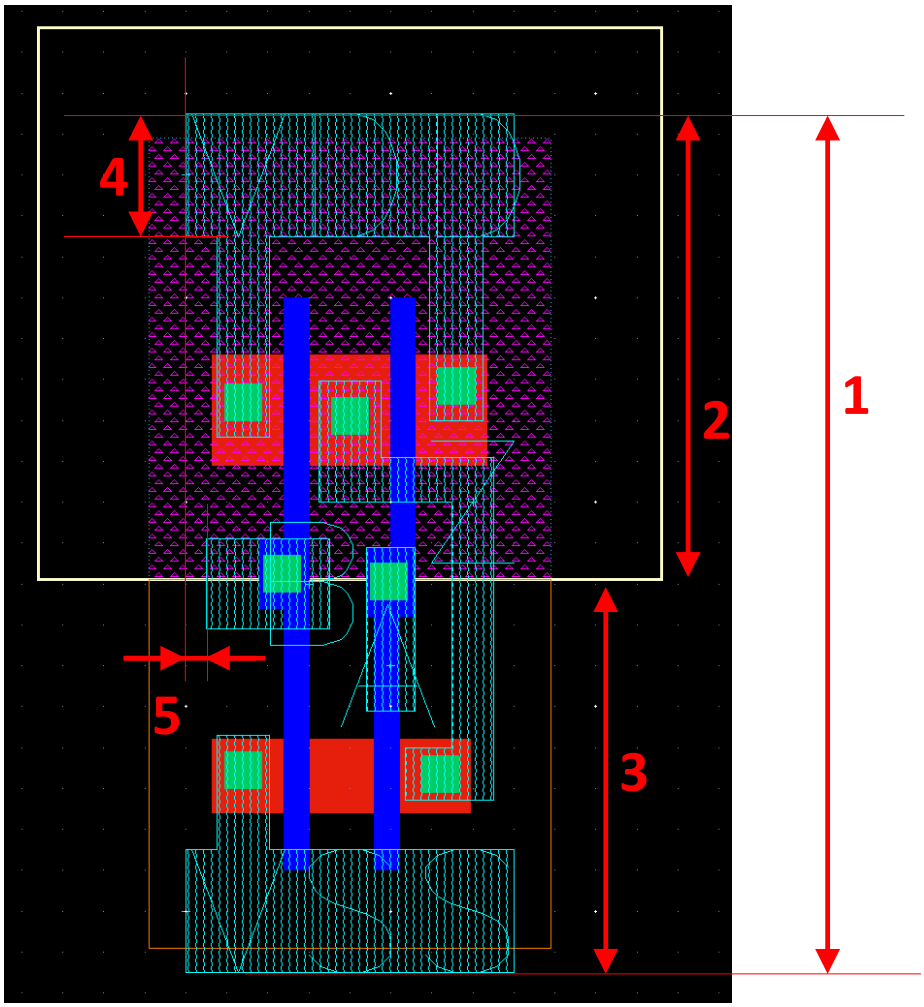
3. LAYOUT OF THE BASIC CELLS

In this section, you will design the basic cells you used in your design.

3.1. DEFINE STANDARDS FOR ALL THE CELLS

Define a standard structure for all the cells. This is described in slide 37 of the class.

As in the following example, define a framework that you will use in the design of your logic gates. Draw your target on paper, to make sure you understand it. Do not overdo it, just make sure that you chose some guidelines, and follow them for all the gates. Take a bit or margin, and sketch all the gates you need on paper first, to not get nasty surprises.



1. **The height of the cell, from the bottom of the VSS to the top of the VDD rail.**

This corresponds to the height you have for your standard cell. Note that once your cells will be organized together, the actual available space is not “1”, but “1-4”, as the VDD and VSS rails will be shared with the above and below cells.

You can define the height almost arbitrarily between 2 and 3.5um. For e.g. the standard cell library of UMC takes 2.1um (this is quite challenging). Generally taller cells will give you more space for routing and sizing larger transistors without having to do multiple-finger transistors. Smaller cells will allow for a more compact design, but will limit the maximum W you can fit before you need to use multi-finger transistors.

2. **The height of the NWELL. From the top of the VDD rail to the middle of the cell.**

This corresponds to the height of the common NWELL for all your cells. In practice, the available area for your transistors will be the distance from the bottom of the VDD rail, to the bottom of the NWELL.

Note that the minimum distance from the NWELL to a transistor active area (DF), as described in the TLR page 17, is 150nm (NW-N_DF.S3) → this will give you an insight on how close from the bottom of the NWELL could you transistors be. Note that you also have to place contacts to the transistors gates there, so, you also need to keep a bit of space.

For the top side, the limit will be given (cf TLR page 28)

- By the minimum polysilicon extension on top of the diffusion (OH.2 = 140nm)
- By the polysilicon-to-polysilicon distance (the distance to the mirrored polysilicon in the neighbour logic gate), i.e., half of S.2=120nm , thereby 60nm to the middle of the VDD rail.

The remaining distance, will be the available distance to make a PMOS transistor width active area.

3. **The area for NMOS transistors. From the bottom of the NWELL to the bottom of the VSS rail.**

As for the PMOS area. The limits will be:

- On the top, the distance from DF to NW (150nm), and the distance with contacts (CO) which will be placed there.
- On the bottom, the same constraints as for the top of dimension "2", the polysilicon to polysilicon distance.

4. **Width of the VDD and VSS rails**

Define here your VDD rail width. 300nm can be a good pick.

5. **Margin to the cell edges**

Here, you want to make sure you are taking enough margin on the sides of your cells, so that when abutting them to their neighbours, you do not overlap or break spacing rules for ME1, DF, Poly , or any layer you use internally.

For e.g., for a ME1 wire, make sure that you respect the spacing S.1 (TLR page 51) with a potentially ME1 wire in a neighbouring cell. In other words, half the spacing between the metal and the cell boundary.

3.2. BUILD ALL THE CELLS WITH THE SAME STANDARD

Now that you have a framework, build the cells you need with the same structure. Make sure you are able to abut them both horizontally and vertically.

Do not forget to build a TAP cell.

Try only using ME1 and Poly inside the logic gates. If you need to use ME2, check the guidelines from the next section.

IMPORTANT : the via definition inside virtuoso (key "O") does not consider the densest rules for that technology. Check here on moodle, and use the vias provided in the **VIAS_65nmUMC** library for dense single vias.

4. LAYOUT OF THE 1BIT LOGIC, ADDER, MUX AND ALU CELLS

Assemble the different cells into 1bit blocks. And assemble them together as a 1bit ALU cell.

Inspire from the guidelines given in the class.

- Use ME1 inside the gates.
- From ME2 onward, use perpendicular routing to ease your life.
    - Select a direction for ME2 (horizontal or vertical) and stick to it.
    - Define ME3 perpendicular to ME2, ME4 perpendicular to ME3 etc.

5. LAYOUT OF THE 8BIT ALU

Assemble the different 1bit blocks into a 8bit block. Remember that the overall area must be rectangular.

Think about the following to-do-list :

- Your VDD and GND pins must be at the edge (boundary) of the circuit on 1um ME4 layer wires.
- In this technology, tap cells should be added every 30um. If not respected, the DRC or LVS will complain.
- Place the pins of the signals A<7:0> and B<7:0> at the bottom boundary of the circuit
- Place the pins of the signals SEL and CTR at the left boundary of the circuit
- Place the pins of the X<7:0> at the top boundary of the circuit

6. VERIFICATION

6.1. DRC CHECKS

Your circuit must pass the DRC on all the levels. Do regular DRC checks along the way when doing the design.

Rely on the TLR to understand the errors you may face.

6.2. LVS CHECKS

Your circuit must pass the LVS on all the layers.

> Remember that the LVS may not pass if you miss the tap cells as it will consider the bulk is not connected. One tip consists in adding a tap cell just to pass the LVS and to remove it after.

7. PARASITIC EXTRACTION

Work smart : Do not run post PEX simulations for each level, only run it on the top once you are done with the layout.

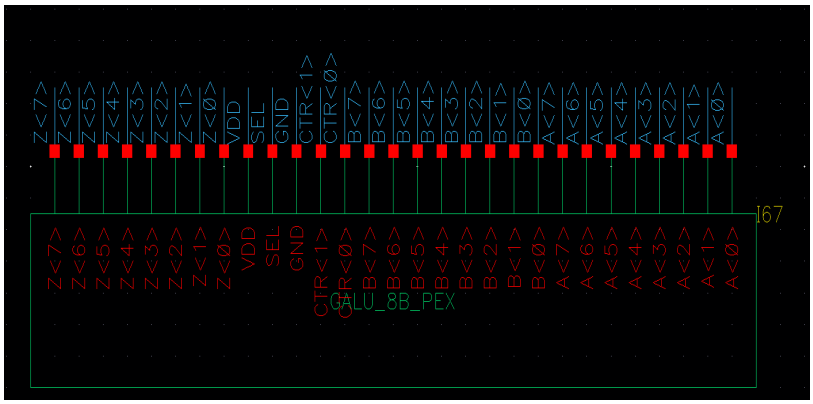
The post PEX simulation is then the same as what you did in LAB3 section 3.6.

- Import both the pre and post PEX symbols
- Adapt the names and capacitances
- Adapt the environment list
- Run the simulation

8. RE-OPTIMIZATION AND FINAL VERIFICATION

Run a simulation with the post PEX netlist and characterize the critical paths as you did in lab 3. Do not forget to add “spectreText” in the first position of the Switch View List in the environment options.

e.g. of a final ALU symbol after the PEX process. There is no constraint on the shape of the symbol. The names MUST correspond.



Hint : to create all the labels with the correct names, select the cell, and press the spacebar.

You should expect a post PEX degradation ranging from 30% to 50% compared to your schematic simulation. If it is worse than 60%, you may want to check the following parameters in your layout :

- length of the polysilicon lines. Try not having them too long. Longer than 700nm-1um may be an issue.
- Length of ME1 lines.
- Vias are resistive. And may add a lot of parasitic resistance to your signals. Doubling them can sometimes help.
- Long wires driven by small drivers

9. GRADING AND DELIVERABLE PREPARATION

Fail/Pass criterion :

- The extracted design must not return any error with the automated test and the slowest delay be below 1ns
- The design must be smaller than 500um2
- The design must have a correct functionality
- No DRC/LVS errors

Additional metrics:

- Faster designs get a better grade
  - We apply a delay*area product to evaluate them
- Floorplan quality/justification
- Good practice in terms of routing, power management, substrate biasing

9.1. REPORT DELIVERY

Fill the powerpoint with your timing, area metrics as well as your screenshots as requested. You can submit it either as a PDF or PPTX format. **Do not use any other format**.

➔ The reference PPTX can be found on moodle.

9.2. ARCHIVE OF THE DESIGN LIBRARY

The file lastname_FCproject.tar.gz shall include the full EDATP library. To create this file, follow these instructions :

1. close virtuoso
2. from your terminal, go in your EE429_FULLCUSTOM folder
3. Run the following command : **tar -zcvf lastname_FCproject.tar.gz EDATP** (this command will create an archive in your EE429_FULLCUSTOM folder that you can then upload on moodle).
4. submit the lastname_FCproject.tar.gz archive on moodle

Please note that in order to upload the file from the servers, you have to launch Firefox from the Linux terminal (simply type: firefox). Then you will be able to login on the moodle and complete the submission.

9.3. NETLISTS

submit the two netlists :

- schematic
- post-PEX