Fundamentals of Analog VLSI Design
Exercise 9 - Solution

Fully-differential OTAs and Common-mode Feedback (CMFB)

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1 Problem 1: Fully-differential Simple OTA

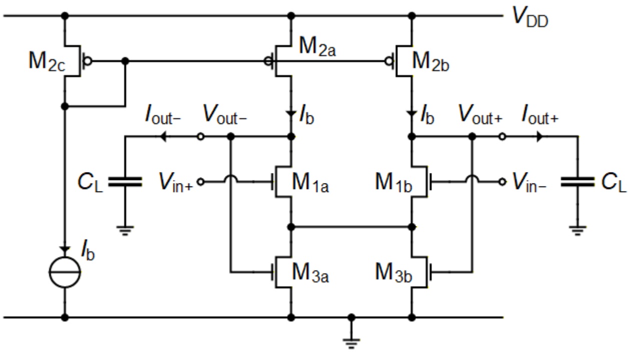

Figure 1.1: Schematic of the fully differential simple OTA.

- What is approximately the level of the common-mode output voltage $V_{oc} \triangleq (V_{out+} + V_{out-})/2$?

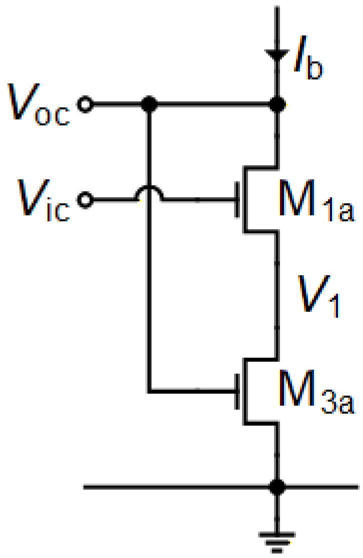

Figure 1.2: Schematic for evaluating the common-mode output voltage.

Assuming a perfectly symmetrical circuit, the output common-mode voltage V_{oc} can be evaluated with the help of the schematic shown in Figure 1.2. Assuming that M_{1a}-M_{1b} are biased in strong inversion and in saturation we have

$$I_b = \frac{\beta_1}{2\,n_1}\,(V_{ic} - V_{T0n} - n_1\,V_1)^2. \tag{1.1}$$

For a given bias current I_b, the input-common-mode voltage V_{ic} sets the voltage V_1 at the source node of M_{1a} according to

$$V_1 = \frac{V_{ic} - V_{T0n}}{n_1} - \sqrt{\frac{2\,I_b}{n_1\,\beta_1}}. \tag{1.2}$$

Assuming that M_{3a}-M_{3b} are biased in strong inversion and in the linear region we have

$$I_b = \beta_3\left(V_{oc} - V_{T0n} - \frac{n_3}{2}\,V_1\right)V_1 \tag{1.3}$$

If we can additionally assume that $V_1 \ll 2(V_{oc} - V_{T0n})/n_3$ then

$$I_b \cong \beta_3 \left(V_{oc} - V_{T0n}\right) V_1. \tag{1.4}$$

Solving for V_{oc} we get

$$V_{oc} \cong \frac{I_b}{\beta_3 V_1} + V_{T0n} = n_1 \frac{\beta_1}{\beta_3} \frac{I_b}{V_{ic} - V_{T0n} - \sqrt{2 n_1 \beta_1 I_b}}. \tag{1.5}$$

We see that the output common-mode voltage depends on the input common-mode voltage: increasing V_{ic} decreases V_{oc}. This dependence will be illustrated in the calculation of the small-signal common-mode voltage gain A_c done below.

We also see that V_{oc} is strongly dependent on technology parameters such as V_{T0n} and μC_{ox}. This should be avoided. The circuit in Problem 2 will show an example of how to better control the output common-mode voltage which is independent of the technology parameters and is only limited by matching.

- Derive the small-signal differential-mode transconductance

$$G_{md} = \frac{\Delta I_{out+} - \Delta I_{out-}}{\Delta V_{id}} \tag{1.6}$$

  and the differential gain-bandwidth product GBW_{dm} assuming a perfectly symmetrical circuit.

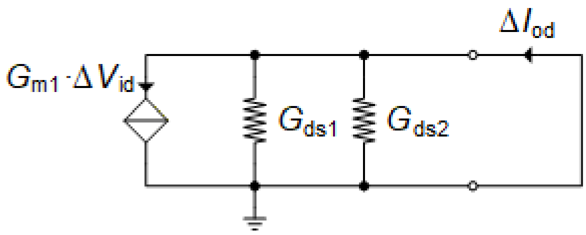

Figure 1.3: Small-signal schematic for evaluating G_{md}.

In differential mode and assuming a perfectly symmetrical circuit, the common-source node of the differential pair stays constant and can be considered as a small-signal AC ground. The small-signal schematic then simplifies to the circuit shown in Figure 1.3. The differential-mode transconductance is then simply equal to the transconductance of $\mathrm{M_{1a}}$

$$G_{md} = G_{m1}. \tag{1.7}$$

The corresponding differential-mode gain-bandwidth product is then simply

$$GBW_{dm} = \frac{G_{m1}}{C_L}. \tag{1.8}$$

- Calculate the small-signal common-mode transconductance G_{mc} of the CMFB circuit in open-loop

$$G_{mc} = \frac{\Delta I_{out-}}{\Delta V_{G3a}} = \frac{\Delta I_{out+}}{\Delta V_{G3b}}. \tag{1.9}$$

  To do this you need to disconnect the gates of M_{3a} and M_{3b} from the outputs. The open-loop common-mode transconductance is then obtained by applying a common-mode voltage at the gates of M_{3a} and M_{3b} and measuring the common-mode output current. Hint: Assuming a perfectly symmetrical circuit, you can use the half-circuit in common-mode operation.

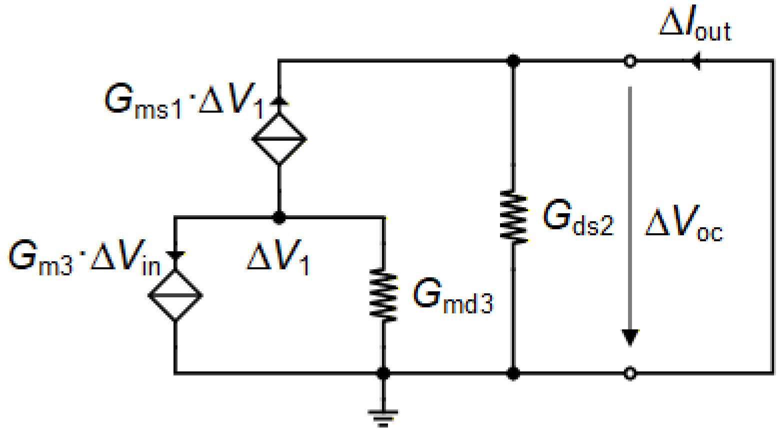

Figure 1.4: Small-signal schematic for calculating the open-loop common-mode transconductance G_{mc}.

To calculate the open-loop common-mode transconductance G_{mc} we disconnect the gates of M_{3a} and M_{3b} from the outputs and connect them to a input voltage ΔV_{in}. Assuming that the transistors in the left and right branches are perfectly matched and that M_{3a}-M_{3b} are biased in the linear region, we get then equivalent circuit shown in Figure 1.4, where we have neglected the output conductances. Analyzing this circuit we obtain the open-loop common-mode transconductance as

$$G_{mc} = \frac{G_{m3}\,G_{ms1}}{G_{md3} + G_{ms1}} = \frac{G_{m3}}{1 + G_{md3}/G_{ms1}}. \tag{1.10}$$

This seems reasonable since the input voltage ΔV_{in} is first transformed into a current through G_{m3} and then to the voltage ΔV_1 by the load conductance $G_{md3} + G_{ms1}$ and finally to the output current by G_{ms1}.

If we assume that M_{3a}-M_{3b} are biased in strong inversion and in the linear region, then

$$G_{m3} = \beta_3 \cdot V_{D3}, \tag{1.11}$$
$$G_{md3} = n_3 \cdot \beta_3 \cdot (V_{P3} - V_{D3}) \cong \beta_3 \cdot (V_{G3} - V_{T0n} - n_3 \cdot V_{D3}). \tag{1.12}$$

The gate voltage of M_{3a}-M_{3b} is equal to the output common-mode voltage V_{oc}.

If we assume that M_{1a}-M_{1b} are biased in strong inversion then

$$G_{ms1} = n_1 \cdot \beta_1 \cdot (V_{P1} - V_{S1}) = n_1 \cdot \beta_1 \cdot (V_{P1} - V_{D3}) = \beta_1 \cdot (V_{ic} - V_{T0n} - n_1 \cdot V_{D3}) \tag{1.13}$$

Assuming that $n_1 = n_3$, we get

$$\frac{G_{md3}}{G_{ms1}} = \frac{\beta_3 \cdot (V_{oc} - V_{T0n} - n \cdot V_{D3})}{\beta_1 \cdot (V_{ic} - V_{T0n} - n \cdot V_{D3})}. \tag{1.14}$$

If additionally we assume that the output common-mode voltage is set to the input common-mode voltage $V_{oc} = V_{ic}$, then the G_{md3}/G_{ms1} ratio only depends on the β ratio

$$\frac{G_{md3}}{G_{ms1}} \cong \frac{\beta_3}{\beta_1}. \tag{1.15}$$

If $\beta_1 \gg \beta_3$, then $G_{md3}/G_{ms1} \ll 1$ and

$$G_{mc} \cong G_{m3}. \tag{1.16}$$

The corresponding common-mode gain-bandwidth product is then given by

$$GBW_{cm} = \frac{G_{mc}}{C_L} = \frac{G_{m3}\,G_{ms1}}{C_L\,(G_{md3} + G_{ms1})}. \tag{1.17}$$

In the case $G_{md3} \ll G_{ms1}$, then

$$GBW_{cm} \cong \frac{G_{m3}}{C_L}. \tag{1.18}$$

Since G_{m3} depends on its drain voltage according to $G_{m3} \cong \beta_3 \cdot V_{D3}$ it is directly linked to the input common voltage $V_{D3} = V_{ic} - V_{GS1}$. The common-mode gain-bandwidth product will depend on the input common-mode voltage which is not ideal.

- How do they compare?

The ratio G_{md}/G_{mc} is given by

$$\frac{G_{md}}{G_{mc}} = \frac{G_{md3} + G_{ms1}}{n_1\, G_{m3}}. \tag{1.19}$$

Assuming again that $G_{md3} \ll G_{ms1}$, we have

$$\frac{G_{md}}{G_{mc}} \cong \frac{G_{m1}}{G_{m3}}. \tag{1.20}$$

where we have used $G_{ms1} = n_1 \cdot G_{m1}$. Assuming again that M_{1a}-M_{1b} are biased in strong inversion then

$$G_{m1} = \beta_1 \cdot (V_{P1} - V_{S1}) = \beta_1 \cdot (V_{P1} - V_{D3}) = \frac{\beta_1}{n_1} \cdot (V_{ic} - V_{T0n} - n_1 \cdot V_{D3}) \tag{1.21}$$

and

$$\frac{G_{md}}{G_{mc}} \cong \frac{\beta_1}{\beta_3} \cdot \left(\frac{V_{P3}}{V_{D3}} - 1\right) = \frac{\beta_1}{\beta_3} \cdot \left(\frac{V_{ic} - V_{T0n}}{n_1 \cdot V_{D3}} - 1\right), \tag{1.22}$$

which is usually larger than 1. This means that the common-mode gain-bandwidth GBW_{cm} is unavoidably smaller than the differential-mode gain-bandwidth product GBW_{dm} which is usually not desired.

- Calculate the small-signal differential voltage gain $A_d \triangleq \Delta V_{od}/\Delta V_{id}$ assuming a perfectly symmetrical circuit where $\Delta V_{id} \triangleq \Delta V_{in+} - \Delta V_{in-}$ and $\Delta V_{od} \triangleq \Delta V_{out+} - \Delta V_{out-}$ are the input and output small-signal differential voltages. Deduce the differential DC voltage gain A_{d0}, the cut-off frequency $\omega_{c,dm}$ and the differential mode gain-bandwidth product GBW_{dm}.

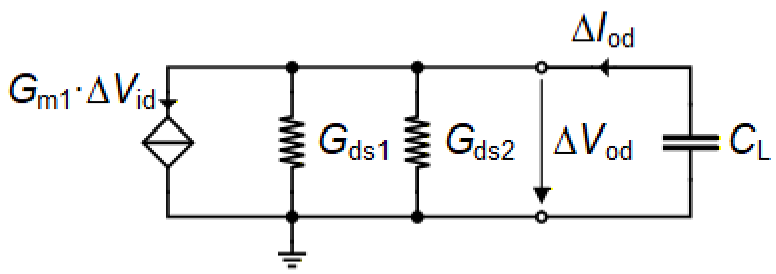

Figure 1.5: Small-signal schematic for calculating the differential voltage gain.

The small-signal circuit in differential mode assuming that the left and right branches are perfectly matched is shown in Figure 1.5. The small-signal differential voltage gain is then given by

$$A_d \triangleq \frac{\Delta V_{od}}{\Delta V_{id}} = \frac{A_{d0}}{1 + \frac{s}{\omega_{c,dm}}} \tag{1.23}$$

where

$$A_{d0} \cong -\frac{G_{m1}}{G_{ds1} + G_{ds2}}, \tag{1.24}$$

$$\omega_{c,dm} \cong \frac{G_{ds1} + G_{ds2}}{C_L}. \tag{1.25}$$

are the differential-mode DC gain and bandwidth, respectively. As expected, the gain-bandwidth product is equal to

$$GBW_{dm} = |A_{vd0}| \cdot \omega_{c,dm} = \frac{G_{m1}}{C_L}, \tag{1.26}$$

which is consistent with the result found above.

- Calculate the small-signal common-mode voltage gain $A_c \triangleq \Delta V_{oc}/\Delta V_{ic}$ assuming a perfectly symmetrical circuit where $\Delta V_{ic} \triangleq (\Delta V_{in+} + \Delta V_{in-})/2$ and $\Delta V_{oc} \triangleq (\Delta V_{out+} + \Delta V_{out-})/2$ are the input and output common-mode voltages. Deduce the common-mode DC voltage gain A_{c0}, the cut-off frequency $\omega_{c,cm}$ and the common-mode gain-bandwidth product GBW_{cm}.

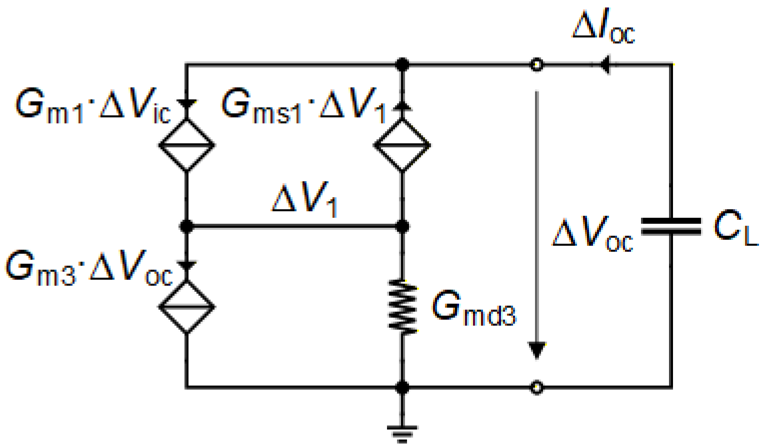

Figure 1.6: Small-signal schematic of the fully differential simple OTA in common-mode operation (closed-loop).

Assuming again a perfectly symmetrical circuit and neglecting the output conductances, the small-signal circuit in common-mode operation simplifies to Figure 1.6. The common-mode voltage gain is then given by

$$A_c \triangleq \frac{\Delta V_{oc}}{\Delta V_{ic}} = \frac{A_{c0}}{1 + \frac{s}{\omega_{c,cm}}}. \tag{1.27}$$

where the common-mode DC gain A_{c0} and bandwidth $\omega_{c,cm}$ are given by

$$A_{c0} \cong -\frac{G_{md3}}{n_1\, G_{m3}}, \tag{1.28}$$

$$\omega_{c,cm} \cong \frac{G_{m3}\, G_{ms1}}{(G_{md3} + G_{ms1})\, C_L} \cong \frac{G_{m3}}{C_L}, \tag{1.29}$$

for $G_{ms1} \gg G_{md3}$. Note that, since the feedback gain is unity, the bandwidth $\omega_{c,cm}$ actually corresponds to the open-loop common-mode gain-bandwidth product GBW_{cm} calculated above.

Reusing the expressions of G_{m3} and G_{md3} found above, the DC common-mode voltage gain is given by

$$A_{c0} \cong -\frac{n_3}{n_1}\frac{V_{P3} - V_{D3}}{V_{D3}} \cong 1 - \frac{V_{P3}}{V_{D3}} \cong 1 - \frac{V_{G3} - V_{T0n}}{n_3\, V_{D3}} = 1 - \frac{V_{oc} - V_{T0n}}{n_3\, V_{D3}}, \tag{1.30}$$

where we have assumed that $n_1 \cong n_3$. Usually, V_{P3} cannot be made much larger than V_{D3} and therefore the common-mode DC gain remains small, which is not really a problem. It is actually even better because if the common-mode gain is small, any common-mode error at the input does not propagate to the output.

- Calculate the corresponding DC $CMRR = A_{d0}/A_{c0}$.

The DC $CMRR$ is then simply given by

$$CMRR \triangleq \left|\frac{A_d}{A_c}\right| \cong \frac{G_{m1}}{G_{ds1} + G_{ds2}} \cdot \frac{n_1\, G_{m3}}{G_{md3}}. \tag{1.31}$$

- Calculate the common-mode to differential-mode voltage gain $A_{cd} \triangleq \Delta V_{od}/\Delta V_{ic}$ assuming there is a G_m-mismatch ΔG_{m1} between M_{1a} and M_{1b}.

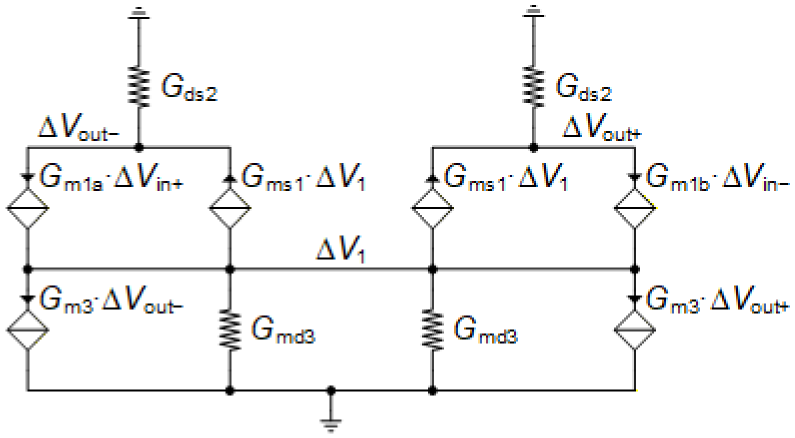

Figure 1.7: Small-signal schematic of the fully differential simple OTA to calculate the common-mode to differential-mode voltage gain due to a G_{m1} mismatch.

To calculate the effect of the G_m mismatch in the differential pair, we use the small-signal schematic shown in Figure 1.7. Assuming that all the components are symmetrical except for G_{m1a} and G_{m1b}, the common-mode to differential-mode voltage gain is then given by

$$A_{cd} \triangleq \frac{\Delta V_{od}}{\Delta V_{ic}} = \frac{\Delta G_{m1}}{G_{ds1} + G_{ds2}}, \tag{1.32}$$

where $\Delta G_{m1} = G_{m1a} - G_{m1b}$. The ratio of the differential gain A_d to the common-mode input to differential output gain A_{cd} is then given by

$$\left|\frac{A_d}{A_{cd}}\right| \cong \left(\frac{\Delta G_{m1}}{G_{m1}}\right)^{-1}. \tag{1.33}$$

The ratio of the differential gain A_d to the common-mode input to differential output gain A_{cd} is inversely proportional to the relative G_m error in the differential pair M_{1a}-M_{1b}.

- Propose a way to improve the CMFB offering a better control on the output common-mode voltage without increasing the current consumption.

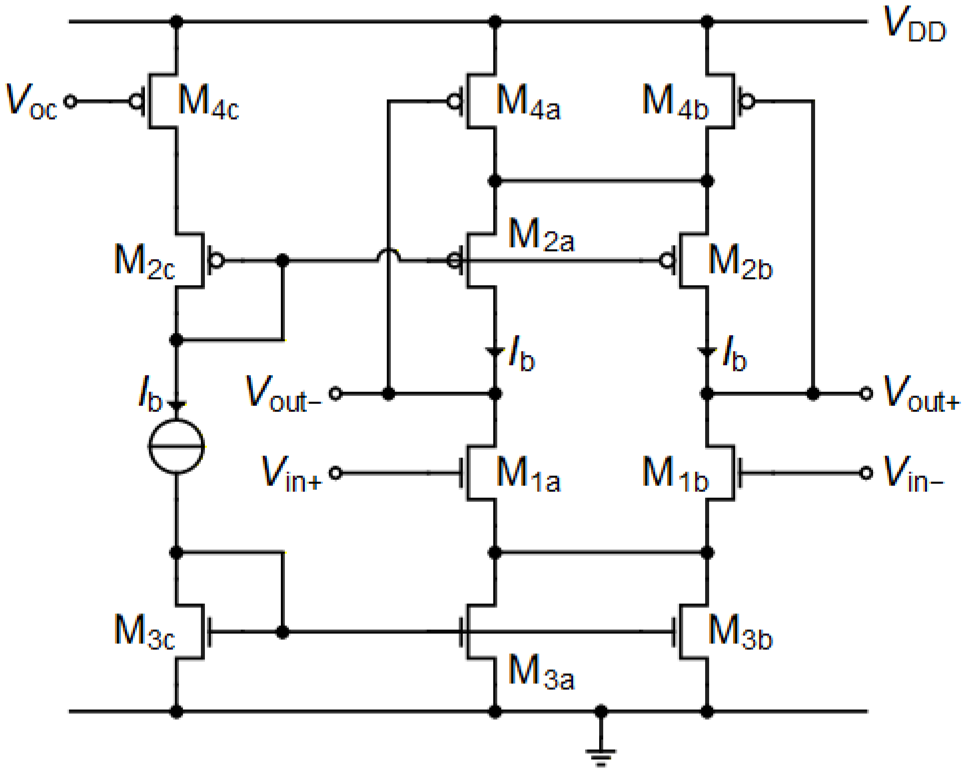

Figure 1.8: Fully differential simple OTA with a CMFB controlling the output common-mode from the top current sources.

The CMFB used in the OTA of Figure 1.1 is very simple and current efficient, but not ideal, because the common-mode gain and gain bandwidth product are set by the input-common mode voltage. There are no additional degrees of freedom to set them independently of the input common-mode voltage. Additionally, the output common-mode voltage depends heavily on the technology parameters, which is not desirable.

The CMFB can be improved by adjusting the common-mode current from the top instead of from the bottom as shown in Figure 1.8. With this CMFB circuit, the output common-mode voltage is set to the reference voltage V_{oc} by matching of the gate voltages of $\mathrm{M_{4a}}$, $\mathrm{M_{4b}}$ and $\mathrm{M_{4c}}$. It therefore does not depend on the process parameters as in the circuit of Figure 1.1 but is limited by transistor matching. However, the common-mode transconductance and gain-bandwidth product is identical to those obtained for the circuit of Figure 1.1. Another CMFB circuit allowing to set the common-mode transconductance and gain-bandwidth product independently of that of the differential mode is discussed below.

2 Problem 2: Fully Differential Folded Cascode OTA

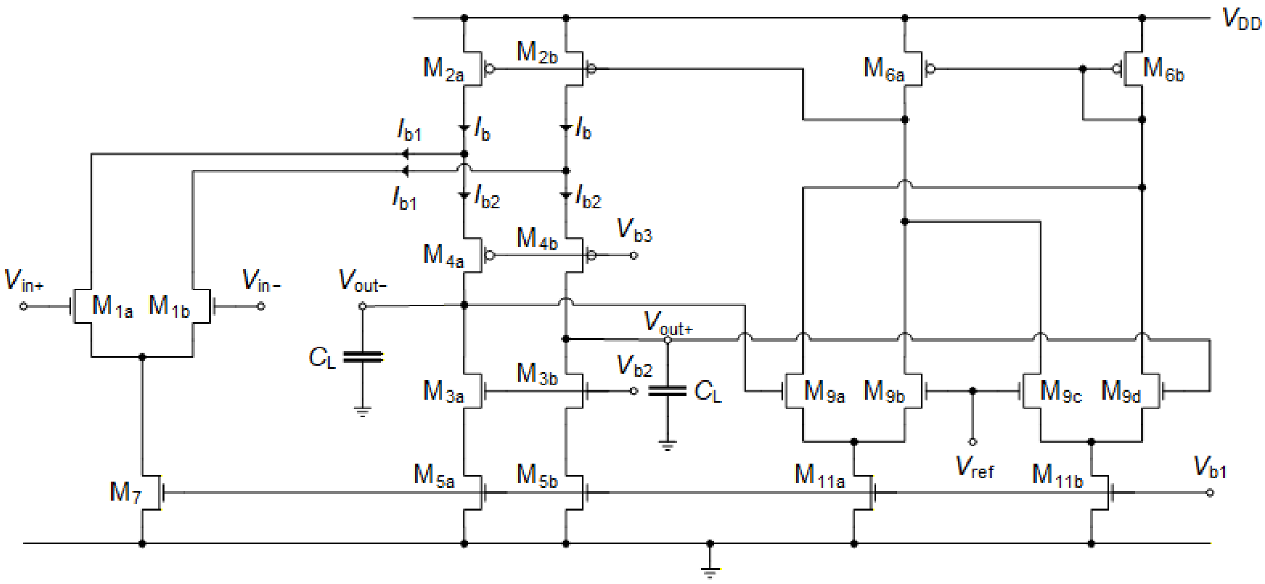

Figure 2.1: Schematic of the fully-differential folded-cascode OTA including the CMFB circuit.

- What is the level of the common-mode output voltage $V_{oc} \triangleq (V_{out+} + V_{out-})/2$?

Contrary to the CMFB of Figure 1.1, the output common-mode voltage in the fully-differential folded-cascode OTA of Figure 2.1 is set to V_{ref} by the CMFB and does not depend on the process parameters. The control of the output common-mode voltage is limited by transistor matching.

- Derive the differential-mode transconductance G_{md} and the differential gain-bandwidth product GBW_{dm} assuming the transistors in the left and right branches are perfectly matched.

The differential transconductance G_{md} is simply equal to G_{m1}. The differential gain-bandwidth product is therefore equal to

$$GBW_{dm} = \frac{G_{m1}}{C_L}. \tag{2.1}$$

- Calculate the DC open-loop common-mode transconductance $G_{mc} \triangleq \Delta I_{out}/\Delta V_{in}$ and gain bandwidth product GBW_{cm} assuming again that the transistors in the left and right branches are perfectly matched.

The DC common-mode transconductance is calculated by opening the loop at the gates of M_{9a} and M_{9d} connecting them together and applying an input voltage ΔV_{in}. It is given by

$$G_{mc} = \frac{\Delta I_{D2}}{\Delta V_{in}} = G_{m2} \cdot A_{cm} \tag{2.2}$$

where A_{cm} is the voltage gain of the differential difference amplifier

$$A_{cm} = \frac{G_{m9}}{G_o} \tag{2.3}$$

where G_o is the total conductance at the drains of M_{9b} and M_{9c}. Finally, the common-mode gain-bandwidth product is simply given by

$$GBW_{cm} = \frac{G_{mc}}{C_L}. \tag{2.4}$$

- How do they compare?

In this case, the common-mode gain-bandwidth product can be made larger than the differential-mode gain-bandwidth product by choosing

$$G_{m1} \leq G_{m2} \cdot \frac{G_{m9}}{G_o}. \tag{2.5}$$

G_{mc} and GBW_{cm} can be made larger than G_{md} and GBW_{dm} by choosing $G_{m9} = G_{m1}$.

- What is the total current consumption for $GBW_{cm} = GBW_{dm}$? How much is the current penalty compared to the single-ended case?

If we choose $G_{m9} = G_{m1}$, then the bias current of M_{9a}-M_{9b} and M_{9c}-M_{9d} are equal to that of M_{1a}-M_{1b}. This adds $4\,I_{b1}$ to the current consumption. If $I_{b2} = 1.2\,I_{b1}$ then the total current consumption is $I_{tot} = 8.4\,I_{b1}$ compared to $4.4\,I_{b1}$. The total current is therefore almost doubled.

2.1 Design Example

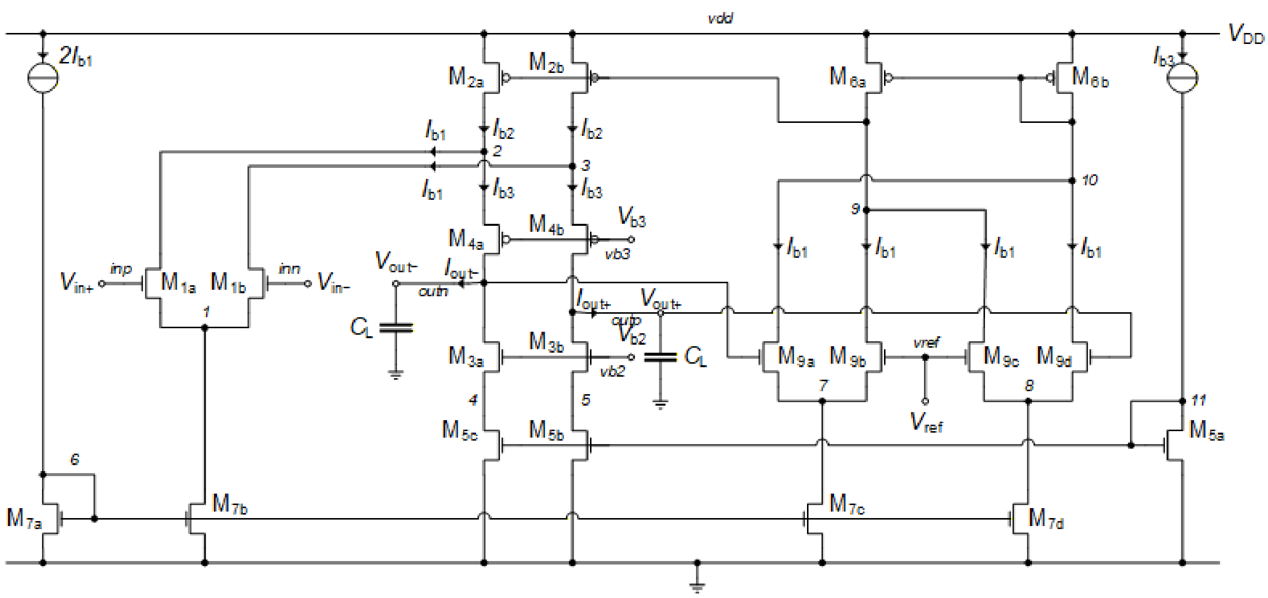

Figure 2.2: Fully differential folded-cascode OTA used for the simulation.

We want to design the fully differential cascode OTA shown in Figure 2.2 for the specifications given in Table 2.1 for a generic 180nm bulk CMOS process. The physical parameters are given in Table 2.2, the global process parameters in Table 2.3 and finally the MOSFET parameters in Table 2.4.

Table 2.1: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	100	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Input common-mode voltage	V_{ic}	0.9	V
Output common-mode voltage	V_{oc}	0.9	V
Maximum input-referred random offset voltage	V_{os}	10	mV
Phase margin	PM	60	$^\circ$

Table 2.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 2.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 2.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	20	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	6.8e-23	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$

Table 2.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

2.1.1 Design

The transconductance is given by

$$G_{m1} = \omega_u \cdot C_L \tag{2.6}$$

which for the given specs gives $G_{m1} = 6.283\ \mu A/V$. Choosing an inversion coefficient for M_{1a}-M_{1b} equal to $IC_1 = 0.1$ gives the required current to achieve the desired gain-bandwidth product $I_{b1} = 189$ nA. However this is without accounting for the parasitic capacitances that add to the load capacitances at the outputs because of M_{3b} and M_{4b} which are large transistors since they are biased in weak inversion. To have some margin we choose $I_{b1} = 250\ nA$ which gives $I_{spec1} = 2.500\ \mu A$ and $W_1/L_1 = 3.496$. The final width and length will be calculated when sizing the cascode transistors M_{4a}-M_{4b}.

For the current source M_{2a}-M_{2b} we choose $IC_2 = 10$. With the bias current $I_{b2} = 550\ nA$ we have $I_{spec2} = 55\ nA$ and $W_2/L_2 = 0.318$. The final width and length will be calculated when sizing the cascode transistors M_{4a}-M_{4b}.

For the current mirror M_{5a}-M_{5b}-M_{5c}, we choose $IC_5 = 10$. With the bias current $I_{b3} = 300\ nA$ we have $I_{spec5} = 30\ nA$ and $W_5/L_5 = 0.042$. Since the W/L is fairly small we need to set $W_5 = W_{min} = 200\ nm$, which leads to $L_5 = 5.77\ \mu m$.

To size the cascode we first calculate the output conductance G_o from the DC gain as $G_o = G_{m1}/A_{dc} = 0.063\ nA/V$. The output conductance is approximately equal to

$$G_o \cong G_{on} + G_{op}, \tag{2.7}$$

where

$$G_{on} = \frac{G_{ds5}\, G_{ds3}}{G_{ms3}}, \tag{2.8}$$

$$G_{op} = \frac{(G_{ds1} + G_{ds2})\, G_{ds4}}{G_{ms4}}. \tag{2.9}$$

We can split G_o half-half between G_{on} and G_{op}

$$\frac{G_{ds5}\, G_{ds3}}{G_{ms3}} = \frac{G_o}{2} \tag{2.10}$$

and

$$\frac{(G_{ds1} + G_{ds2})\, G_{ds4}}{G_{ms4}} = \frac{G_o}{2}. \tag{2.11}$$

Choosing to bias M_{3a}-M_{3b} in weak inversion with $IC_3 = 0.1$, for $I_{b3} = 300\ nA$ we get $I_{spec3} = 3.00$ μA and $W_3/L_3 = 4.196$. We also have $G_{ms3} = 10.621\ \mu A/V$ and $G_{ds5} = 2.633\ nA/V$, we can derive $G_{ds3} = 126.712.\ nA$, which gives $L_3 = 194\ nm$, which is below the minimum length.

Choosing $L_3 = 2L_{min} = 360\ nm$ gives $W_3 = 1.15\ \mu m$.

To avoid having a too large transistor for M_{4a}-M_{4b}, we have chosen $IC_4 = 0.2$. We can split G_{op} half-half between $G_{ds1} + G_{ds2}$ and G_{ds4}, resulting in $G_{ds4} = 17.638\ nA/V$. $L_4 = 922\ nm$.

Spliting $G_{ds1} + G_{ds2}$ half-half between G_{ds1} and G_{ds2} leads to $G_{ds1} = 8.819\ nA/V$ and $G_{ds2} = 8.819$ nA/V. The length for M_{1a}-M_{1b} and M_{2a}-M_{2b} are then $L_1 = 1.49\ \mu m$ and $L_2 = 3.19\ \mu m$.

2.1.2 Transistor information

The transistor sizes and large-signal variables are summarized in Table 2.5, whereas Table 2.6 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

Table 2.5: Transistor size and bias information.

Transistor	W $[\mu m]$	L $[\mu m]$	I_D $[nA]$	I_{spec} $[nA]$	IC	$V_G - V_{T0}$ $[mV]$	V_{DSsat} $[mV]$
M1a	4.92	1.49	250	2500	0.100	-45	105
M1b	4.92	1.49	250	2500	0.100	-45	105
M2a	0.94	3.19	550	55	10.000	127	194
M2b	0.94	3.19	550	55	10.000	127	194
M3a	1.15	0.36	300	3000	0.100	-45	105
M3b	1.15	0.36	300	3000	0.100	-45	105
M4a	7.31	0.92	300	1500	0.200	-28	106
M4b	7.31	0.92	300	1500	0.200	-28	106
M5a	0.20	5.77	300	30	10.000	130	194
M5b	0.20	5.77	300	30	10.000	130	194
M5c	0.20	5.77	300	30	10.000	130	194
M6a	0.20	0.90	500	53	9.409	122	190
M6b	0.20	0.90	500	53	9.409	122	190
M7a	0.20	3.49	500	50	10.000	130	194
M7b	0.20	3.49	500	50	10.000	130	194
M7c	0.20	3.49	500	50	10.000	130	194
M7d	0.20	3.49	500	50	10.000	130	194
M9a	4.92	1.49	250	2500	0.100	-45	105
M9b	4.92	1.49	250	2500	0.100	-45	105
M9c	4.92	1.49	250	2500	0.100	-45	105
M9d	4.92	1.49	250	2500	0.100	-45	105

Table 2.6: Transistor small-signal and thermal noise parameters.

Transistor	n	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1a	1.271	96.618	8.851	6.962	8.370	0.653
M1b	1.271	96.618	8.851	6.962	8.370	0.653
M2a	1.306	2.126	5.742	4.397	8.620	0.812
M2b	1.306	2.126	5.742	4.397	8.620	0.812
M3a	1.271	115.942	10.621	8.354	41.667	0.653
M3b	1.271	115.942	10.621	8.354	41.667	0.653
M4a	1.306	57.971	9.903	7.582	16.261	0.685
M4b	1.306	57.971	9.903	7.582	16.261	0.685
M5a	1.271	1.159	3.132	2.464	2.599	0.790
M5b	1.271	1.159	3.132	2.464	2.599	0.790
M5c	1.271	1.159	3.132	2.464	2.599	0.790
M6a	1.306	2.054	5.356	4.101	27.791	0.810
M6b	1.306	2.054	5.356	4.101	27.791	0.810
M7a	1.271	1.932	5.220	4.106	7.156	0.790
M7b	1.271	1.932	5.220	4.106	7.156	0.790
M7c	1.271	1.932	5.220	4.106	7.156	0.790
M7d	1.271	1.932	5.220	4.106	7.156	0.790
M9a	1.271	96.618	8.851	6.962	8.370	0.653

Table 2.6: Transistor small-signal and thermal noise parameters.

Transistor	n	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M9b	1.271	96.618	8.851	6.962	8.370	0.653
M9c	1.271	96.618	8.851	6.962	8.370	0.653
M9d	1.271	96.618	8.851	6.962	8.370	0.653

2.1.3 Simulations

2.1.3.1 Operating point

We first write the parameter file for this specific design for running the ngspice simulations. Before running the AC and NOISE simulations, we first need to check the quiescent voltages and currents and the operating points of all transistors by running a .OP simulation.

Table 2.7: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
vb2	0.9
vb3	0.9
inp	0.9
inn	0.9
outp	0.900024
outn	0.900024
ic	0.9
id	0
1	0.396674
2	1.43977
3	1.43977
4	0.377617
5	0.377617
6	0.680208
7	0.396385
8	0.396385
9	1.11034
10	1.09933
11	0.676095

We can extract the OTA quiescent node voltages from the ngspice .ic file. They are presented in Table 2.7. As expected, the simulated quiescent positive and negative output voltages are $V_{out+} = 0.900\ V$ and $V_{out-} = 0.900\ V$, which shows that the CMFB circuit operates properly.

The operating point information for all transistors are extracted from the ngspice .op file. The data is split into the large-signal operating informations in Table 2.8, the small-signal operating point informations in Table 2.9 and the noise operating point informations in Table 2.10.

Table 2.8: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC	n	V_{Dsat} $[mV]$
M1a	249	2291	0.109	1.27	121

Table 2.8: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC	n	V_{Dsat} $[mV]$
M1b	249	2291	0.109	1.27	121
M2a	549	49	11.203	1.31	277
M2b	549	49	11.203	1.31	277
M3a	299	2849	0.105	1.27	120
M3b	299	2849	0.105	1.27	120
M4a	299	1292	0.232	1.31	128
M4b	299	1292	0.232	1.31	128
M5a	300	27	11.005	1.27	275
M5b	299	27	10.999	1.27	275
M5c	299	27	10.999	1.27	275
M6a	498	48	10.566	1.31	272
M6b	499	48	10.567	1.31	272
M7a	500	45	11.044	1.27	275
M7b	498	45	11.036	1.27	275
M7c	498	45	11.036	1.27	275
M7d	498	45	11.036	1.27	275
M9a	249	2283	0.109	1.27	121
M9b	249	2283	0.109	1.27	121
M9c	249	2283	0.109	1.27	121
M9d	249	2283	0.109	1.27	121

Table 2.9: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	G_m $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_{ds} $[nA/V]$
M1a	7.045	8.747	7.218
M1b	7.045	8.747	7.218
M2a	4.023	5.415	6.218
M2b	4.023	5.415	6.218
M3a	8.486	10.475	58.296
M3b	8.486	10.475	58.296
M4a	7.559	9.685	11.417
M4b	7.559	9.685	11.417
M5a	2.295	2.955	1.616
M5b	2.290	2.950	2.798
M5c	2.290	2.950	2.798
M6a	3.775	5.078	13.482
M6b	3.776	5.080	13.420
M7a	3.813	4.909	4.460
M7b	3.801	4.896	6.943
M7c	3.801	4.896	6.948
M7d	3.801	4.896	6.948
M9a	7.043	8.747	8.493
M9b	7.041	8.744	8.438
M9c	7.041	8.744	8.438
M9d	7.043	8.747	8.493

Table 2.10: Noise operating point information extracted from ngspice .op file for each transistor.

Transistor	R_n [$k\Omega$]	$\sqrt{S_{ID,th}}$ [$nA/\sqrt{Hz}$]	γ_n [-]	$\sqrt{S_{ID,fl}}$ at 1Hz [$nA/\sqrt{Hz}$]
M1a	91.647	38.976	0.646	11.685
M1b	91.647	38.976	0.646	11.685
M2a	213.028	59.424	0.857	50.738
M2b	213.028	59.424	0.857	50.738
M3a	76.106	35.518	0.646	53.248
M3b	76.106	35.518	0.646	53.248
M4a	90.174	38.662	0.682	35.745
M4b	90.174	38.662	0.682	35.745
M5a	359.787	77.226	0.826	26.525
M5b	360.692	77.323	0.826	26.525
M5c	360.692	77.323	0.826	26.525
M6a	227.050	61.348	0.857	194.776
M6b	226.985	61.339	0.857	194.776
M7a	217.235	60.008	0.828	34.255
M7b	218.026	60.117	0.829	34.255
M7c	218.027	60.117	0.829	34.255
M7d	218.027	60.117	0.829	34.255
M9a	91.692	38.986	0.646	11.685
M9b	91.714	38.990	0.646	11.685
M9c	91.714	38.990	0.646	11.685
M9d	91.692	38.986	0.646	11.685

2.1.3.2 Large-signal differential transfer characteristic

We now simulate the DC differential transfer characteristic. The simulation of the large-signal input-output characteristic is presented in Figure 2.3.

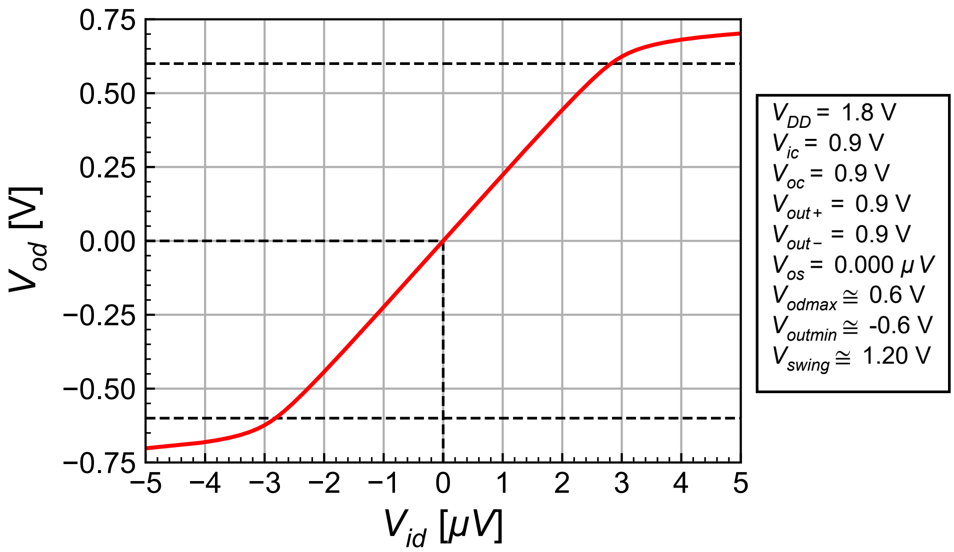

Figure 2.3: Simulated large-signal input-output characteristic.

Contrary to the single-ended folded-cascode OTA, in this fully-differential version there is no systematic offset introduced by the different V_{DS} voltages at the nMOS current mirror. So we don't need to add an offset voltage at the input to bring the output to the desired quiescent voltage (typically at $V_{DD}/2$) in the high gain region.

2.1.3.3 Open-loop transfer function

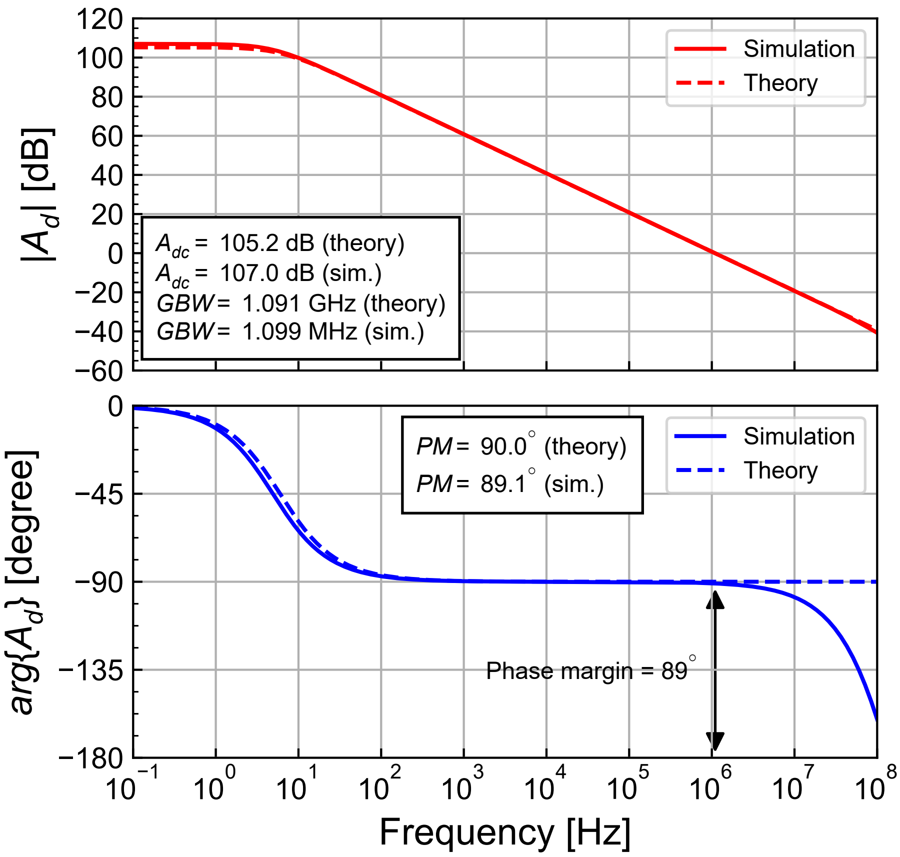

Figure 2.4: Simulated gain response compared to theoretical estimation.

From Figure 2.4, we see that the simulated transfer function is very close to the theoretical estimation below the GBW. The simulated gain-bandwidth product $GBW = 1.099\ MHz$ is equal to the theoretical estimation 1.091 MHz and slightly above target 1.000 MHz. The simulated DC gain $A_{dc} = 107.018\ dB$ is slightly higher than the estimated DC gain 105.237 dB and higher than the specifications 100 dB, offering some margin. Notice that he DC gain obtained from the AC simulation is consistent with the value extracted above from the DC transfer characteristic.

We also see that the non-dominant pole lays way above the GBW. This is simply because it is given by

$$\omega_p \cong \frac{G_2}{C_2}, \tag{2.12}$$

where G_2 is the conductance at node 2

$$G_2 \cong G_{ms4} + G_{ds1} + G_{ds2} \tag{2.13}$$

and C_2 the total parasitic capacitance at node 2

$$C_2 \cong C_{GD1} + C_{BD1} + C_{GD2} + C_{BD2} + C_{GS3} + C_{BS3}. \tag{2.14}$$

This gives $G_2 \cong 9.920\ \mu A/V$ and $C_2 \cong 29\ fF$ resulting in $f_p = 54.779\ MHz$ which is close to the value extracted from simulation 59.920 MHz.

2.1.4 Power consumption

The price to pay for this fully-differential implementaion is the additional power consumption used in the CMFB circuit which adds 1 μA of current consumption to the 1.1 μA used in the main OTA (not counting the additional current drawn by M_{5a} and M_{7a}). So almost doubling the power consumption.