Fundamentals of Analog VLSI Design
Exercise 7 - Solution

Gain and Bandwidth Enhancement

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1 Problem 1: Gain Enhancement

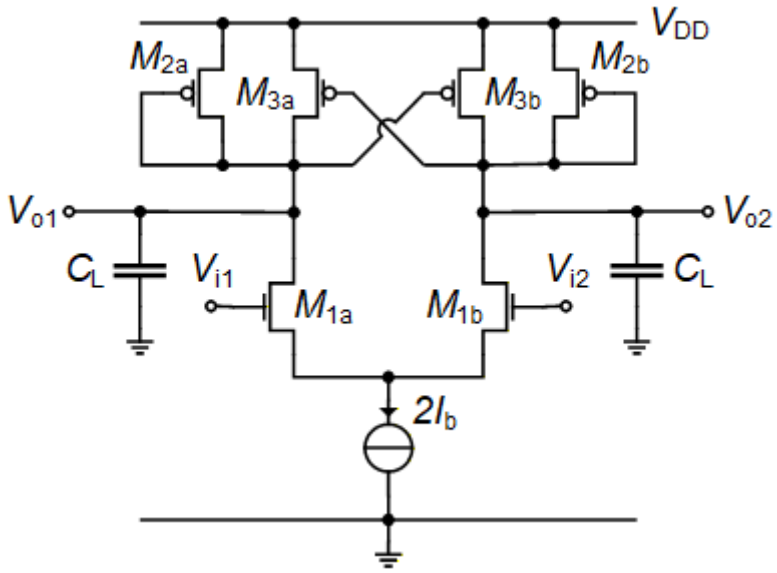

Figure 1.1: Schematic of gain enhancement amplifier.

The amplifier shown in Figure 1.1 allows to enhance the DC gain by reducing the load conductance seen by the differential pair M_{1a}-M_{1b} [1] [2].

1.1 Small-signal analysis

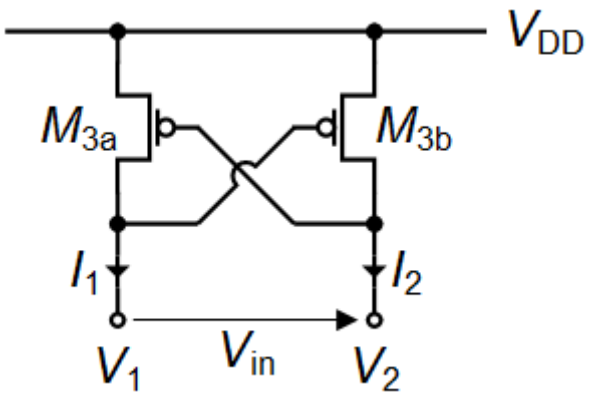

Figure 1.2: Negative conductance.

The cross-coupled transistors M_{3a}-M_{3b} which are redrawn in Figure 1.2, allow to implement a negative conductance. When combined with transistors M_{2a}-M_{2b}, they allow to reduce the conductance seen by the differential pair M_{1a}-M_{1b}.

The small-signal circuit corresponding to Figure 1.2 is shown in Figure 1.3.

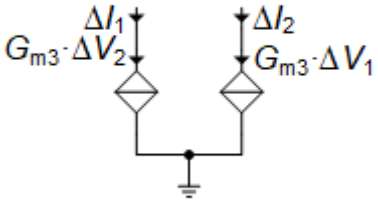

Figure 1.3: Small-signal circuit of Figure 1.2.

With $\Delta I_{in} \triangleq \Delta I_1 - \Delta I_2$ and $V_{in} \triangleq V_1 - V_2$ is then straightforward to show that

$$G \triangleq \frac{\Delta I_{in}}{\Delta V_{in}} = -G_{m3}. \tag{1.1}$$

The circuit of Figure 1.2 therefore implements a negative conductance equal to the transconductance of M_{3a}-M_{3b}.

> **Note**
>
> Note that the circuit of Figure 1.1 is used in regenerative comparators [3] [4] [5]. It is also used in oscillators to compensate the losses in the oscillator in order to sustain the oscillations.

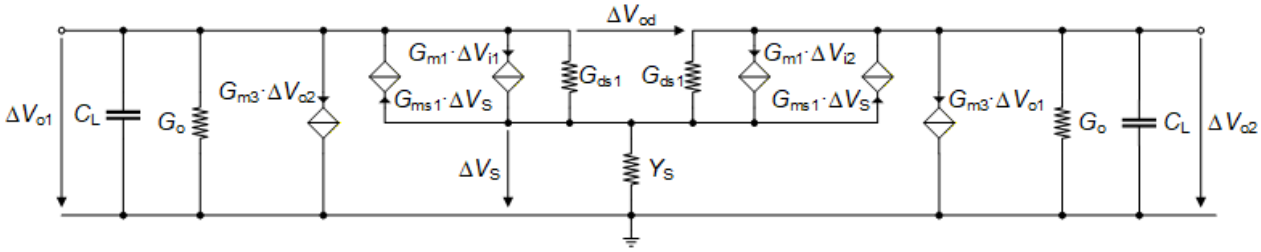

Figure 1.4: Small-signal circuit of Figure 1.2 in differential mode.

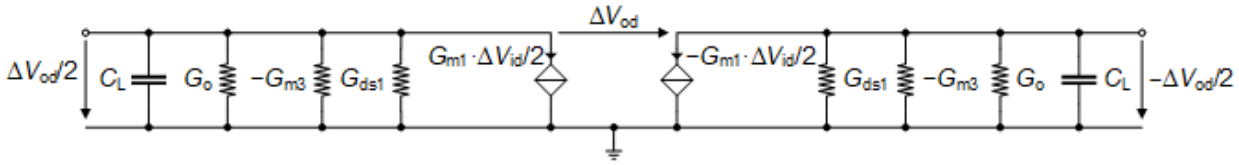

Figure 1.5: Small-signal circuit of Figure 1.2 in differential mode.

The small-signal circuit of Figure 1.1 is shown in Figure 1.4, where G_o is the total conductance at the output node given by

$$G_o = G_{m2} + G_{ds2} + G_{ds3} \cong G_{m2}. \tag{1.2}$$

In differential operation we have

$$\Delta V_{i1} = \frac{\Delta V_{id}}{2}, \tag{1.3}$$

$$\Delta V_{i2} = -\frac{\Delta V_{id}}{2}, \tag{1.4}$$

where ΔV_{id} is the small-signal differential input voltage. If we assume a perfect matching between the transistors in left and right branches, then $\Delta V_S = 0$ and the small-signal circuit of Figure 1.4 simplifies

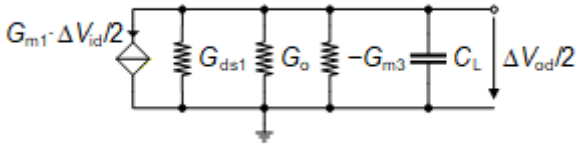

Figure 1.6: Small-signal circuit of Figure 1.2 in differential mode.

to the one shown in Figure 1.5. We can then use the half-circuit shown in Figure 1.6 to calculate the small-signal differential transfer function. It is easy to show that the differential transfer function is given by

$$A_d(s) \triangleq \frac{\Delta V_{od}}{\Delta V_{id}} = \frac{A_{dc}}{1+\frac{s}{\omega_p}}, \tag{1.5}$$

where

$$A_{dc} = -\frac{G_{m1}}{G_{od}-G_{m3}} = -\frac{G_{m1}}{G_{m2}+G_{ds1}+G_{ds2}+G_{ds3}-G_{m3}}, \tag{1.6}$$

$$\omega_p = \frac{G_{od}-G_{m3}}{C_L} = \frac{G_{m2}+G_{ds1}+G_{ds2}+G_{ds3}-G_{m3}}{C_L}, \tag{1.7}$$

with

$$G_{od} = G_o + G_{ds1} = G_{m2} + G_{ds1} + G_{ds2} + G_{ds3}. \tag{1.8}$$

The gain-bandwidth product or unity gain frequency ω_u is then simply given by

$$\omega_u \triangleq |A_{dc}| \cdot \omega_p = \frac{G_{m1}}{C_L}. \tag{1.9}$$

Contrary to the DC gain, the gain-bandwidth product is not increased and is the same as the amplifier without M_{3a}-M_{3b}.

From the expression of the pole ω_p, we see that for it to be located in the left half-plane, we need $G_{m3} < G_{od} = G_{m2} + G_{ds1} + G_{ds1} + G_{ds3}$.

We can rewrite the DC gain as

$$A_{dc} = -\frac{G_{m1}}{G_{m2}} \cdot K, \tag{1.10}$$

where K is the DC gain enhancement factor compared to the circuit without the cross-coupled pair M_{3a}-M_{3b} given by

$$K = \frac{1}{\frac{G_{od}}{G_{m2}} - \frac{G_{m3}}{G_{m2}}} = \frac{1}{1+\frac{G_{ds1}}{G_{m2}}+\frac{G_{ds2}}{G_{m2}}+\frac{G_{ds3}}{G_{m2}}-\frac{G_{m3}}{G_{m2}}}. \tag{1.11}$$

If we set $G_{m3} = G_{m2}$, the gain-enhancement factor becomes

$$K = \frac{G_{m2}}{G_{ds1}+G_{ds1}+G_{ds3}}, \tag{1.12}$$

which seems large. But looking at the DC gain, it reduces to

$$A_{dc} = -\frac{G_{m1}}{G_{ds1}+G_{ds2}+G_{ds3}}. \tag{1.13}$$

We see that it is basically the gain of a common-source stage loaded by an active load (current source). So we have indeed increased the gain compared to G_{m1}/G_{m2}, but we don't really improve the DC gain compared to a simple CS stage. We could have achieved the same gain with replacing the diode-connected transistors M_{2a}-M_{2b} with current sources.

To really boost the gain we need to compensate for more than G_{m2} but making sure that $G_{m3} < G_{od}$ to avoid any instability. Because of variability and mismatch, it is however not easy to control G_{m3} such that it always remains smaller than G_{od} in presence of mismatch and instability.

1.2 Noise analysis

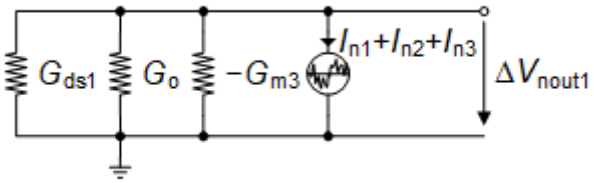

Figure 1.7: Small-signal half schematic of the amplifier of Figure 1.1 including all the noise sources.

The small-signal half schematic of the amplifier of Figure 1.1 including all the noise sources is shown in Figure 1.7. The output noise voltage is then simply given by

$$V_{nout1} = \frac{I_{n1} + I_{n2} - I_{n3}}{G_{od} - G_{m3}}. \tag{1.14}$$

The corresponding output noise resistance is then given by

$$R_{nout} = 2\,\frac{G_{n1} + G_{n2} + G_{n3}}{(G_{od} - G_{m3})^2}, \tag{1.15}$$

where

$$G_{ni} = \gamma_{ni}\,G_{mi} + G_{mi}^2\,\frac{\rho_i}{f\,W_i\,L_i} \quad \text{for } i = 1, 2, 3. \tag{1.16}$$

The noise can be referred to the input by dividing (1.15) by A_{dc}^2 resulting in

$$R_{nin} = \frac{R_{nout}}{A_d^2} = 2\,\frac{G_{n1} + G_{n2} + G_{n3}}{G_{m1}^2} = 2\frac{G_{n1}}{G_{m1}^2}\,(1 + \eta) \tag{1.17}$$

where

$$\eta = \frac{G_{n2}}{G_{n1}} + \frac{G_{n3}}{G_{n1}} \tag{1.18}$$

corresponds to the noise contributions of M_{2a}-M_{2b} and M_{3a}-M_{3b} relative to that of the differential pair M_{1a}-M_{1b}. If we have no gain enhancement (i.e. remove transistors M_{3a}-M_{3b}), the noise is increased by the contribution of M_{2a}-M_{2b} only. The cross-coupled pair M_{3a}-M_{3b} does not cancel the noise of M_{2a}-M_{2b} but simply adds some noise resulting in the additional term in G_{n3}/G_{n1} in η further degrading the input-referred noise.

We can now have a closer look at the input-referred thermal noise resistance.

1.2.1 Input-referred thermal noise resistance

The input-referred thermal noise resistance R_{nt} is given by

$$R_{nt} = 2\,\frac{\gamma_{n1}}{G_{m1}}\,(1 + \eta_{th}), \tag{1.19}$$

where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}}\,\frac{G_{m2}}{G_{m1}} + \frac{\gamma_{n3}}{\gamma_{n1}}\,\frac{G_{m3}}{G_{m1}}, \tag{1.20}$$

represents the contributions of M_{2a}-M_{2b} and M_{3a}-M_{3b} to the input-referred thermal noise relative to that of M_{1a}-M_{1b}. If we set $G_{m3} = G_{m2}$, the contribution of M_{3a}-M_{3b} is then equal to that of M_{2a}-M_{2b}. The value of η_{th} is then twice that of of the circuit without M_{3a}-M_{3b}. Note that G_{m1}/G_{m2} represents the voltage gain without M_{3a}-M_{3b}, the contributions of M_{2a}-M_{2b} and M_{3a}-M_{3b} should remain reasonable.

1.2.2 Input-referred flicker noise resistance

The input-referred flicker noise resistance R_{nf} is given by

$$R_{nf} = 2\,\frac{\rho_n}{f\,W_1\,L_1}\,(1+\eta_{fl}), \tag{1.21}$$

where

$$\eta_{fl} = \frac{\rho_p}{\rho_n}\,\left(\frac{G_{m2}}{G_{m1}}\right)^2\,\frac{W_1\,L_1}{W_2\,L_2} + \frac{\rho_p}{\rho_n}\,\left(\frac{G_{m3}}{G_{m1}}\right)^2\,\frac{W_1\,L_1}{W_3\,L_3}, \tag{1.22}$$

represents the contributions of M_{2a}-M_{2b} and M_{3a}-M_{3b} to the input-referred flicker noise relative to that of M_{1a}-M_{1b}. For the same reasons as discussed above, the contributions of M_{2a}-M_{2b} and M_{3a}-M_{3b} should remain small thanks to the square of the G_m ratios. They can be further reduced by making the gate area of M_{2a}-M_{2b} and M_{3a}-M_{3b} larger than that of M_{1a}-M_{1b}.

1.3 Conclusion

Adding the cross-coupled pair M_{3a}-M_{3b} seems very attractive to boost the DC gain. However, if we set $G_{m3} = G_{m2}$, we have seen that the gain is indeed increased but only to that of a simple CS stage. The same gain would be easier to reach with replacing the diode-connected transistors M_{2a}-M_{2b} by simple current source. In addition, the cross-coupled pair M_{3a}-M_{3b}, although canceling part of the output conductance G_{od}, adds more noise than what we get from a simple CS stage.

2 Problem 2: Bandwidth enhancement

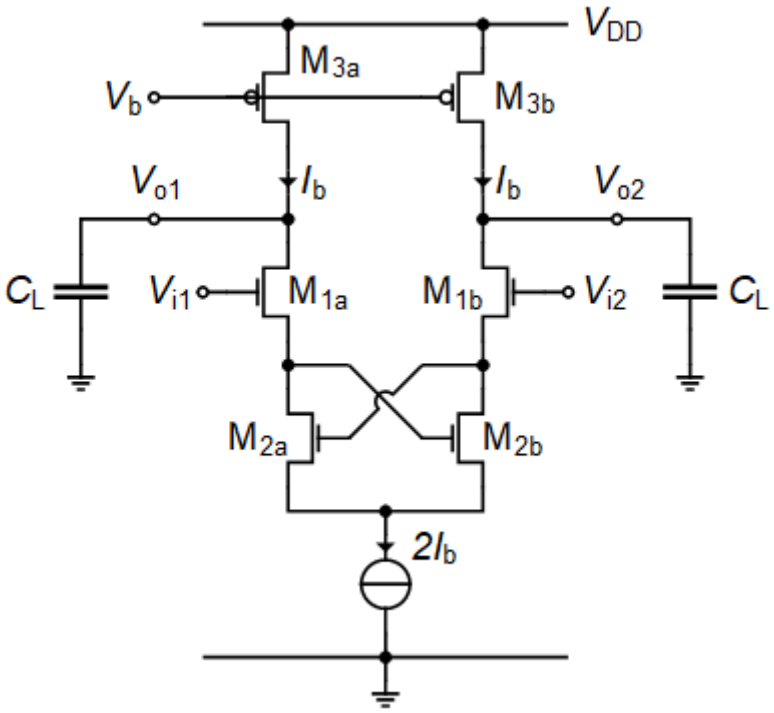

Figure 2.1: Enhanced G_m differential OTA [1] [6]

The fully differential OTA shown in Figure 2.1 shows a larger gain-bandwidth product compared to the case without the cross-coupled transistors M_{2a}-M_{2b} [1] [6].

2.1 Small-signal analysis

The OTA of Figure 2.1 uses the differential transconductor shown in Figure 2.2 which allows to increase the equivalent transconductance compared to the case of a simple differential pair.

In small-signal differential operation (i.e. $V_{i1} = \Delta V_{id}/2$ and $V_{i2} = -\Delta V_{id}/2$), assuming that transistors M_{1a}-M_{1b} and M_{2a}-M_{2b} are perfectly matched, the common source voltage of M_{2a}-M_{2b} does not change $\Delta V_{S2} = 0$ and can be considered as an AC ground. By symmetry we also can state that $\Delta V_{G2a} = \Delta V_{D2b} = -\Delta V_{D2a}$. The VCCS modeling M_{2a} is therefore controlled by its drain voltage ΔV_{D2a} which is equal to $-\Delta V_{G2a}$. This means that the VCCS can be replaced by a negative conductance $-G_{m2}$. The small-signal circuit then simplifies to the half-circuit shown in Figure 2.3

From the circuit shown in Figure 2.3, it is easy to derive the equivalent transconductance G_{meq} as [6] [7]

$$G_{meq} \triangleq \frac{\Delta I_{od}}{\Delta V_{id}} = \frac{G_{m1}\,(G_{ds2} - G_{m2})}{G_{ms1} + G_{ds1} + G_{ds2} - G_{m2}}. \tag{2.1}$$

We see that setting $G_{m2} = G_{ms1} + G_{ds1} + G_{ds2} \cong G_{ms1}$ gives an infinite transconductance G_{meq}. We can now distinguish two cases $G_{m2} < G_{ms1}$ or $G_{m2} > G_{ms1}$. To investigate whether both choices are

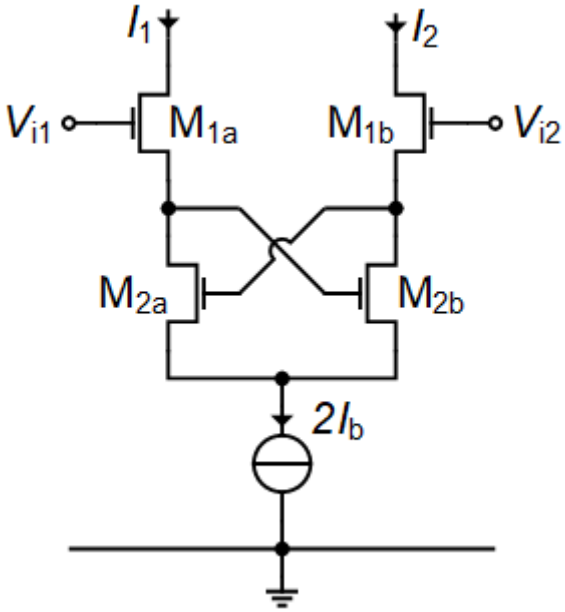

Figure 2.2: Enhanced G_m differential transconductor

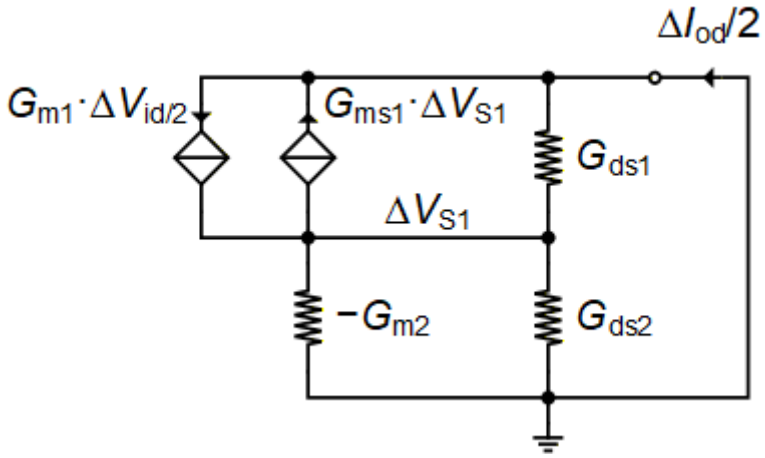

Figure 2.3: Small-signal circuit of the transconductor of Figure 2.2 in differential mode assuming that transistors M_{1a}-M_{1b} and M_{2a}-M_{2b} are perfectly matched.

possible, we need to have a closer look at the small-signal circuit including the parasitic capacitance C_p at the sources of M_{1a}-M_{1b}. The latter is equal to the parasitic capacitances of M_{2a}-M_{2b}

$$C_p \cong C_{GS2} + 4\,C_{GD2}. \tag{2.2}$$

The factor 4 comes from splitting the $2\,C_{GD2}$ capacitances in two capacitances of value $4\,C_{GD2}$ which are connected in series with the middle point connected to ground. They therefore come in parallel to C_{GS2} on each side.

To derive the transadmittance we can use the half-circuit shown in Figure 2.4.

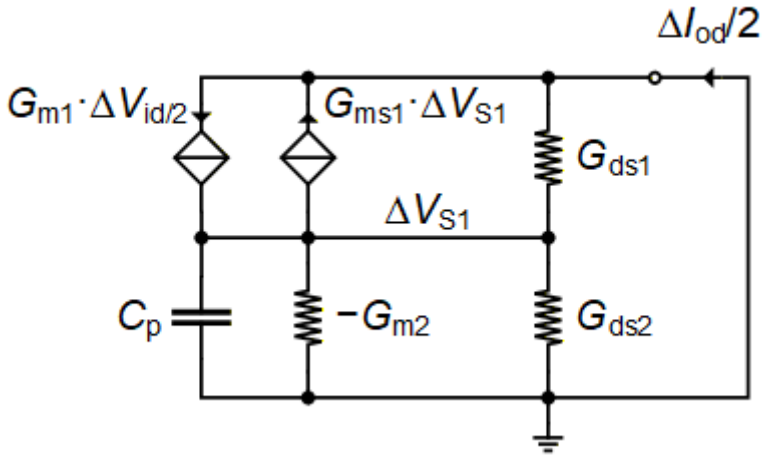

Figure 2.4: Half small-signal circuit in differential mode including parasitic capacitance C_p.

The resulting transadmittance is then given by

$$Y_{meq} = G_{meq}\,\frac{1 - s/\omega_z}{1 + s/\omega_p}, \tag{2.3}$$

where

$$G_{meq} = \frac{G_{m1}\,(G_{ds2} - G_{m2})}{G_{ms1} + G_{ds1} + G_{ds2} - G_{m2}} \cong -\frac{G_{m1}\,G_{m2}}{G_{ms1} - G_{m2}}, \tag{2.4}$$

$$\omega_z = \frac{G_{m2} - G_{ds2}}{C_p} \cong \frac{G_{m2}}{C_p}, \tag{2.5}$$

$$\omega_p = \frac{G_{ms1} + G_{ds1} + G_{ds2} - G_{m2}}{C_p} \cong \frac{G_{ms1} - G_{m2}}{C_p}, \tag{2.6}$$

$$C_p = C_{GS2} + 4\,C_{GD2}. \tag{2.7}$$

From the expression of the pole ω_p, we can deduce that for the pole to be in the left half-plane requires $G_{ms1} > G_{m2}$. We can then rewrite

$$G_{meq} \cong -\frac{G_{m1}}{G_{ms1}/G_{m2} - 1} = -\frac{G_{m1}}{\alpha - 1}, \tag{2.8}$$

$$\omega_z \cong \frac{G_{m2}}{C_p}, \tag{2.9}$$

$$\omega_p \cong \frac{G_{m2}}{C_p}\left(1 - \frac{G_{ms1}}{G_{m2}}\right) = \frac{G_{m2}}{C_p}\,(\alpha - 1), \tag{2.10}$$

where

$$\alpha \triangleq \frac{G_{ms1}}{G_{m2}} > 1 \tag{2.11}$$

Notice that the equivalent transconductance G_{meq} becomes negative for $\alpha > 1$.

The equivalent transconductance of a differential pair is therefore increased by a factor K given by

$$K = \frac{1}{\alpha - 1}. \tag{2.12}$$

To achieve a transconductance increase of K, the transconductance ratio $\alpha = G_{ms1}/G_{m2}$ needs to be equal to $1 + 1/K$.

If transistors M_{1a}-M_{1b} and M_{2a}-M_{2b} are all biased in strong inversion then

$$G_{ms1} = \sqrt{2\, n_1\, \beta_1\, I_{D1}}, \tag{2.13}$$

$$G_{m2} = \sqrt{\frac{2\, \beta_2\, I_{D2}}{n_2}}. \tag{2.14}$$

Since M_{1a}-M_{1b} and M_{2a}-M_{2b} share the same current $I_{D1} = I_{D2} = I_b$ and the transconductance ratio is then given by

$$\alpha = \frac{G_{ms1}}{G_{m2}} = \sqrt{\frac{n_1\, n_2\, \beta_1}{\beta_2}}, \tag{2.15}$$

which only depends on the β_1/β_2 ratio.

Choosing $\beta_1 = \beta_2$ leads to $\alpha = 1.30$ and a transconductance increase $K = 3.333$ for $n_1 = n_2 = 1.30$.

To minimize the V_{GS} voltages of M_{1a}-M_{1b} and M_{2a}-M_{2b} and better control the transconductance ratio $\alpha = G_{ms1}/G_{m2}$ by a current ratio, we should bias them in weak inversion [6]. In this case the transconductances are given by

$$G_{ms1} = \frac{I_{D1}}{U_T}, \tag{2.16}$$

$$G_{m2} = \frac{I_{D2}}{n_2\, UT}. \tag{2.17}$$

The transconductance ratio is then proportional to the current ratio

$$\alpha = \frac{G_{ms1}}{G_{m2}} = n_2\, \frac{I_{D1}}{I_{D2}} \tag{2.18}$$

The equivalent transconductance then writes

$$G_{meq} = \frac{G_{m1}}{n_2\, \frac{I_{D1}}{I_{D2}} - 1} = \frac{I_{D1}}{n_1\, U_T}\, \frac{1}{n_2\, \frac{I_{D1}}{I_{D2}} - 1}. \tag{2.19}$$

Note that I_{D1} is actually half the total bias current.

If M_{1a}-M_{1b} and M_{2a}-M_{2b} share the same bias current I_b as it is the case in the circuit of Figure 2.2 then $I_{D1} = I_{D2} = I_b$ and $\alpha = n_2 > 1$ which is larger than 1. For $n_2 = 1.30$, we get $K = 3.333$.

We can compare the equivalent transconductance to the transconductance achieved in weak inversion by M_{1a}-M_{1b}

$$G_{mwi} = \frac{I_{D1}}{n_1\, U_T}, \tag{2.20}$$

by defining the ratio

$$\frac{G_{meq}}{G_{mwi}} = K = \frac{1}{n_2\, \frac{I_{D1}}{I_{D2}} - 1}. \tag{2.21}$$

The K-factor is plotted versus the current ratio I_{D1}/I_{D2} in Figure 2.5.

From (2.21) and Figure 2.5, we see that we only gain if the drain current ratio I_{D1}/I_{D2} is smaller than $2/n_2 = 1.538$. On the other hand, the condition $\alpha > 1$ requires I_{D1}/I_{D2} to be larger than $1/n_2 = 0.769$. The drain current ratio I_{D1}/I_{D2} needs therefore to satisfy the following inequalities

$$\frac{1}{n_2} < \frac{I_{D1}}{I_{D2}} < \frac{2}{n_2}, \tag{2.22}$$

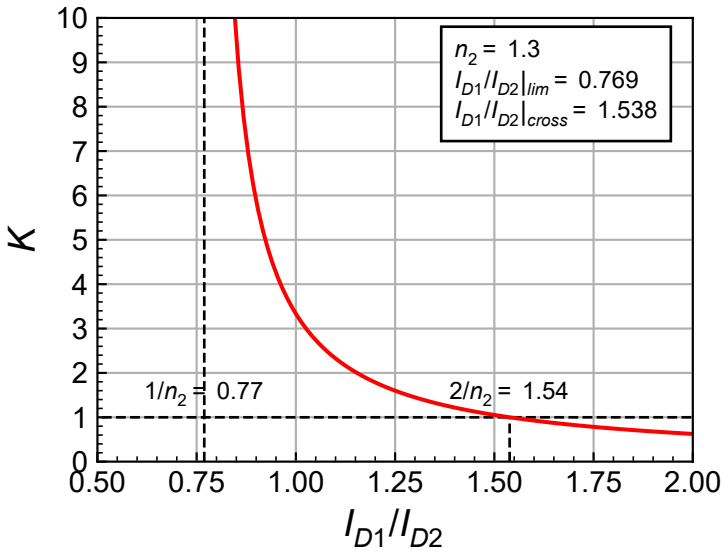

Figure 2.5: Equivalent transconductance compared to the transconductance in weak inversion with the same total current versus I_{D2}/I_{D1} ratio.

which for $n_2 = 1.300$ gives $0.769 < I_{D1}/I_{D2} < 1.538$. This actually leaves little margin. Choosing $I_{D1} = I_{D2}$ is a good choice because of its simple implementation (it does not require to add any bias current to increase the current in M_{1a}-M_{1b}).

The transfer function of the G_m-enhanced OTA of Figure 2.1 is given by

$$A_d \triangleq \frac{V_{od}}{V_{id}} \cong \frac{G_{meq}}{G_{ds3} + s\,C_L} = \frac{A_{dc}}{1 + \frac{s}{\omega_p}}. \tag{2.23}$$

with

$$A_{dc} \cong= K \cdot \frac{G_{m1}}{G_{ds3}}. \tag{2.24}$$

$$\tag{2.25}$$

The gain-bandwidth product is then given by

$$\omega_u = |A_{dc}|\,\omega_c \cong K \cdot \frac{G_{m1}}{C_L}. \tag{2.26}$$

We see that adding the cross-coupled pair M_{2a}-M_{2b} increases both the DC gain and the gain-bandwidth product by the factor K compared to the same circuit of Figure 2.1 but without the cross-coupled pair M_{2a}-M_{2b}.

We can rewrite the DC gain as

$$A_{dc} \cong -\frac{G_{m1}}{G_{ds3}} \frac{1}{1 + \frac{G_{ds1}}{G_{ds3}} - \frac{G_{ms1}}{G_{m2}}} \tag{2.27}$$

From (2.27), we see that in order to also increase the DC gain, we need to make G_{ms1}/G_{m2} sligthly larger than 1 but still smaller than $1 + G_{ds1}/G_{ds3}$ to avoid instability. Indeed if we set $G_{ms1}/G_{m2} = 1$ the DC gain becomes $-G_{m1}/G_{ds1}$ which corresponds to the gain of a simple common-source stage. We have compensated the output conductance of M_{3a}-M_{3b} but not that of M_{1a}-M_{1b}. To boost the DC gain we need

$$1 < \frac{G_{ms1}}{G_{m2}} < 1 + \frac{G_{ds1}}{G_{ds3}}. \tag{2.28}$$

It is however dangerous to set G_{ms1}/G_{m2} sligthly larger than 1, because we don't control the G_{ds1}/G_{ds3} very weel due to variability and mismatch.

To really take advantage of the G_m-enhancement also for the DC gain, the latter should be developped at another node than the drain of M_{1a}-M_{1b}. An example of such circuit is shown in Figure 2.7 which is close to the one proposed in [6].

2.2 Noise analysis

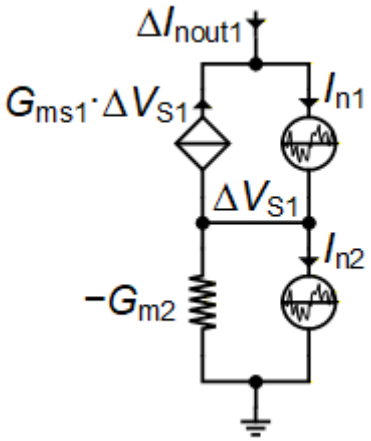

Figure 2.6: Small-signal schematic of the circuit of Figure 2.2

The small-signal schematic of Figure 2.2 including all the noise sources is shown in Figure 2.6. The output noise current I_{nout1} is given by

$$I_{nout1} = H_{n1} \cdot I_{n1} + H_{n2} \cdot I_{n2}, \tag{2.29}$$

with

$$H_{n1} = \frac{G_{m2}}{G_{m2} - G_{ms1}} = -\frac{1}{\alpha - 1}, \tag{2.30}$$

$$H_{n2} = \frac{G_{ms1}}{G_{ms1} - G_{m2}} = \frac{\alpha}{\alpha - 1}, \tag{2.31}$$

where $\alpha = G_{ms1}/G_{m2}$. The differential output noise current is simply $I_{nout} = 2\, I_{nout1}$ and the output noise conductance then writes

$$G_{nout} = 2\left(|H_{n1}|^2\, G_{n1} + |H_{n2}|^2\, G_{n2}\right), \tag{2.32}$$

with

$$G_{ni} = \gamma_{ni}\, G_{mi} + G_{mi}^2\, \frac{\rho_i}{f\, W_i\, L_i} \quad \text{for } i = 1, 2. \tag{2.33}$$

The input-referred noise resistance is then given by

$$R_{nin} = \frac{G_{nout}}{G_{meq}^2} = 2\frac{G_{n1}}{G_{m1}^2}\,(1 + \eta) \tag{2.34}$$

where

$$\eta = \left(\frac{G_{ms1}}{G_{m2}}\right)^2 \frac{G_{n2}}{G_{n1}} = \alpha^2\, \frac{G_{n2}}{G_{n1}} \tag{2.35}$$

corresponds to the noise contributions of M_{2a}-M_{2b} relative to that of the differential pair M_{1a}-M_{1b}. We see that the input-referred noise is degraded by M_{2a}-M_{2b}.

2.2.1 Input-referred thermal noise resistance

The input-referred thermal noise resistance R_{nt} is given by

$$R_{nt} = 2\,\frac{\gamma_{n1}}{G_{m1}}\,(1+\eta_{th}), \tag{2.36}$$

where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}}\,\frac{n_1\,G_{ms1}}{G_{m2}} = \frac{\gamma_{n2}}{\gamma_{n1}}\,n_1\,\alpha, \tag{2.37}$$

represents the contributions of M_{2a}-M_{2b} to the input-referred thermal noise relative to that of M_{1a}-M_{1b}. If both transistors M_{1a}-M_{1b} and M_{2a}-M_{2b} are biased in weak inversion then

$$\alpha = n_2\,\frac{I_{D1}}{I_{D2}} \tag{2.38}$$

and

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}}\,n_1\,n_2\,\frac{I_{D1}}{I_{D2}} \cong n_1\,n_2\,\frac{I_{D1}}{I_{D2}}, \tag{2.39}$$

In the case $I_{D1} = I_{d2} = I_b$ then

$$\eta_{th} \cong n_1\,n_2. \tag{2.40}$$

For $n_1 = n_2 = 1.30$, we get $\eta_{th} = 1.690$, which means that M_{2a}-M_{2b} contribute 1.690-times more than M_{1a}-M_{1b} to the input-referred thermal noise.

2.2.2 Input-referred flicker noise resistance

The input-referred flicker noise resistance R_{nf} is given by

$$R_{nf} = 2\,\frac{\rho_n}{f\,W_1\,L_1}\,(1+\eta_{fl}), \tag{2.41}$$

where

$$\eta_{fl} = n_1^2\,\frac{W_1\,L_1}{W_2\,L_2}, \tag{2.42}$$

represents the contributions of M_{2a}-M_{2b} to the input-referred flicker noise relative to that of M_{1a}-M_{1b}. We see that if M_{1a}-M_{1b} and M_{2a}-M_{2b} have the same gate area, their contribution to the input-referred flicker noise is about the same. For $n_1 = 1.30$ and $W_1\,L_1 = W_2\,L_2$, we get $\eta_{fl} = 1.690$, which means that M_{2a}-M_{2b} contributes 1.690 more than M_{1a}-M_{1b}. We can of course reduce this contribution by making $W_2\,L_2$ larger than $W_1\,L_1$.

The above analysis has shown that the G_m-enhanced OTA of Figure 2.1 can increase the gain-bandwidth product and eventually the DC gain compared to the same OTA without the cross-coupled pair M_{2a}-M_{2b}, but this comes at the cost of a higher noise.

2.3 Example

2.3.1 Design

We want to design the single-ended G_m-enhanced OTA shown in Figure 2.7 [6] for the specifications given in Table 2.1. The circuit of Figure 2.7 corresponds to a symmetrical OTA to which we have added the cross-coupled pair M_{2a}-M_{2b}. It is close to the original OTA proposed by Castello [6]. As explained above, this circuit takes advantage of the G_m-enhancement provided by the cross-coupled pair M_{2a}-M_{2b} to increase both the gain-bandwidth product and the DC gain. The reason is that the DC gain is realized at the output node instead of the drain of M_{1a}-M_{1b} like it is the case for the OTA of Figure 2.1.

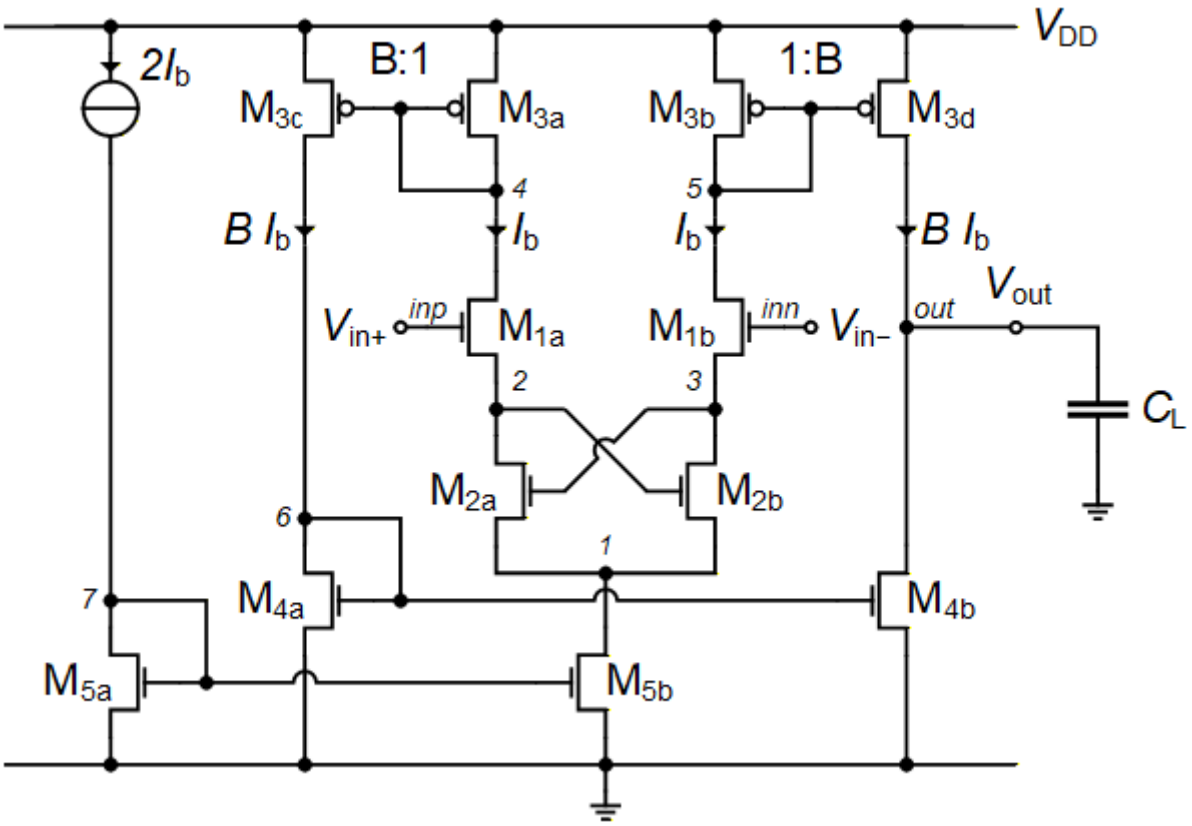

Figure 2.7: Single-ended version of the G_m-enhanced OTA [6]

We need to find the bias current and size the transistors to achieve the specs Table 2.1. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 2.2, the global process parameters in Table 2.3 and finally the MOSFET parameters in Table 2.4.

Table 2.1: Specifications for the differential pair with resistive loads.

Specification	Symbol	Value	Unit
Input common mode voltage	V_{ic}	1.2	V
DC gain	A_{dc}	80	dB
DC gain	A_{dc}	10000	-
Gain-bandwidth product	GBW	10	MHz
Load capacitance	C_L	1	pF

Table 2.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 2.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$

Table 2.3: Global process parameters

Parameter	Value	Unit
W_{min}	200	nm
L_{min}	180	nm

Table 2.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	20	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

The DC gain also benefits from the current gain B in the pMOS current mirrors. The equivalent transconductance is then given by

$$G_{meq} = B \cdot K \cdot G_{m1}. \tag{2.43}$$

where

$$K = \frac{1}{\alpha - 1} \tag{2.44}$$

with

$$\alpha = \frac{G_{ms1}}{G_{m2}} = n_2. \tag{2.45}$$

For the chosen technology this gives $\alpha = 1.271$ and $K = 3.685$.

The small-signal differential DC voltage gain is approximately given by

$$A_{dc} \cong -\frac{G_{meq}}{G_o} \tag{2.46}$$

with

$$G_o = G_{ds3d} + G_{ds4b}. \tag{2.47}$$

We additionnally set the current gain of the pMOS current mirrors to $B = 3$. With $K = 3.685$ we have a total G_m-enhancement factor $B \cdot K = 11.055$. From the specified gain-bandwidth product and the load capacitance we can deduce the transconductance of M_{1a}-M_{1b} $G_{m1} = 5.848\ \mu A/V$. Setting the inversion coefficient of M_{1a}-M_{1b} to $IC_1 = 0.1$, we get the bias current $I_b = 204\ nA$, which we slightly increase to $I_b = 210\ nA$ in order to have some margin. The differential pair bias current $2I_b = 420\ nA$.

> **Note**
>
> Note that if we want to achieve the same gain-bandwidth product $GBW = 10\ MHz$ without the cross-coupled pair and current gain, keeping the same inversion coefficient for M_{1a}-M_{1b}, we would need a bias current $I_b = 2.256\ \mu A$, which is 11.055 times larger than the bias current with the cross-coupled pair and the current gain.

We can now deduce the I_{spec} and W/L for M_{1a}-M_{1b} as $I_{spec1} = 2\ \mu A$ and $W_1/L_1 = 2.937$. Choosing $L_1 = L_{min} = 180\ nm$ we get and $W_1 = 0.71\ \mu m$.

The transconductance of M_{2a}-M_{2b} is $G_{m2} = G_{ms1}/\alpha = 5.848\ \mu A/V$. For a current $I_{D2} = I_b = 210\ nA$, we get $G_{m2}\, n_2\, U_T/I_{D2} = 0.916$ leading to $IC_2 = 0.100$. The specific current I_{spec} and W/L for M_{2a}-M_{2b} are given by $I_{spec2} = 2.100\ \mu A$ and $W_2/L_2 = 2.937$. Choosing $L_2 = L_{min} = 180\ nm$ we get and $W_2 = 0.34\ \mu m$.

For M_{3a} to M_{3d}, choosing $IC_3 = 10$, we get $I_{spec3} = 21\ nA$ and $W_3/L_3 = 0.121$. If we split G_o equally between M_{3d} and M_{4b} $G_{ds3d} = G_{ds4b}$, then $G_{ds3d} = 3.142\ nA/V$. This leads to $L_3 = 10.10\ \mu m$ and $W_3 = 1.16\ \mu m$.

Similarly for M_{4a}-M_{4b}, choosing $IC_4 = 10$, we get $I_{spec4} = 63\ nA$ and $W_4/L_4 = 0.088$. With $G_{ds4b} = 3.142\ nA/V$. This leads to $L_4 = 10.10\ \mu m$ and $W_4 = 0.83\ \mu m$.

This gives very big transistors for M_{3a} to M_{3d} and M_{4a}-M_{4b} that will add large parasitic capacitances at the mirror nodes and at the output penalizing the gain-bandwidth product and the phase margin. This is even more the case when accounting for the current gain $B = 3$ which makes the width of M_{3c}-M_{3d} 3-times larger than the width of M_{3a}-M_{3b}. In order to minimize the parasitic capacitances at the mirror nodes and at the output, we choose for M_{3a}-M_{3b} $W_3 = W_{min} = 200\ nm$, which leads to $L_3 = 2.17\ \mu m$. Note that the width of M_{3c}-M_{3d} is 3-times that of M_{3a}-M_{3b}.

Similarly for M_{4a}-M_{4b}, we choose $W_4 = W_{min} = 200\ nm$, which leads to $L_4 = 2.79\ \mu m$. This will obviously reduce the DC gain below the target value. The estimated DC gain is now only $A_{dc} \cong 67.45\ dB$. Simulations will show that this value is pessimistic and that we loose less DC gain, but still do not achieve the target value. Of course we could cascode the M_{3d} and M_{4b} to save the DC gain without penalty on the current consumption (except the additional bias circuit for biasing the cascode transistors).

Finally, choosing $IC_5 = 10$ for M_{5a}-M_{5b}, we get $I_{spec5} = 42\ nA$ and $W_5/L_5 = 0.059$. Choosing $W_5 = W_{min} = 200\ nm$, we get $L_5 = 4.14\ \mu m$.

2.3.2 Transistor information

The transistor sizes and large-signal variables are summarized in Table 2.5, whereas Table 2.6 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

Table 2.5: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1a	0.71	0.18	210	5169	0.041	-64	104
M1b	0.71	0.18	210	5169	0.041	-64	104
M2a	0.34	0.18	210	2636	0.080	-50	105
M2b	0.34	0.18	210	2636	0.080	-50	105
M3a	0.20	2.17	210	21	10.000	127	194
M3b	0.20	2.17	210	21	10.000	127	194
M3c	0.60	2.17	630	54	11.651	138	205
M3d	0.60	2.17	630	54	11.651	138	205
M4a	0.20	2.79	630	63	10.000	130	194
M4b	0.20	2.79	630	63	10.000	130	194
M5a	0.20	4.14	420	42	10.000	130	194
M5b	0.20	4.14	420	42	10.000	130	194

Table 2.6: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1a	199.777	7.811	6.143	58.333	0.644
M1b	199.777	7.811	6.143	58.333	0.644
M2a	101.884	7.556	5.943	58.333	0.650
M2b	101.884	7.556	5.943	58.333	0.650
M3a	0.812	2.193	1.679	4.847	0.812
M3b	0.812	2.193	1.679	4.847	0.812
M3c	2.090	6.164	4.720	14.542	0.816
M3d	2.090	6.164	4.720	14.542	0.816
M4a	2.435	6.578	5.174	11.296	0.790
M4b	2.435	6.578	5.174	11.296	0.790
M5a	1.623	4.385	3.449	5.067	0.790
M5b	1.623	4.385	3.449	5.067	0.790

2.3.3 Simulation

2.3.3.1 Operating point

We first write the parameter file for this specific design for running the ngspice simulations. Before running the AC and NOISE simulations, we first need to check the quiescent voltages and currents and the operating points of all transistors by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 2.7.

Table 2.7: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
inp	1.2
inn	1.2
id	0
ic	1.2
out	0.662637

Table 2.7: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
1	0.230944
2	0.683804
3	0.683804
4	1.1074
5	1.1074
6	0.662637
7	0.678442

From Table 2.7, we see that the ouput voltage is equal to $V_{outq} = 663\ mV$ for an input common mode voltage $V_{ic} = 1.2\ V$. We need to check wether this quiescent output voltage is in the high gain region for running the AC simulation. This is done below by looking at the large-signal transfer characteristic.

The operating point information for all transistors coming from the EKV2.6 compact model are extracted from the ngspice .op.dat file. The data is split into the large-signal operating informations presented in Table 2.8, the small-signal operating point informations shown in Table 2.9 and the noise operating point informations in Table 2.10.

Table 2.8: Large-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC [-]	n [-]	$V_{DSsat}\ [mV]$
M1a	206.9	5021.8	0.041	1.27	114
M1b	206.9	5021.8	0.041	1.27	114
M2a	206.9	2811.6	0.074	1.27	118
M2b	206.9	2811.6	0.074	1.27	118
M3a	206.9	18.7	11.110	1.31	276
M3b	206.9	18.7	11.110	1.31	276
M3c	535.4	48.3	11.120	1.31	276
M3d	535.4	48.3	11.120	1.31	276
M4a	535.4	57.5	9.347	1.27	262
M4b	535.4	57.5	9.347	1.27	262
M5a	420.0	38.2	11.024	1.27	275
M5b	413.8	38.0	11.013	1.27	275

Table 2.9: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$G_m\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_{ds}\ [nA/V]$
M1a	6.366	7.581	130.964
M1b	6.366	7.581	130.964
M2a	5.960	7.340	120.751
M2b	5.960	7.340	120.751
M3a	1.526	2.053	2.180
M3b	1.526	2.053	2.180
M3c	3.944	5.306	4.691
M3d	3.944	5.306	4.691
M4a	4.384	5.643	6.153
M4b	4.384	5.643	6.153
M5a	3.207	4.129	3.157
M5b	3.076	4.112	152.354

Table 2.10: Noise operating point information extracted from ngspice .op file for each transistor.

Transistor	R_n [$k\Omega$]	$\sqrt{S_{ID,th}}$ [$nA/\sqrt{Hz}$	γ_n [-]	$\sqrt{S_{ID,fl}}$ at 1Hz [$nA/\sqrt{Hz}$]
M1a	96.861	40.070	0.617	110866
M1b	96.861	40.070	0.617	110866
M2a	108.924	42.492	0.649	155855
M2b	108.924	42.492	0.649	155855
M3a	561.542	96.479	0.857	122362
M3b	561.542	96.479	0.857	122362
M3c	217.183	60.000	0.857	76256.2
M3d	217.183	60.000	0.857	76256.2
M4a	187.923	55.812	0.824	38419.7
M4b	187.923	55.812	0.824	38419.7
M5a	257.913	65.385	0.827	31396.5
M5b	281.811	68.347	0.867	31396.5

2.3.3.2 Large-signal differential transfer characteristic

We can now simulate the large-signal DC input-output transfer characteristic. The simulation result is presented in Figure 2.8.

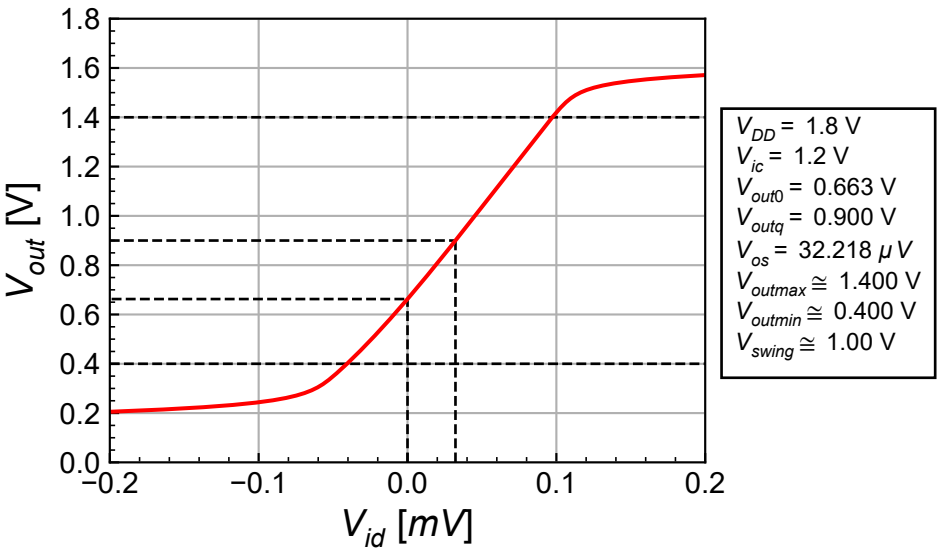

Figure 2.8: Simulated large-signal input-output characteristic.

We see from Figure 2.8 that the quiescent output voltage is in the linear region. We nevertheless can impose the extracted offset voltage $V_{os} = 32.2\ \mu V$ to center the output voltage at $V_{outq} = V_{DD}/2 = 0.9\ V$. We also see that the OTA offers a rather large output voltage swing $V_{swing} = 1.0\ V$.

2.3.3.3 Open-loop gain

After having checked the operating point information and making sure that the OTA output is not saturated and in the high gain region, we can now perform the AC simulation. The simulation results are compared to the theoretical estimations in Figure 2.9.

From Figure 2.9, we see that the simulated gain-bandwidth product is right on target and larger than the theoretical estimation. The simulated DC gain is slightly smaller than the specs, but larger than the theoretical estimation.

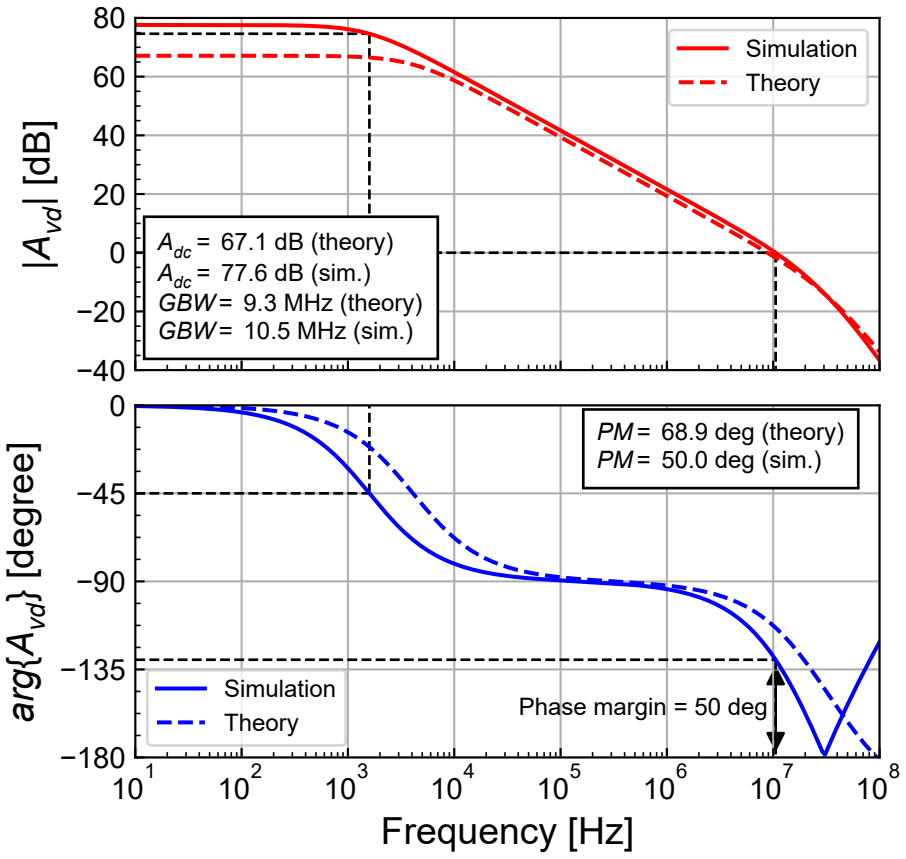

Figure 2.9: Simulated gain response compared to theoretical estimation.

2.4 Conclusion

The OTA of Figure 2.7 shows that the DC gain and gain-bandwidth product can both be increased without spending more current thanks to the cross-coupled pair M_{2a}-M_{2b} [6]. However, this achievement comes at the cost of a larger voltage required to bias the input transconductor M_{1a}-M_{1b} and M_{2a}-M_{2b}. Indeed, the minimum supply voltage is now increased by the V_{GS} voltage of M_{2a}-M_{2b} which is typically $V_{T0n} = 455\ mV$. In addition, the OTA of Figure 2.7 shows more noise because the cros-coupled pair contributes $n_1\, n_2$-times more than the differential pair. For $n_1 = n_2 = 1.27$ the cross-coupled pair contributes 1.62-times more than the differential pair, which is significant. We also have to remember that the G_m-enhancement is directly related to transconductance ratio $\alpha = G_{ms1}/G_{m2}$ which depend on the current ratio I_{D1}/I_{D2}. This current ratio might not be well controlled and subject to variability and mismatch. Note that taking $I_{D1} = I_{D2}$ would result in $\alpha \cong 1$ which could lead to instability.

3 Conclusion

In the exercise we have investigated two techniques to boost the gain and bandwidth of an OTA. They are both based on the use of a crsoss-coupled pair either at the drain for gain-enhancement or at the source for G_m-enhancement. Although these techniques look attarctive at first glance they don't really provide more performance compared to other techniques like simple cascode. Indeed cascode or its improved versions regulated cascode and gain-boosting turn out to be the simplest and most efficient gain-enhancement techniques [8] [9] [10].

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