Fundamentals of Analog VLSI Design
Exercise 6 - Solution

The Fully Differential G_m-R Gain Stage

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1 Introduction

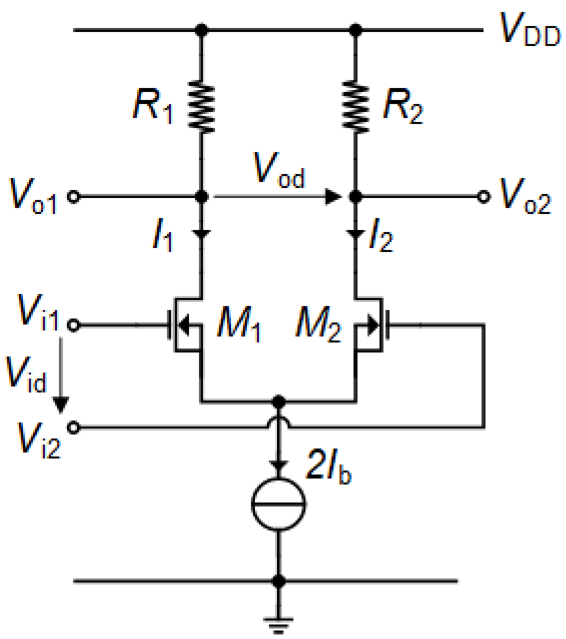

Figure 1.1: Schematic of the differential pair with resistive load.

Figure 1.1 shows a differential pair composed of two NMOS transistors M_1 and M_2, loaded with resistors R_1 and R_2, respectively. Since there are two input terminals, the output current or voltage depends on both the input voltages V_{i1} and V_{i2}. It is usually more interesting to express the output current or voltage in terms of the differential and common mode input voltages V_{id} and V_{ic} defined as

$$V_{id} \triangleq V_{i1} - V_{i2}$$
$$V_{ic} \triangleq \frac{V_{i1} + V_{i2}}{2}.$$

The differential mode and common mode operations are defined for $V_{ic} = const.$ and for $V_{id} = 0$, respectively. The input terminals are set to an appropriate common mode voltage V_{ic}, to which a differential voltage V_{id} is superimposed according to

$$V_{i1} = V_{ic} + \frac{V_{id}}{2}$$
$$V_{i2} = V_{ic} - \frac{V_{id}}{2}.$$

2 Small-signal analysis

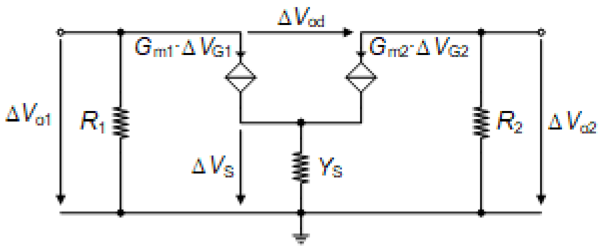

Figure 2.1: Small-signal schematic of the differential pair with resistive load.

Figure 2.1 shows the small-signal schematic of the differential pair of Figure 1.1, where Y_s corresponds to the admittance to ground at the common source node made of the output conductance of the bottom current source and the total capacitance between the common source node and ground.

If the transistors and resistances are perfectly matched, in small-signal operation (i.e. $G_{m1} = G_{m2} = G_m$ and $R_1 = R_2 = R$), an increase of the gate voltage of M_1 by $\Delta V_{id}/2$ combined with a decrease of the gate voltage of M_2 by the same amount keeps the common source node unchanged. This node can therefore be considered as a virtual AC ground (i.e. ΔV_S). The circuit then reduces to a common-source stage loaded by a resistance R which has a voltage gain $-G_m\,R$. The differential stage has therefore the same ideal differential voltage gain $A_{vd} = -G_m\,R$ as the common-source stage.

Of course we can find this results by solving the KCL equations of the equivalent small-signal circuit of Figure 2.1. Writing the KCL equation for the three nodes leads to

$$G_{m1}\,\Delta V_{G1} + \Delta V_{o1}/R_1 = 0, \tag{2.1}$$
$$G_{m2}\,\Delta V_{G2} + \Delta V_{o2}/R_2 = 0, \tag{2.2}$$
$$G_{m1}\,\Delta V_{G1} + G_{m2}\,\Delta V_{G2} = Y_s\,\Delta V_S. \tag{2.3}$$

Additionally, the incremental gate voltages are related to the input voltages according to

$$\Delta V_{G1} = \Delta V_{i1} - \Delta V_S, \tag{2.4}$$
$$\Delta V_{G2} = \Delta V_{i2} - \Delta V_S. \tag{2.5}$$

Solving together, we obtain the incremental output voltages as

$$\Delta V_{o1} = -G_{m1}\,R_1 \cdot \frac{(G_{m2} + Y_s)\,\Delta V_{i1} - G_{m2}\Delta V_{i2}}{G_{m1} + G_{m2} + Y_s}, \tag{2.6}$$
$$\Delta V_{o2} = -G_{m2}\,R_2 \cdot \frac{-G_{m1}\Delta V_{i1} + (G_{m1} + Y_s)\Delta V_{i2}}{G_{m1} + G_{m2} + Y_s}. \tag{2.7}$$

We now express the output voltages in terms of the differential and common mode voltages ΔV_{id} and ΔV_{ic} defined as

$$\Delta V_{id} \triangleq \Delta V_{i1} - \Delta V_{i2}, \tag{2.8}$$
$$\Delta V_{ic} \triangleq \frac{\Delta V_{i1} + \Delta V_{i2}}{2}, \tag{2.9}$$

such that

$$\Delta V_{i1} = \Delta V_{ic} + \frac{\Delta V_{id}}{2}, \tag{2.10}$$

$$\Delta V_{i2} = \Delta V_{ic} - \frac{\Delta V_{id}}{2}. \tag{2.11}$$

The differential mode of operation is then defined for $\Delta V_{ic} = 0$, whereas the common mode operation corresponds to $\Delta V_{id} = 0$.

The *differential voltage gain*, is then defined as

$$A_{vd} \triangleq \frac{\Delta V_{od}}{\Delta V_{id}} = \frac{\Delta V_{o1} - \Delta V_{o2}}{\Delta V_{id}} \tag{2.12}$$

and is obtained from (2.6) and (2.7) as

$$A_{vd} = -\frac{G_{m1}\, G_{m2}\, (R_1 + R_2) + (G_{m1} R_1 + G_{m2} R_2) Y_s/2}{G_{m1} + G_{m2} + Y_s}. \tag{2.13}$$

Assuming that the transistors and resistances are perfectly matched $G_{m1} = G_{m2} = G_m$ and $R_1 = R_2 = R$, the expression for the differential voltage gain simplifies to the expected result

$$A_{vd} = -G_m\, R. \tag{2.14}$$

One of the main feature of the differential pair is to reject the input common-mode voltage. In the case the transistors and resistances are perfectly matched, the common-mode to differential output voltage gain is ideally equal to zero because $\Delta V_{o1} = \Delta V_{o2}$. However, if there is a mismatch between the transistors or the resistances (or both), $\Delta V_{o1} \neq \Delta V_{o2}$ and therefore a differential output voltage is generated. The common-mode to differential voltage gain is given by

$$A_{vc} = Y_s \cdot \frac{G_{m2}\, R_2 - G_{m1}\, R_1}{G_{m1} + G_{m2} + Y_s} \tag{2.15}$$

From (2.15), we see that for a perfect matching (i.e. $G_{m1} = G_{m2}$ and $R_1 = R_2$) then $A_{vc} = 0$ since $G_{m1}\, R_1 = G_{m2}\, R_2 = G_m\, R$. Note that at low frequency, Y_s is equal to the output conductance G_{ds} of the bottom current source. The common-mode to differential voltage gain is proportional to G_{ds}. We can account for the mismatch by replacing

$$G_{m1} = G_m + \frac{\Delta G_m}{2}, \tag{2.16}$$

$$G_{m2} = G_m - \frac{\Delta G_m}{2}, \tag{2.17}$$

$$R_1 = R + \frac{\Delta R}{2}, \tag{2.18}$$

$$R_2 = R - \frac{\Delta R}{2}, \tag{2.19}$$

resulting in

$$A_{vc} = -G_{ds} \cdot \frac{G_m\, R}{G_{ds} + 2G_m} \cdot \left(\frac{\Delta G_m}{G_m} + \frac{\Delta R}{R}\right) \cong -\frac{G_{ds}\, R}{2} \left(\frac{\Delta G_m}{G_m} + \frac{\Delta R}{R}\right), \tag{2.20}$$

since $G_m \gg G_{ds}$.

The ability of the differential pair to reject the differential voltage is measured by the common-mode rejection ratio or CMRR defined as

$$CMRR \triangleq \frac{|A_{vd}|}{|A_{vc}|} \cong \frac{2G_m/G_{ds}}{\frac{\Delta G_m}{G_m} + \frac{\Delta R}{R}}. \tag{2.21}$$

From (2.21), we observe that the $CMRR$ is proportional to the transistor intrinsic gain (or self-gain) G_m/G_{ds}.

3 Noise analysis

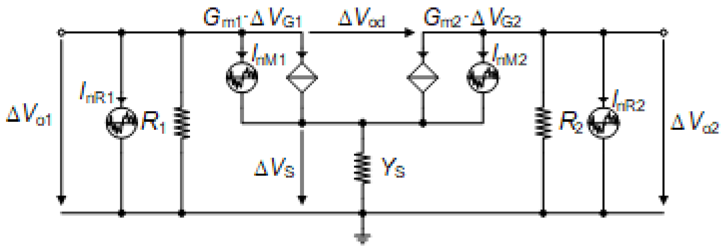

Figure 3.1: Small-signal schematic of the differential pair with resistive load including the noise sources.

The equivalent small-signal circuit of Figure 1.1 including all the noise sources is shown in Figure 3.1 where I_{nM1} and I_{nM2} represent the noise of M_1 and M_2, whereas I_{nR1} and I_{nR2} represent the thermal noise of R_1 and R_2. For noise analysis the inputs are connected to the dc common-mode input voltage V_{ic} so that $\Delta V_{i1} = \Delta V_{i2} = 0$ and $\Delta V_{G1} = \Delta V_{G2} = -\Delta V_S$. The output noise voltages are then simply given by

$$\Delta V_{no1} = -R \cdot (I_{nM1} + I_{nR1}), \tag{3.1}$$

$$\Delta V_{no2} = -R \cdot (I_{nM2} + I_{nR2}). \tag{3.2}$$

and the differential output noise voltage is given by

$$\Delta V_{nout} = -R \cdot (I_{nM1} + I_{nR1} - I_{nM2} - I_{nR2}). \tag{3.3}$$

The PSD of the differential output noise voltage is then simply given by

$$S_{nout} = R^2 \cdot (S_{I_{nM1}} + S_{I_{nR1}} + S_{I_{nM2}} + S_{I_{nR2}}) = 2R^2 \cdot (S_{I_{nM}} + S_{I_{nR}}). \tag{3.4}$$

which can also be written in terms of the output noise resistance R_{nout}

$$S_{nout} = 4kT\, R_{nout} \tag{3.5}$$

with

$$R_{nout} = R^2 \cdot 2(G_{nM} + G_{nR}). \tag{3.6}$$

The noise conductances G_{nM} and G_{nR} are given by

$$G_{nM} = \gamma_n\, G_m + \frac{\rho_n}{W\,L\,f}, \tag{3.7}$$

$$G_{nR} = \frac{1}{R}. \tag{3.8}$$

The input-referred noise resistance at low-frequency is then given by

$$R_{nin} = \frac{R_{nout}}{|A_{vd}|^2} = \frac{R_{nout}}{(G_m\, R)^2} = 2\frac{G_{nM} + G_{nR}}{G_m^2}. \tag{3.9}$$

The input-referred thermal noise resistance is then given by

$$R_{nin,th} = \frac{2\gamma_n}{G_m} \cdot (1 + \eta_{th}), \tag{3.10}$$

where η_{th} represents the contribution of the resistances relative to the contribution of the differential pair

$$\eta_{th} = \frac{1}{\gamma_n \, G_m \, R}. \tag{3.11}$$

From (3.11), we see that the larger the differential gain, the lower the contribution of the resistances to the input-referred thermal noise resistance, which is consistent with the intuition that the larger the gain of the first stage the lower the contribution of the following stages to the input-referred noise.

The input-referred flicker noise resistance is only due to the transistors since the resistances only generate thermal noise

$$R_{nin,fl}(f) = 2\frac{\rho_n}{W \, L \, f}. \tag{3.12}$$

If we include a capacitance C in parallel to the resistors R, the output thermal noise PSD is given by

$$S_{nout,th} = \frac{S_0}{1 + (\omega/\omega_c)^2}, \tag{3.13}$$

with

$$S_0 = 8kT \cdot R \cdot (\gamma_n \, G_m \, R + 1) \tag{3.14}$$

and $\omega_c = 1/(RC)$ is the cut-off frequency. The output noise is therefore a 1^{st}-order low-pass filtered white noise. The noise bandwidth is therefore given by

$$B_n = \frac{\omega_c}{4} = \frac{1}{4RC}, \tag{3.15}$$

The resulting variance of the output thermal noise voltage is then given by

$$V_{nout,th}^2 = \frac{2kT}{C} \cdot (\gamma_n \, G_m \, R + 1) = \frac{2kT \, \gamma_n \, G_m \, R}{C} + \frac{2kT}{C} \cong \frac{2kT}{C} \cdot \gamma_n \, G_m \, R \tag{3.16}$$

assuming that $G_m \, R \gg 1$. We see that the contribution of the resistance is simply $2kT/C$ because the noise level is proportional to R while the cut-off frequency is inversely proportional to R. The contribution of the differential pair depends on G_m because G_m sets the noise level but the cut-off frequency is set by R and does not depend on G_m.

The variance of the input-referred thermal noise voltage is then given by

$$V_{nin,th}^2 = \frac{V_{nout,th}^2}{(G_m \, R)^2} = \frac{2kT}{C \, G_m \, R} \left(\gamma_n + \frac{1}{G_m \, R}\right) \cong \frac{2\gamma_n kT}{C \, G_m \, R}. \tag{3.17}$$

From (3.17), we see that the variance of the input-referred thermal noise for $G_m \, R \gg 1$ is inversely proportional to the voltage gain $G_m \, R$ and proportional to the transistor thermal noise excess factor γ_n.

> **ℹ Note**
>
> Note that because the noise bandwidth is set by R and is independent of G_m, we can set independently the bandwidth with R, the DC gain with G_m and the thermal noise power with C.

4 Offset analysis

Because of the transistor and resistor mismatch, the output voltage is not equal to zero when the differential input voltage is zero. To calculate the offset voltage we can reuse the expression of the output noise voltage (3.3) obtained in the noise analysis and replace

$$I_{nM1} = +\frac{\Delta I_D}{2}, \tag{4.1}$$

$$I_{nM2} = -\frac{\Delta I_D}{2}, \tag{4.2}$$

$$I_{nR1} = +\frac{I_b}{R} \cdot \frac{\Delta R}{2}, \tag{4.3}$$

$$I_{nR2} = -\frac{I_b}{R} \cdot \frac{\Delta R}{2}. \tag{4.4}$$

The resulting differential output offset voltage is then given by

$$V_{os,out} = -R\, I_b \cdot \left(\frac{\Delta R}{R} + \frac{\Delta I_D}{I_b}\right) \tag{4.5}$$

The dc input-referred offset voltage is then given by

$$V_{os} = \frac{V_{os,out}}{-G_m\, R} = \frac{I_b}{G_m} \cdot \left(\frac{\Delta R}{R} + \frac{\Delta I_D}{I_b}\right). \tag{4.6}$$

The variance of the input-referred offset voltage is then given by

$$\sigma^2_{V_{os}} = \left(\frac{I_b}{G_m}\right)^2 \cdot (\sigma^2_{\Delta R/R} + \sigma^2_{\Delta I_D/I_D}). \tag{4.7}$$

The variance $\sigma^2_{\Delta I_D/I_D}$ depends on the transistor β- and V_T-mismatch according to

$$\sigma^2_{\Delta I_D/I_D} = \sigma^2_{\Delta\beta/\beta} + \left(\frac{G_m}{I_b}\right)^2 \cdot \sigma^2_{\Delta V_{T0}}, \tag{4.8}$$

resulting in

$$\sigma^2_{V_{os}} = \sigma^2_{\Delta V_{T0}} + \left(\frac{I_b}{G_m}\right)^2 \cdot \left(\sigma^2_{\Delta R/R} + \sigma^2_{\Delta\beta/\beta}\right) \tag{4.9}$$

The variances $\sigma^2_{\Delta V_{T0}}$ and $\sigma^2_{\Delta\beta/\beta}$ can be expressed in terms of the transistor area according to

$$\sigma^2_{\Delta V_{T0}} = \frac{A^2_{\Delta V_{T0}}}{W\, L}, \tag{4.10}$$

$$\sigma^2_{\Delta\beta/\beta} = \frac{A^2_{\beta}}{W\, L}. \tag{4.11}$$

From (4.9), we see that the contributions of the resistance mismatch and transistor β-mismatch to the input-referred offset voltage can be minimized by biasing the differential pair in weak inversion. The input-referred offset voltage then reduces to the transistor V_{T0} mismatch.

5 Common-mode input range analysis (CMIR) and differential-mode output range analysis (DMOR)

The minimum common-mode input voltage is limited by the saturation voltage of the bias current source

$$V_{ic,min} = V_{GS} + V_{DSsat,I_b}, \tag{5.1}$$

where V_{GS} is the gate-to-source voltage of M_1-M_2 and V_{DSsat,I_b} the saturation voltage of the bias current source.

The maximum common-mode input voltage is limited by the voltage drop across the load resistance and the differential pair transistors M_1-M_2 going out of saturation. Indeed, when increasing the common-mode input voltage the common-source node voltage follows reducing the V_{DS} voltage of M_1-M_2 until it becomes smaller than the saturation voltage V_{DSsat}. The maximum common-mode input voltage is therefore given by

$$V_{ic,max} = V_{GS} - V_{DSsat} - R\, I_b + V_{DD}, \tag{5.2}$$

where V_{GS} is the gate-to-source voltage of M_1-M_2 and V_{DSsat} its saturation voltage.

The maximum output voltage is simply equal to V_{DD}. One of the output voltage saturates to V_{DD} when the differential voltage is large enough for all the bias current to be steered into one side of the differential pair leaving no current flowing in the other branch making its voltage equal to V_{DD}.

The minimum output voltage corresponds to the same situation with all the current flowing into one branch. The voltage drop across the load resistor is then $R\, 2I_b$ leading to

$$V_{o,min} = V_{DD} - 2\, I_b\, R. \tag{5.3}$$

The output voltage swing at each output node V_{o1} and V_{o2} is then given by

$$\Delta V_{o,max} = V_{o,max} - V_{o,min} = 2\, I_b\, R \tag{5.4}$$

so that the voltage swing of the differential output voltage V_{od} is simply

$$\Delta V_{od,max} = 2\, \Delta V_{o,max} = 4\, I_b\, R. \tag{5.5}$$

6 Example

We want to size the circuit of Figure 1.1 for the specifications given in Table 6.1. We need to find the minimum current and size the transistor to achieve this specs. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 6.2, the global process parameters in Table 6.3 and finally the MOSFET parameters in Table 6.4.

Table 6.1: Specifications for the differential pair with resistive loads.

Specification	Symbol	Value	Unit
Input common mode voltage	V_{ic}	0.8	V
DC gain	A_{dc}	25	dB
DC gain	A_{dc}	18	-
Bandwidth	B	1	MHz
Input-referred thermal noise resistance	$R_{nin,th}$	10	$k\Omega$
Maximum input-referred offset voltage	V_{os}	2	mV

Table 6.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 6.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 6.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$

Table 6.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

6.1 Design

In order to minimize the input-referred offset voltage, the differential pair is biased in weak inversion with $IC = 0.1$. The differential pair transconductance is set by the specification on the input-referred thermal noise resistance according to

$$R_{nin,th} = \frac{2\gamma_n}{G_m} \cdot (1 + \eta_{th}), \tag{6.1}$$

with

$$\eta_{th} = \frac{1}{\gamma_n \, A_{dc}}. \tag{6.2}$$

The transconductance is then given by

$$G_m = \frac{2\gamma_n}{R_{nin,th}} \cdot (1 + \eta_{th}). \tag{6.3}$$

The DC gain is given by the spec, but we need the thermal noise excess factor γ_n to compute η_{th}. Knowing IC we can calculate $\gamma_n = 0.653$ and the transconductance is then $G_m = 141.939\ \mu A/V$.

The load resistance is then set by the DC gain to $R = 125.285\ k\Omega$ which we round to a slightly higher value to have some margin on the gain.

Choosing $R = 126\ k\Omega$ we get $A_{dc} = 25.049\ dB$.

The transconductance also writes

$$G_m = \frac{G_{spec}}{n}\, g_{ms} = \frac{I_{spec}}{nU_T}\, g_{ms}, \tag{6.4}$$

from which we get the specific current

$$I_{spec} = \frac{G_m \, nU_T}{g_{ms}} \tag{6.5}$$

Knowing IC we can calculate $g_{ms} = 0.092$ and the specific current $I_{spec} = 50.970\ \mu A$. From I_{spec} and IC we get the bias current $I_b = 5.097\ \mu A$.

We round the bias current to $I_b = 5.100\ \mu A$. The W/L is then given by $W/L = 71.328$. To finally find W and L we use the specification on the maximum input-referred offset. If we neglect the β mismatch and the mismatch of the load resistance, we have

$$V_{os,max} = \frac{A_{\Delta V_{T0}}}{\sqrt{W\,L}} \tag{6.6}$$

We finally get $W = 21.114\ \mu m$ and $L = 296.012\ nm$, which we round to $W = 21.1\ \mu m$ and $L = 300\ nm$.

Finally, the load capacitance is set by the bandwidth as $C_L = 1.263\ pF$.

The design is finalized and summarized in Table 6.5.

Table 6.5: Summary of the design.

Parameter	Value	Unit
I_b	5.1	μA
R	126	$k\Omega$
C_L	1.263	pF
W	21.1	μm
L	300	nm

6.2 Simulation

We can now simulate the designed circuit with ngspice to check whether we meet the specifications.

6.2.1 Operating point

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating points by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 6.6.

Table 6.6: Operating point information.

Node	Voltage
vdd	1.8
in1	0.8
in2	0.8
out1	1.1574
out2	1.1574
1	0.384426
ic	0.8
id	0

Table 6.7: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[\mu A]$	I_{spec} $[\mu A]$	IC	n	V_{Dsat} $[mV]$
M1	5.100	74.619	0.068	1.27	117
M2	5.100	74.619	0.068	1.27	117

Table 6.8: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[\mu A/V]$
M1	1.27	183.610	143.521	39.060	1.030
M2	1.27	183.610	143.521	39.060	1.030

The large-signal transistor bias information and the small-signal parameters extracted from the simulation are given in Table 6.7 and Table 6.8, respectively.

6.2.2 Large-signal differential transfer characteristic

We now simulate the large-signal DC input-output transfer characteristic. The simulation result is presented in Figure 6.1.

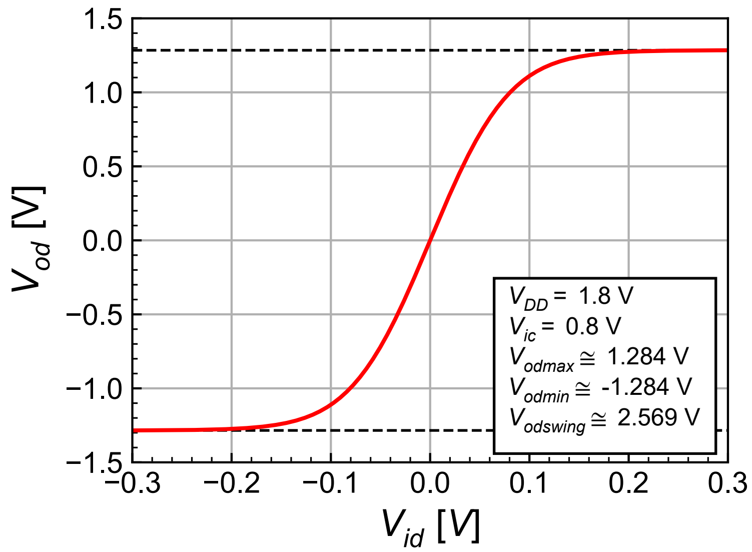

Figure 6.1: Simulated large-signal input-output characteristic.

From Figure 6.1, we see that the differential output voltage swing is $V_{od,swing} = 2.569\ V$, which as expected corresponds to $4R\,I_b = 2.570\ V$.

6.2.3 Transfer function

The simulated transfer function is shown in Figure 6.2.

From Figure 6.2 we see that the simulation matches the theoretical estimation. However, the DC gain is slightly smaller than the specification because of the transistor output conductance which has not been accounted for. On the other hand, the simulated bandwidth is slightly higher than the target because the DC gain is slightly smaller.

6.2.4 Input-referred noise

We can compare the theoretical input-referred noise to that obtained from simulations. The simulation results are presented in Figure 6.3.

We can check that the noise contribution of the load resistors is negligible. This is shown in Figure 6.4, which plots the input-referred thermal noise PSD for M_1-M_2 and R_1-R_2.

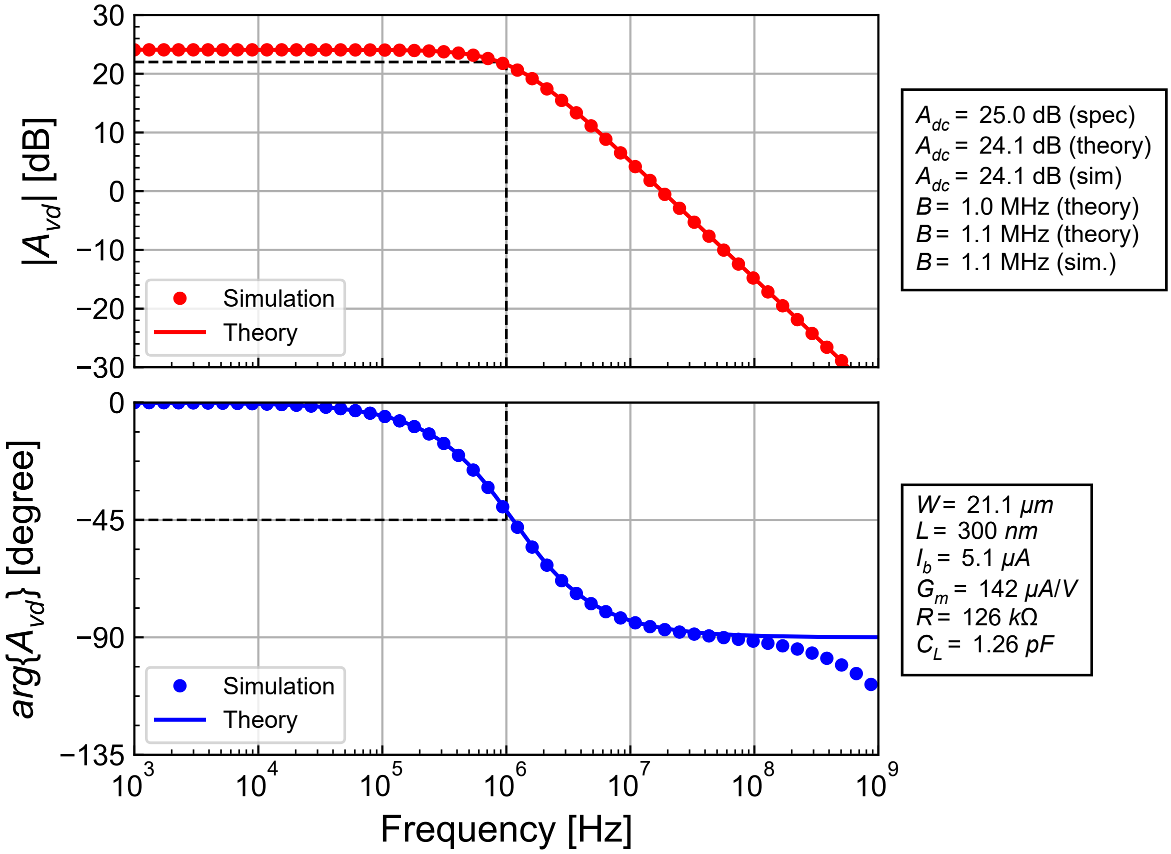

Figure 6.2: Simulated gain response compared to theoretical estimation.

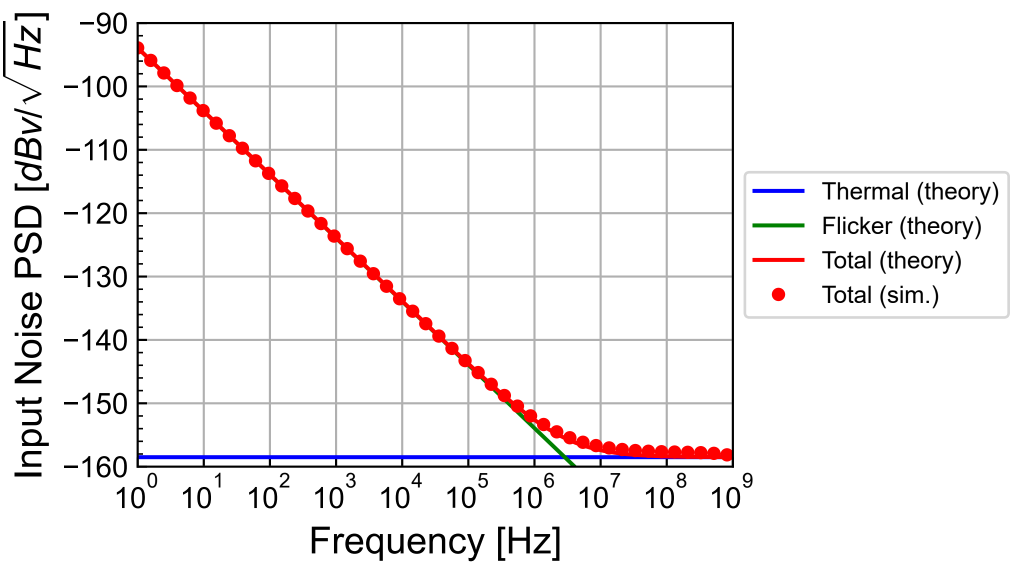

Figure 6.3: Simulated input-referred noise PSD.

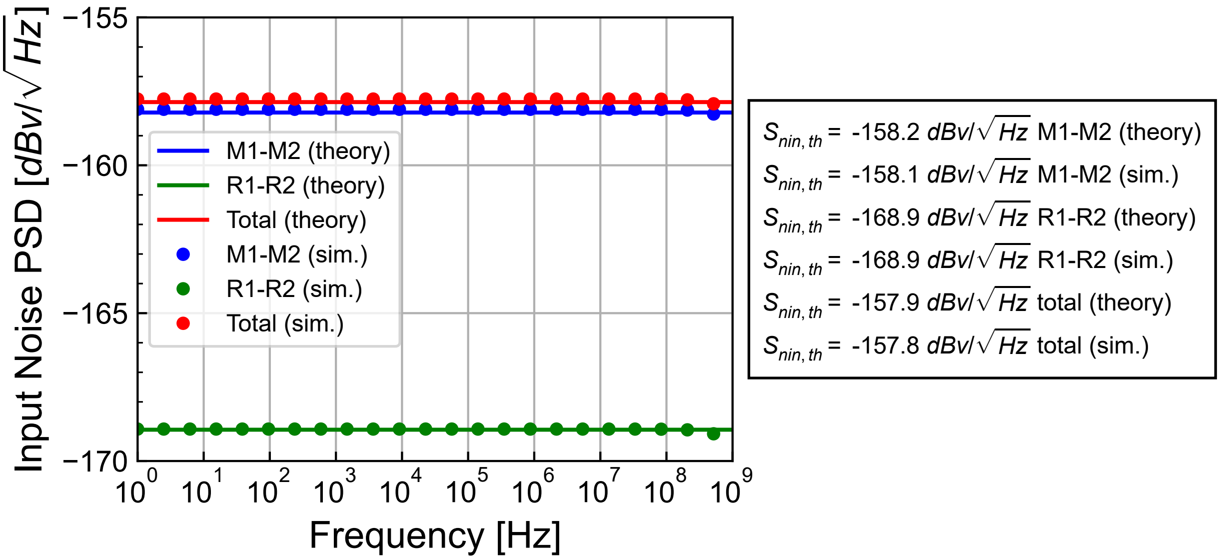

Figure 6.4: Breakdown of the contributions to the simulated input-referred white noise PSD.

We see that the contribution of R_1-R_2 is 10.813 dB smaller than the contribution of M_1-M_2.

6.3 Reducing the supply voltage

If we reduce the supply voltage keeping the same bias current, the RI drop across the load resistor will not change and remains equal to $V_{DD} - V_{out} = 0.643\ V$. If we keep the same input common-mode voltage $V_{ic} = 0.800\ V$, then the voltage at node 1 remains the same $V(1) = 0.384\ V$. The V_{DS} voltage of M_1-M_2 for $V_{DD} = 1.800\ V$ is $V_{DS} = 0.773\ V$. If we reduce the supply voltage to $V_{DD} = 1\,V$, the V_{DS} voltage gets negative and the transistors M_1-M_2 go out of saturation!

We need to reduce the input common mode voltage but leaving enough voltage at node 1 to keep the bias transistor in saturation. The V_{GS} voltage M_1-M_2 is 0.416 V. We therefore could reduce V_{ic} to 0.6 V which would leave 0.184 V for the bias current source and increase the V_{DS} voltage of M_1-M_2 to 0.173 V. This should be just enough to keep M_1-M_2 in saturation owing to the fact that they are biased in weak inversion.

What this illustrates is that the maximum gain of a $G_m\,R$ gain stage is directly related to the supply voltage. Indeed, the voltage gain is given by

$$A_{dc} = G_m\,R = \frac{G_m}{I_b} \cdot R\,I_b = \frac{G_m\,nU_T}{I_b} \cdot \frac{V_{DD} - V_{out}}{nU_T}. \tag{6.7}$$

If we assume that both the current source transistor and the differential pair are biased in weak inversion for maximum current efficiency and minimum saturation voltage, we then have $G_m\,nU_T/I_b \cong 1$ and $V_{out,min} = 2V_{DSsat} \cong 8U_T$. The voltage gain is then given by

$$A_{dc} \cong \frac{V_{DD} - 2V_{DSsat}}{nU_T} = \frac{V_{DD}/U_T - 8}{n}. \tag{6.8}$$

The minimum supply voltage for a given voltage gain including the peak-to-peak output signal swing $2\Delta V_{out}$ is given by

$$V_{DD,min} \cong nU_T \cdot A_{dc} + 2V_{DSsat} + 2\Delta V_{out}. \tag{6.9}$$

The minimum supply voltage given by (6.9) is plotted versus A_{dc} in Figure 6.5.

From Figure 6.5, we see that the minimum supply voltage to achieve the desired voltage gain $A_{dc} = 18$ is $V_{DD,min} = 0.9\ V$, so close to 1 V.

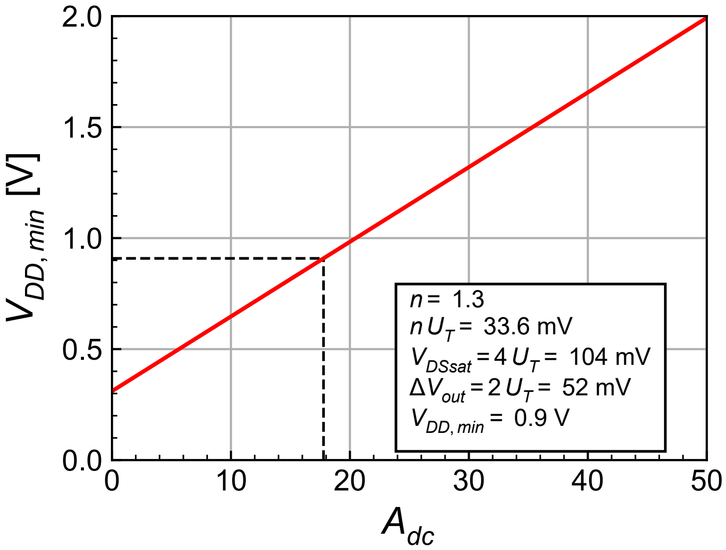

Figure 6.5: Minimum supply voltage versus voltage gain.