Fundamentals of Analog VLSI Design
Exercise 5 - Solution

The Cascode Gain Stage

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1 Cascode stage

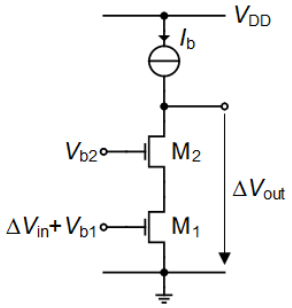

Figure 1.1: Schematic of the cascode gain stage.

1.1 Analysis

1.1.1 Small-signal analysis

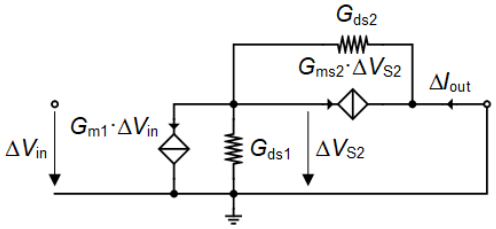

Figure 1.2: Small-signal schematic of the cascode stage of Figure 1.1 for the calculation of the equivalent transconductance.

The small-signal schematic corresponding to Figure 1.1 for the derivation of the equivalent transconductance is shown in Figure 1.2. Note that the output is short-circuited to ground for calculating the short-circuit output current and the corresponding transconductance. The equivalent transconductance is then given by

$$G_{meq} \triangleq \left.\frac{\Delta I_{out}}{\Delta V_{in}}\right|_{\Delta V_{out}=0} = G_{m1} \cdot \frac{G_{ms2}+G_{ds2}}{G_{ms2}+G_{ds1}+G_{ds2}} \cong G_{m1}, \tag{1.1}$$

which shows that assuming $G_{ms2} \gg G_{ds1}, G_{ds2}$, the equivalent transconductance of the cascode stage is equal to the transconductance of the driver transistor M_1. This result is expected since the cascode transistor is a common gate stage which has a unity current gain so that the current coming from the driver transistor M_1 is directly directed to the output.

The small-signal schematic for the calculation of the output conductance is shown in Figure 1.3. The output conductance is given by

$$G_{out} \triangleq \frac{\Delta I_{out}}{\Delta V_{out}} = \frac{G_{ds1}G_{ds2}}{G_{ms2}+G_{ds1}+G_{ds2}} \cong \frac{G_{ds1}}{G_{ms2}/G_{ds2}}, \tag{1.2}$$

which is equal to the output conductance of M_1, G_{ds1}, divided by the voltage gain of the cascode G_{ms2}/G_{ds2}. This means that, at low-frequency, the output conductance of a single transistor can be reduced by adding a cascode stage at the cost of some voltage headroom to maintain M_2 in saturation.

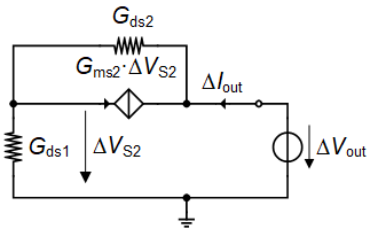

Figure 1.3: Small-signal schematic of the cascode stage of Figure 1.1 for the calculation of the output conductance.

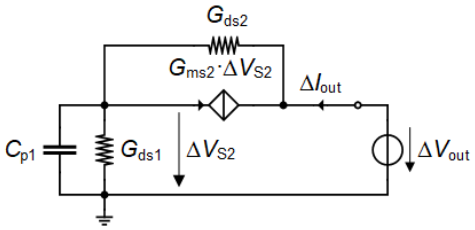

Figure 1.4: Small-signal schematic of the cascode stage of Figure 1.1 for the calculation of the output admittance including the parasitic capacitance C_{p1}.

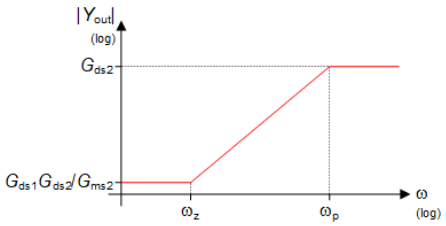

Figure 1.5: Effect of the parasitic capacitance C_{p1} on the output admittance Y_{out}.

The impact of the parasitic capacitance at node 1 on the output admittance can be investigated by adding the capacitance as shown in Figure 1.4. The output admittance then becomes

$$Y_{out} = G_{out} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}, \tag{1.3}$$

where

$$G_{out} \cong \frac{G_{ds1} G_{ds2}}{G_{ms2}}, \tag{1.4}$$

$$\omega_z \triangleq \frac{G_{ds1}}{C_{p1}}, \tag{1.5}$$

$$\omega_p \triangleq \frac{G_{ms2}}{C_{p1}}. \tag{1.6}$$

The magnitude of Y_{out} versus frequency is sketched in Figure 1.5. At low-frequency, i.e. for $\omega \ll \omega_z \ll \omega_p$, the output admittance is equal to the output conductance $Y_{out} \cong G_{out}$. However for $\omega_z \ll \omega_p \ll \omega$, the output admittance increases to the output conductance of M_2 $Y_{out} \cong G_{ds2}$. We see that the cascode effect is lost. This can easily be understood since for $\omega_p \ll \omega$, the cascode node 1 is shortened to the ac ground and the voltage controlling the source of M_2 is zero leaving the output conductance of M_2 only in the small-signal schematic of Figure 1.4.

1.1.2 Noise analysis

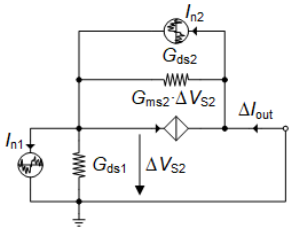

Figure 1.6: Small-signal schematic of the cascode stage of Figure 1.1 for the noise calculation.

To calculate the output noise PSD we can use the schematic shown in Figure 1.6. The output noise current is then given by

$$I_{nout} = \frac{G_{ms2} + G_{ds2}}{G_{ms2} + G_{ds1} + G_{ds2}} \cdot I_{n1} + \frac{G_{ds1}}{G_{ms2} + G_{ds1} + G_{ds2}} \cdot I_{n2} \cong I_{n1} + \frac{I_{n2}}{G_{ms2}/G_{ds1}}, \tag{1.7}$$

for $G_{ms2} \gg G_{ds1}, G_{ds2}$. We see that the contribution to the output noise current of the cascode stage I_{n2} is actually divided by G_{ms2}/G_{ds1}. Provided that this gain can be made sufficiently large and that both transistor have the same noise, the noise of the cascode stage can be made negligible compared to the noise due to M_1. Ultimately if $G_{ds1} = 0$, the noise current I_{n2} circulates in the cascode transistor M_2 (G_{ms2} in the small-signal schematic of Figure 1.6) and hence does not reach the output.

The output noise conductance G_{nout} is then given by

$$G_{nout}(f) \cong G_{n1}(f) + \left(\frac{G_{ds1}}{G_{ms2}}\right)^2 G_{n2}(f) \tag{1.8}$$

where the noise conductances are given by

$$G_{ni}(f) = \gamma_{ni} \cdot G_{mi} + \frac{\rho_n}{f\, W_i\, L_i} \cdot G_{mi}^2 \quad \text{for } i = 1, 2. \tag{1.9}$$

The input-referred noise is obtained by dividing G_{nout} by G_{meq}^2, resulting in

$$R_{nin} = \frac{G_{nout}(f)}{G_{meq}^2} \cong \frac{G_{nout}(f)}{G_{m1}^2} \cong \frac{G_{n1}(f)}{G_{m1}^2} + \left(\frac{G_{ds1}}{G_{m1}\,G_{ms2}}\right)^2 G_{n2}(f). \tag{1.10}$$

It can be decomposed into the thermal and flicker noise components according to

$$R_{nin} = R_{nt} + R_{nf}(f) \tag{1.11}$$

where R_{nt} is the total input-referred thermal noise given by

$$R_{nt} \cong \frac{\gamma_{n1}}{G_{m1}} + \left(\frac{G_{ds1}}{G_{m1}}\right)^2 \frac{\gamma_{n2}}{n_2\,G_{ms2}} = \frac{\gamma_{n1}}{G_{m1}} \cdot (1+\eta_{th}), \tag{1.12}$$

where η_{th}, given by

$$\eta_{th} \cong \frac{\gamma_{n2}}{n_2\,\gamma_{n1}} \cdot \frac{G_{ds1}^2}{G_{m1}\,G_{ms2}}, \tag{1.13}$$

represents the contribution of the cascode transistor M_2 to the input-referred thermal noise relative to that of M_1. Since γ_{n1} and γ_{n2} are of the same order of magnitude and $G_{m1}, G_{ms2} \gg G_{ds1}$, this results in $\eta_{th} \ll 1$, meaning that the contribution of M_2 is negligible compared to that of M_1 (at low frequency).

The noise excess factor of the cascode gain stage is given by

$$\gamma_{cas} \triangleq G_{meq} \cdot R_{nt} \cong G_{m1} \cdot R_{nt} = \gamma_{n1} \cdot (1+\eta_{th}) \cong \gamma_{n1}. \tag{1.14}$$

The thermal noise excess factor of the cascode gain stage is about equal to the thermal noise excess factor of the driver transistor M_1.

The input-referred flicker noise $R_{nf}(f)$ is given by

$$R_{nf}(f) \cong \frac{\rho_n}{f\,W_1 L_1} + \left(\frac{G_{ds1}}{G_{m1}}\right)^2 \frac{\rho_n}{n_2^2 f\,W_2 L_2} = \frac{\rho_n}{f\,W_1 L_1} \cdot (1+\eta_{fl}). \tag{1.15}$$

where η_{fl}, given by

$$\eta_{fl} = \left(\frac{G_{ds1}}{n_2\,G_{m1}}\right)^2 \frac{W_1 L_1}{W_2 L_2} \tag{1.16}$$

Assuming M_1 and M_2 have the same area and $G_{m1}/G_{ds1} \gg 1$, the contribution of M_2 to the input-referred flicker noise is negligible compared to that of M_1 and (1.15) simplifies to

$$R_{nf}(f) \cong \frac{\rho_n}{f\,W_1 L_1}, \tag{1.17}$$

which corresponds to the contribution of M_1 only.

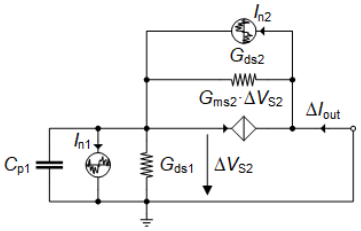

Figure 1.7: Small-signal schematic of the cascode stage of Figure 1.1 for the calculation of the noise including the effect of the parasitic capacitance C_{p1}.

Similarly, the impact of the parasitic capacitance on the noise can be calculated from Figure 1.7. The output noise conductance is then given by

$$G_{nout} = |H_{n1}(\omega)|^2 \cdot G_{n1} + |H_{n2}(\omega)|^2 \cdot G_{n2}, \tag{1.18}$$

where

$$H_{n1}(s) = \frac{1}{1 + s/\omega_p} \tag{1.19}$$

$$H_{n2}(s) = \frac{G_{ds1}}{G_{ms2}} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}. \tag{1.20}$$

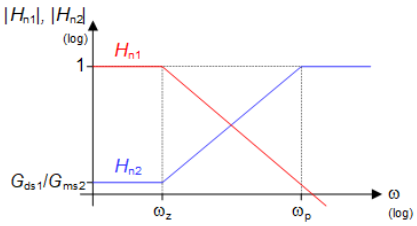

Figure 1.8: Magnitude of the noise transfer functions H_{n1} and H_{n2} versus frequency.

The magnitude of H_{n1} and H_{n2} versus frequency are sketched in Figure 1.8. For $\omega \ll \omega_z \ll \omega_p$, $H_{n1} \cong 1$ and $H_{n2} \cong G_{ds1}/G_{ms2}$ which is the result obtained above. However, for $\omega_z \ll \omega_p \ll \omega$, $H_{n1} \cong \omega_p/s$ and $H_{n2} \cong 1$. We see that the cascode effect is lost since the noise of M_2 is no more divided by the cascode gain G_{ms2}/G_{ds1} but is entirely transferred to the output.

As a conclusion, adding a cascode stage reduces the output conductance without penalty on the noise, but at the cost of a slight voltage overhead for maintaining M_2 in saturation. This is only true for $\omega < \omega_z = G_{ds1}/C_{p1}$. For frequencies $\omega \gg \omega_p = G_{ms2}/C_{p1}$ the cascode effect is lost. Note that in order to maximize G_{ms2} at a given current and minimize its saturation voltage, M_2 should be biased in weak inversion.

1.2 Design

We want to size the circuit of Figure 1.1 for the specifications given in Table 1.1. We need to find the minimum current and size the transistor to achieve these specs. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 1.2, the global process parameters in Table 1.3 and finally the MOSFET parameters in Table 1.4.

Table 1.1: Specifications for the differential pair with resistive loads.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	80	dB
DC gain	A_{dc}	10000	-
Gain-bandwidth product	GBW	10	MHz
Load capacitance	C_L	1	pF

Table 1.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 1.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 1.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	13	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	6.8e-23	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

The gain-bandwidth product direcly sets the transconductance of M_1 as $G_{m1} = 62.832\ \mu A/V$. Imposing an inversion coefficient $IC_1 = 1$ allows to derive the required bias current as $I_b = G_{m1}\, n\, U_T / gmsid(IC1) = 3.344\ \mu A$. We then can find the specific current $I_{spec1} = 3.344\ \mu A$ and aspect ratio $W_1/L_1 = 4.677$.

The DC gain then sets the output conductance as $G_{out} = 6.283\ nA/V$. To minimize the voltage headroom needed for M_2 and maximize its current efficiency, we will bias M_2 in weak inversion setting its inversion coefficient to $IC_2 = 0.1$. Knowing IC_2 and I_b we can deduce its source transconductance as $G_{ms2} = 118.405\ \mu A/V$. If we split the overall voltage gain equally between M_1 and M_2 we get $G_{m1}/G_{ds1} = G_{ms2}/G_{ds2} = \sqrt{A_{dc}} = 100$. We now can deduce $G_{ds1} = 0.628\ \mu A/V$ and $G_{ds2} = 1.184\ \mu A/V$. This leads to $L_1 = 0.49\ \mu m$ and $L_2 = 0.29\ \mu m$.

It turns out that the length of M_1 and M_2 are actually independent of their transconductances G_{m1}

and G_{ms2}. Indeed, from the output conductance we get the transistor length as

$$L_1 = \frac{I_b}{\lambda_n G_{ds1}} \tag{1.21}$$

The output conductance G_{ds1} is set by the required DC gain as

$$G_{ds1} = \frac{G_{m1}}{\sqrt{A_{dc}}} = \frac{2\pi\, GBW\, C_L}{\sqrt{A_{dc}}} \tag{1.22}$$

Now the bias current is given by

$$I_b = G_{m1} \frac{n_1 U_T}{gmsid(IC_1)} \tag{1.23}$$

Replacing (1.23) and (1.22) in (1.21) results in

$$L_1 = \frac{n_1 U_T \sqrt{A_{dc}}}{\lambda_n\, gmsid(IC_1)}, \tag{1.24}$$

which is independent of the transconductance G_{m1}.

Similarly for M_2 we get

$$L_2 = \frac{U_T \sqrt{A_{dc}}}{\lambda_n\, gmsid(IC_2)}, \tag{1.25}$$

which is independent of the source transconductance G_{ms2} of M_2.

We now get the transistor width as $W_1 = 1.88\ \mu m$ and $W_2 = 10.12\ \mu m$.

We still need to set the bias voltage for the cascode transistor. We want to bias M_1 at the onset of saturation V_{DSsat1}. The V_{GS2} voltage of M_2 can be approximated by V_{T0n}. The bias voltage is then given by

$$V_{b2} = V_{GS2} + V_{DSsat1} \tag{1.26}$$

which is $0.571\ V$. We will set it to $V_{b2} = 0.650\ V$ so we have some margin.

Table 1.5: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [\mu A]$	$I_{spec}\ [\mu A]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1	1.88	0.49	3.344	2.763	1.2	22	118
M2	10.12	0.29	3.344	24.682	0.1	-38	105
M3	1.88	0.49	3.344	2.763	1.2	22	118
M4	10.12	0.29	3.344	24.682	0.1	-38	105

Table 1.6: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1	106.796	75.656	59.508	529.950	0.724
M2	953.893	115.312	90.700	877.208	0.659
M3	106.796	75.656	59.508	529.950	0.724
M4	953.893	115.312	90.700	877.208	0.659

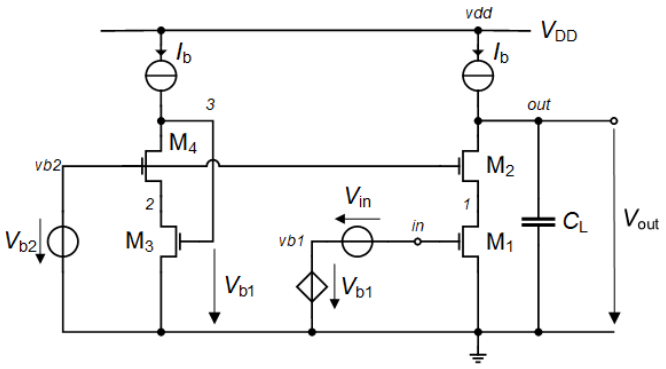

Figure 1.9: Schematic used for the simulation of the transfer function.

1.3 Simulations

We can now can check the design by simulation using the circuit shown in Figure 1.9. The purpose of M_3 and M_4 is to set the DC gate voltage of M_1 such that its current is equal to the bias current. Of course M_3 is identical to M_1 and M_4 is identical to M_2.

We first will check the operating point. The node voltages are given in Table 1.7. We can check that all transistors are biased in saturation. The transistor operating point information are given in Table 1.8 and Table 1.9. We see that the simulated transconductances are very close to the theoretical values given in Table 1.6.

Table 1.7: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
in	0.527778
out	0.527778
vb2	0.65
1	0.176378
2	0.176378
3	0.527778

Table 1.8: Large-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC [-]	n [-]	V_{DSsat} $[mV]$
M1	3.344	3.182	1.060	1.27	157
M2	3.344	33.928	0.099	1.27	120
M3	3.344	3.182	1.060	1.27	157
M4	3.344	33.928	0.099	1.27	120

Table 1.9: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	G_m $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_{ds} $[nA/V]$
M1	60.093	77.541	878.705
M2	93.586	117.423	992.781
M3	60.093	77.541	878.705
M4	93.586	117.423	992.781

1.3.1 Transfer function

We now can simulate the transfer function which is plotted in Figure 1.10. We see that the simulation results are close to the theoretical vaues. The GBW is slightly lower than specs despite the simulated transconductance G_{m1} is larger. This is coming from the self-loading. Indeed, since M_2 is biased in weak inversion, it is a fairly large transistor and therefore its paraisitc capacitance at the drain adds to the load capaciance. We could estimate this parasitic capacitance and add it to the load capacitance.

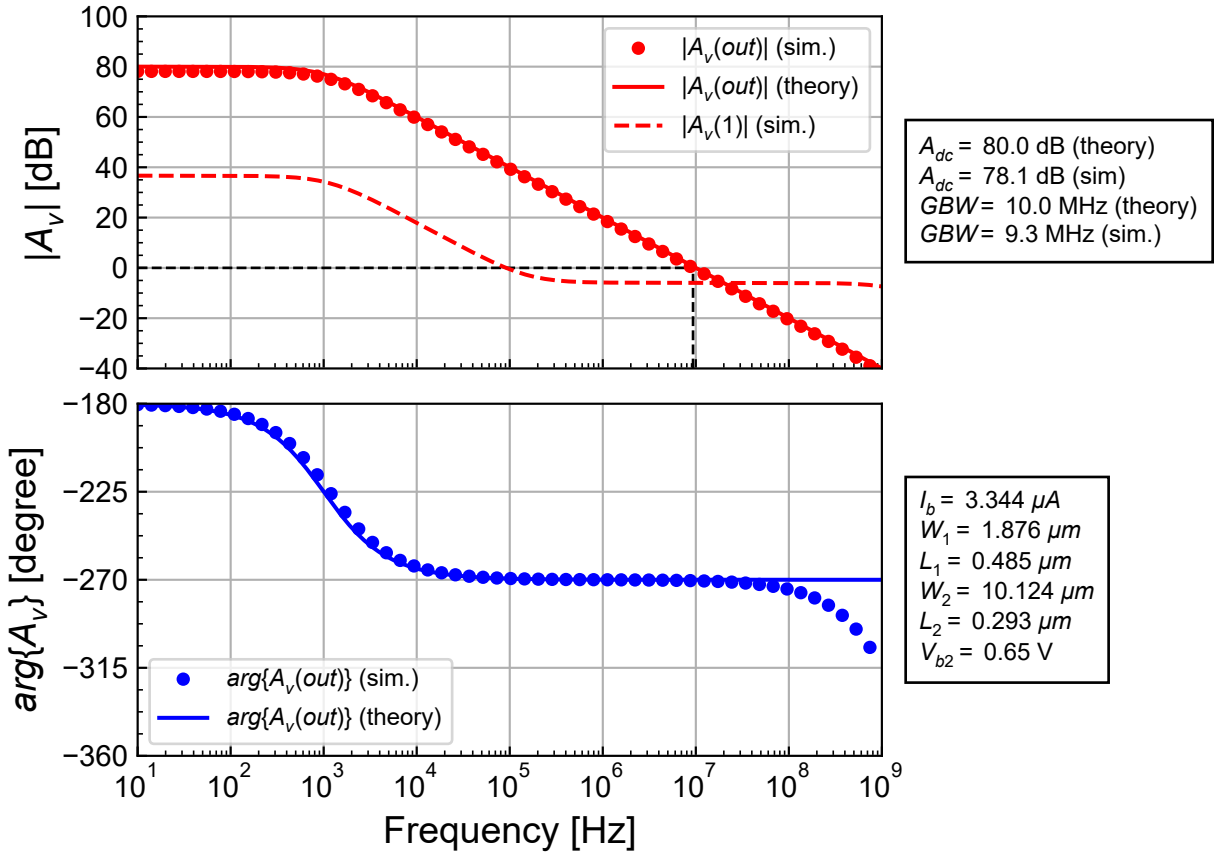

Figure 1.10: Simulated gain response compared to theoretical estimation.

1.3.2 Input-referred noise

We can compare the theoretical input-referred noise to that obtained from simulations. The simulation results are presented in Figure 1.11.

The simulation confirms that, below the gain-bandwidth product $GBW = 10\ MHz$, the square root of the input-referred flicker noise of M_2 is about 40 dB lower than that of M_1.

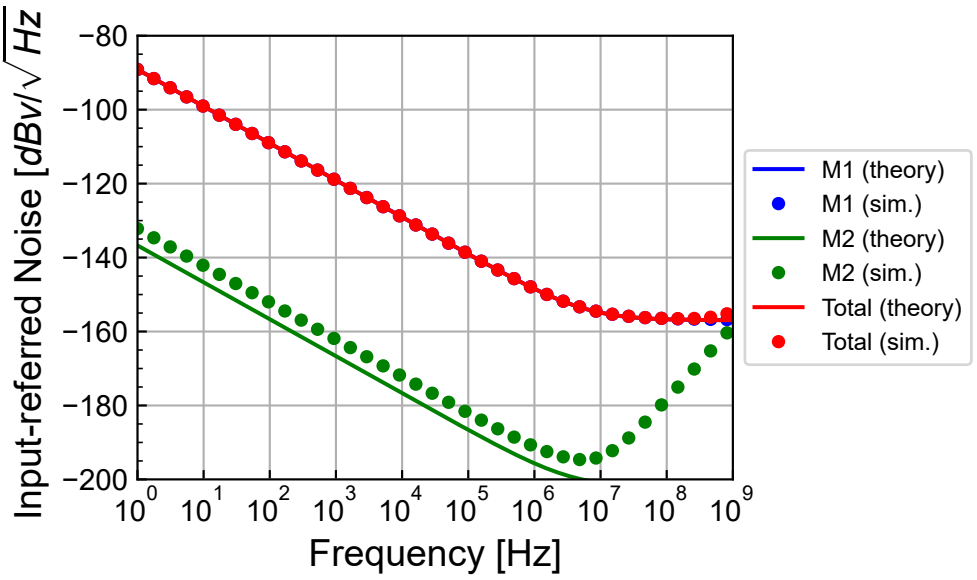

Figure 1.11: Simulated input-referred noise PSD compared to theoretical estimation.

2 Regulated cascode

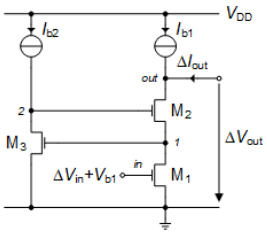

Figure 2.1: Schematic of the regulated cascode.

The schematic of Figure 2.1 corresponds to the regulated cascode, where an additional CS gain stage M_3 is added.

2.1 Small-signal analysis

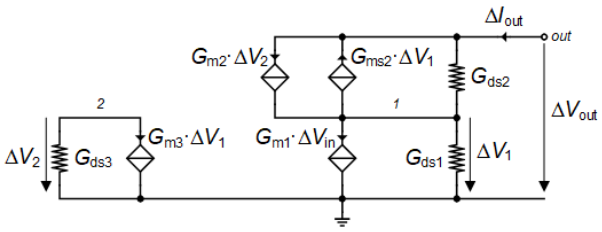

Figure 2.2: Small-signal schematic of the regulated cascode.

The small-signal equivalent schematic of the regulated cascode of Figure 2.1 is presented in Figure 2.2.

Solving the KCL equations accounting for all the output conductances leads to the full expression of the equivalent transconductance given by

$$G_{meq} = G_{m1} \cdot \frac{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds2})}{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds2} + G_{ds1})} \tag{2.1}$$

which for $G_{ms2} \gg G_{ds2}, G_{ds1}$ reduces to

$$G_{meq} \cong G_{m1}. \tag{2.2}$$

This is the same result as the cascode stage.

The output conductance accounting for all transistor's output conductances is given by

$$G_{out} = \frac{G_{ds1}\,G_{ds2}\,G_{ds3}}{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds2} + G_{ds1})}, \tag{2.3}$$

which for $G_{ms2} \gg G_{ds2}, G_{ds1}$ reduces to

$$G_{out} \cong G_{ds1} \cdot \frac{G_{ds2}}{G_{m2}} \cdot \frac{G_{ds3}}{G_{m3}}. \tag{2.4}$$

Equation (2.4) shows that the output conductance of the regulated cascode is equal to the output conductance of M_1 divided by the square of a transistor self-gain, i.e. $(G_m/G_{ds})^2$, this is G_m/G_{ds} smaller than that of the simple cascode.

The voltage gain is given by

$$A_v \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{G_{meq}}{G_{out}} = -G_{m1} \cdot \frac{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds2})}{G_{ds1}\,G_{ds2}\,G_{ds3}}, \tag{2.5}$$

which for $G_{ms2} \gg G_{ds2}, G_{ds1}$ and reduces to

$$A_v \cong -\frac{G_{m1}}{G_{ds1}} \cdot \frac{G_{m2}}{G_{ds2}} \cdot \frac{G_{m3}}{G_{ds3}}. \tag{2.6}$$

Equation (2.6) shows that the voltage gain of the regulated cascode is equivalent of that of a cascade of three stages, i.e. $(G_m/G_{ds})^3$. However, this gain is achieved at lower current since the driver transistor M_1 and the cascode transistor M_2 share the same current (current reuse).

2.2 Noise analysis

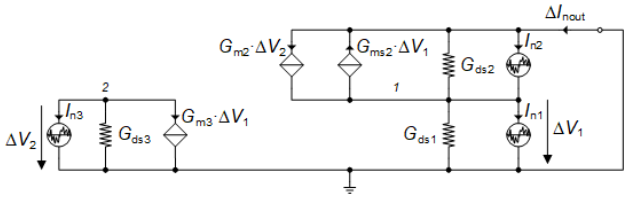

Figure 2.3: Small-signal schematic of the regulated cascode including the noise sources.

The equivalent small-signal circuit of the regulated cascode including all the noise current sources for the calculation of the noise is shown in Figure 2.3. The output noise current is given by

$$I_{nout} = H_{n1} \cdot I_{n1} + H_{n2} \cdot I_{n2} + H_{n3} \cdot I_{n3}. \tag{2.7}$$

where

$$H_{n1} = \frac{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds2})}{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds1} + G_{ds2})} \cong 1, \tag{2.8}$$

$$H_{n2} = \frac{G_{ds1}\,G_{ds3}}{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds1} + G_{ds2})} \cong \frac{G_{ds1}\,G_{ds3}}{G_{m2}\,G_{m3}}, \tag{2.9}$$

$$H_{n3} = -\frac{G_{m2}\,G_{ds1}}{G_{m2}\,G_{m3} + G_{ds3}\,(G_{ms2} + G_{ds1} + G_{ds2})} \cong -\frac{G_{ds1}}{G_{m3}}. \tag{2.10}$$

Equation (2.8) shows that the noise of M_1 is transferred directly to the output. Equation (2.9) shows that the noise of M_2 is divided by the square of a transistor self-gain, i.e. divided by $(G_m/G_{ds})^2$. Finally, the noise coming from M_3 is divided by G_m/G_{ds}. This means that the noise coming from M_2 and M_3 are much smaller than the noise coming from M_1 and can usually be neglected. We still will derive the output and input-referred noise accounting for all contributions.

The output noise conductance is given by

$$G_{nout} = |H_{n1}|^2 \cdot G_{n1} + |H_{n2}|^2 \cdot G_{n2} + |H_{n3}|^2 \cdot G_{n3} \tag{2.11}$$

where G_{ni} is given by (1.9).

The input-referred noise is obtained by dividing G_{nout} by G_{meq}^2, resulting in

$$R_{nin} = \frac{G_{nout}(f)}{G_{meq}^2}. \tag{2.12}$$

It can be decomposed into a thermal and flicker noise component according to

$$R_{nin} = R_{nt} + R_{nf}(f) \tag{2.13}$$

R_{nt} is the total input-referred thermal noise resistance which can be written as

$$R_{nt} = \frac{\gamma_{n1}}{G_{m1}} \cdot (1 + \eta_{th}), \tag{2.14}$$

where η_{th} represents the contributions of M_2 and M_3 to R_{nt} relative to that of M_1

$$\eta_{th} \cong \frac{\gamma_{n2}}{\gamma_{n1}} \cdot \frac{G_{ds1}^2\, G_{ds3}^2}{G_{m1}\, G_{m2}\, G_{m3}^2} + \frac{\gamma_{n3}}{\gamma_{n1}} \cdot \frac{G_{ds1}^2}{G_{m1}\, G_{m3}}. \tag{2.15}$$

η_{th} allows to compare the contributions of M_2 and M_3 to that of M_1. It confirms what we already have mentioned above, namely that the contribution of M_2 (first term in (2.15)) is completely negligible since it is inversely proportional to $(G_m/G_{ds})^4$. The contribution of M_3 (second term in (2.15)) is also very small since it is inversely proportional to $(G_m/G_{ds})^2$.

The input-referred flicker noise resistance is given by

$$R_{nf} = \frac{\rho_n}{f\, W_1\, L_1} \cdot (1 + \eta_{fl}), \tag{2.16}$$

where η_{fl} represents the contributions of M_2 and M_3 to R_{nf} relative to the that of M_1

$$\eta_{fl} \cong \left(\frac{G_{ds1}}{G_{m1}} \cdot \frac{G_{ds3}}{G_{m3}}\right)^2 \cdot \frac{W_1\, L_1}{W_2\, L_2} + \left(\frac{G_{ds1}}{G_{m1}}\right)^2 \cdot \frac{W_1\, L_1}{W_3\, L_3}. \tag{2.17}$$

Similarly to the thermal noise, assuming that M_1, M_2 and M_3 have all about the same gate area, (2.17) shows that the contribution of M_2 (first term in (2.17)) is completely negligible since it is inversely proportional to $(G_m/G_{ds})^4$. The contribution of M_3 (second term in (2.17)) is also very small since it is inversely proportional to $(G_m/G_{ds})^2$.

The equivalent noise excess factor of the regulated cascode can then be written as

$$\gamma_{neq} \triangleq G_{meq} \cdot R_{nt} \cong \gamma_{n1} \cdot (1 + \eta_{th}) \cong \gamma_{n1}. \tag{2.18}$$

This shows that, similarly to the cascode gain stage, the noise of the regulated cascode is dominated by the contribution of the driver transistor M_1.