

Fundamentals of Analog VLSI Design

Exercise 4 - Solution

Basic Common-source Gain Stages

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1 Problem 1

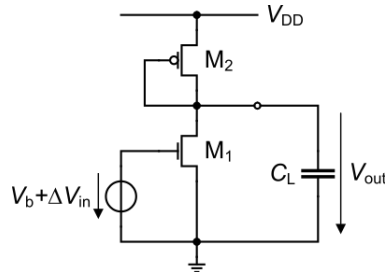


Figure 1.1: Schematic of an elementary gain stage with diode connected load.

Figure 1.1 shows the schematic of a simple common-source (CS) gain-stage with a diode-connected pMOS load. We first will analyze the small-signal operation of this circuit and then will design it for the specifications given in Table 1.1 for a generic 180nm bulk CMOS process. Finally we want to validate the design with circuit simulation.

1.1 Analysis

- Draw the small-signal schematic of including all the noise sources.
- Derive the small-signal transfer function $A_v(s) \triangleq \Delta V_{out}/\Delta V_{in}$. Give the DC gain A_{dc} and cut-off frequency f_c .
- How should M_1 and M_2 be biased to maximize the DC voltage gain?
- What is the maximum achievable voltage gain?
- Calculate the input-referred noise resistance R_{nin} and split it in terms of the input-referred thermal noise resistance R_{nt} and flicker noise resistance R_{nf} .
- Calculate the input-referred thermal noise excess factor $\gamma_{neq} \triangleq G_{m1} \cdot R_{nt}$.
- How should M_1 and M_2 be biased to minimize the input-referred thermal noise excess factor?

1.1.1 Small-signal equivalent circuit

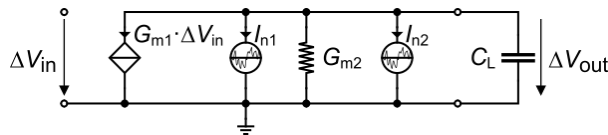


Figure 1.2: Small-signal schematic of an elementary gain stage with diode connected load including all the noise sources.

The equivalent small-signal schematic is shown in Figure 1.2. We have neglected the output conductances of M_1 and M_2 because it comes in parallel with G_{m2} and usually we can consider that $G_{ds1}, G_{gds2} \ll G_{m2}$.

1.1.2 Small-signal voltage gain

The small-signal voltage gain assuming there is no load is given by

$$A_v(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A_{dc}}{1 + s/\omega_c}. \quad (1.1)$$

with

$$A_{dc} = -\frac{G_{m1}}{G_{m2}}, \quad (1.2)$$

$$\omega_c = \frac{G_{m2}}{C_L}. \quad (1.3)$$

The DC voltage gain is maximized when M_1 is biased in weak inversion and M_2 in strong inversion. In this case we have

$$G_{m1} = \frac{I_b}{n_1 U_T}, \quad (1.4)$$

$$G_{m2} = \frac{2I_b}{V_{P2}} = \frac{2n_2 I_b}{V_{BG2} - V_{T0p}}, \quad (1.5)$$

which results in

$$A_{dc} = -\frac{V_{BG2} - V_{T0p}}{2n_1 n_2 U_T}. \quad (1.6)$$

Since M_1 is biased in weak inversion its saturation voltage is about $V_{Dsat1} = 4U_T$. The maximum voltage gain is then directly related to the supply voltage according to

$$A_{dc,max} \cong -\frac{V_{DD} - 4U_T - V_{T0p}}{2n_1 n_2 U_T}. \quad (1.7)$$

The voltage gain is ultimately limited by the supply voltage (and the pMOS threshold voltage).

1.1.3 Input-referred noise

The input-referred noise resistance is given by

$$R_{nin} = \frac{G_{n1} + G_{n2}}{G_{m1}^2}, \quad (1.8)$$

where

$$G_{ni} = \gamma_{ni} \cdot G_{mi} + G_{mi}^2 \cdot \frac{\rho_i}{W L f} \quad \text{for } i = 1, 2 \quad (1.9)$$

1.1.3.1 Thermal noise

The input-referred thermal noise resistance is given by

$$R_{nt} = \frac{\gamma_{n1}}{G_{m1}} \cdot (1 + \eta_{th}) = \frac{\gamma_{neq}}{G_{m1}} \quad (1.10)$$

and the amplifier thermal excess noise factor by

$$\gamma_{neq} = \gamma_{n1} \cdot (1 + \eta_{th}), \quad (1.11)$$

where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}} \cdot \frac{G_{m2}}{G_{m1}} = \frac{\gamma_{n2}}{\gamma_{n1}} \cdot \frac{1}{|A_v|}. \quad (1.12)$$

Note that η_{th} corresponds to the contribution of M_2 to the input referred thermal noise relative to the contribution of M_1 .

1.1.3.2 Flicker noise

The input-referred flicker noise resistance is given by

$$R_{nf} = \frac{\rho_n}{W_1 L_1 f} \cdot (1 + \eta_{fl}), \quad (1.13)$$

with

$$\eta_{fl} = \frac{\rho_p}{\rho_n} \cdot \left(\frac{G_{m2}}{G_{m1}} \right)^2 \cdot \frac{W_1 L_1}{W_2 L_2} \quad (1.14)$$

Note that η_{fl} corresponds to the contribution of M_2 to the input referred flicker noise relative to the contribution of M_1 .

Finally the corner frequency is given by

$$f_k = \frac{\rho_n}{W_1 L_1} \cdot \frac{G_{m1}}{\gamma_{n1}} \cdot \frac{1 + \eta_{fl}}{1 + \eta_{th}}. \quad (1.15)$$

We can now proceed with the design.

1.2 Design

We now will design the amplifier for the specifications given in Table 1.1.

Table 1.1: Specifications for problem 1.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	-10	-
DC gain in dB	$A_{dc,dB} = 20 \log(A_{dc})$	20	dB
Cut-off frequency	f_c	1	MHz
Load capacitance	C_L	1	pF

Table 1.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 1.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 1.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\Box}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	6.8e-23	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

Note that the effective channel width and length are defined as follows

$$W_{eff} \triangleq W + \Delta W, \quad (1.16)$$

$$L_{eff} \triangleq L + \Delta L, \quad (1.17)$$

where W and L are drawn width and length.

The maximum achievable DC gain is given by

$$A_{dc,max} \cong -\frac{V_{DD} - 4U_T - V_{T0p}}{2n_1 n_2 U_T}. \quad (1.18)$$

which gives $A_{dc,max} = -14.565$ or 23.266 dB.

The transconductance of M_2 is set by the bandwidth as $G_{m2} = 2\pi f_c C_L = 6.283 \mu A/V$, while the transconductance of M_1 is set by the DC gain as $G_{m1} = |A_{dc}| G_{m2} = 62.832 \mu A/V$.

The minimum bias current for achieving the required G_{m1} is given by $I_{b,min} = G_{m1} nU_T = 2.067 \mu A$. We choose to bias M_1 in weak inversion for maximum current efficiency and therefore set its inversion coefficient to $IC_1 = 0.1$. We can deduce the bias current I_b from the G_m/I_b ratio as $I_b = G_{m1} nU_T / gmsid(IC_1) = 2.256 \mu A$, where $gmsid$ is the normalized G_m/I_D function. We can deduce I_{spec} and W/L for M_1 as $I_{spec1} = I_b / IC_1 = 22.563 \mu A$ and $W/L = 31.556$. Choosing $L_1 = L_{min} = 180$ nm, we get $W_{eff1} = 3.282 \mu m$ and $W_1 = 3.243 \mu m$.

Having G_{m2} and I_b , we can deduce $G_{m2} nU_T / I_b = 0.094$ from which we get M_2 's inversion coefficient $IC_2 = 102.291$ where we have assumed that M_2 is a long-channel device. Since the inversion coefficient

is rather large, we need to check the quiescent output voltage to make sure M_1 remains in saturation for the given supply voltage. We first calculate the bulk-to-gate voltage of M_2 $V_{BG2} = 1.172 \text{ V}$. The quiescent output voltage is then estimated as $V_{outq} = V_{DD} - V_{BG2} = 0.628 \text{ V}$, which is large enough for keeping M_1 in saturation.

We can now size M_2 , by first calculating $I_{spec2} = 22 \text{ nA}$ and the aspect ratio $W/L = 0.127$. Choosing $W_2 = W_{min} = 200 \text{ nm}$, we get $L_{eff2} = 1.994 \text{ }\mu\text{m}$ and $L_2 = 2.066 \text{ }\mu\text{m}$.

The thermal noise excess factors of M_1 and M_2 only depend on their inversion coefficient and slope factors. They are given by $\gamma_{n1} = 0.653$ and $\gamma_{n2} = 0.850$ from which we get $\eta_{th} = 0.130$. This means that the contribution of M_2 to the input-referred thermal noise is only 0.130 times that of M_1 . The equivalent thermal noise excess factor is then given by $\gamma_{neq} = 0.738$ which is only slightly larger than $\gamma_{n1} = 0.653$. The input-referred thermal noise resistance and PSD are given by $R_{nt} = 11.753 \text{ k}\Omega$ and $\sqrt{S_{nth}} = 13.951 \text{ nV}/\sqrt{\text{Hz}}$.

The flicker noise PSD at 100 Hz is given by $\sqrt{S_{nf}(100\text{Hz})} = 5.449 \text{ }\mu\text{V}/\sqrt{\text{Hz}}$. The corner frequency is given by $f_k = 15.253 \text{ MHz}$, which is very large. We can try to reduce f_k by increasing the gate areas of M_1 and M_2 .

In order to keep η_{fl} constant, we need to increase both $W_1 L_1$ and $W_2 L_2$ by the same factor. In order to bring the corner frequency down to 1 MHz we need to increase $W_1 L_1$ and $W_2 L_2$ by a factor 15.253. Keeping the same W/L , this changes W_1 , L_1 , W_2 and L_2 according to $W_1 = 12.778 \text{ }\mu\text{m}$, $L_1 = 482 \text{ nm}$, $W_2 = 938 \text{ nm}$ and $L_2 = 7.858 \text{ }\mu\text{m}$.

1.3 Simulations

- Simulate the designed circuit with ngspice.

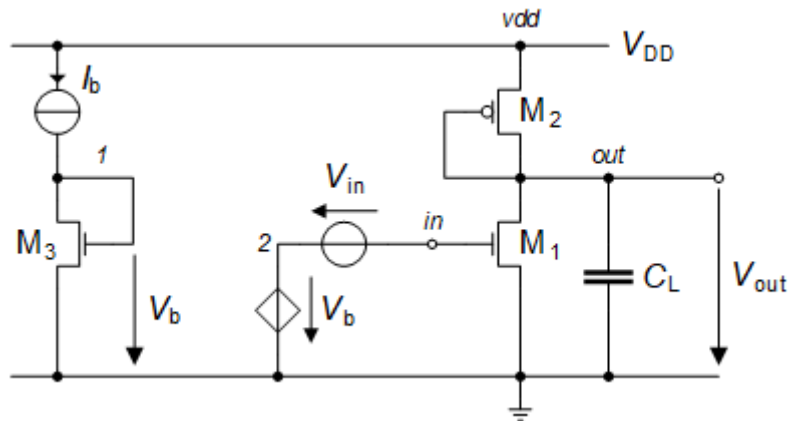


Figure 1.3: Schematic of the common-source (CS) gain stage used for simulation.

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.3, where transistor M_3 is used to correctly bias the gate of the CS transistor M_1 for the desired bias current I_b .

The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=2.256u CL=1.0p
.param W1=12.78u L1=482n AD1=5.13e-12 PD1=2.64e-05 W2=938n L2=7.86u AD2=3.97e-13 PD2=2.78e-06
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.5.

Table 1.5: Operating point information.

Node	Voltage
vdd	1.8
in	0.425679
out	0.497434
1	0.425679
2	0.425679

The operating information for each transistor can be extracted and are given in Table 1.6 and Table 1.7.

Table 1.6: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D [μA]	I_{spec} [μA]	IC	n	V_{Dsat} [mV]
M1	2.278	23.481	0.097	1.27	120
M2	2.278	0.015	147.801	1.31	732

Table 1.7: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} [$\mu A/V$]	G_m [$\mu A/V$]	G_{mb} [$\mu A/V$]	G_{ds} [$\mu A/V$]
M1	1.27	80.428	62.504	17.625	0.299
M2	1.31	6.706	4.835	1.865	0.005

We see that the transconductance of M_1 is close to the theoretical value. However the transconductance of M_2 is lower than the theoretical value resulting in a higher DC gain. This is due to the fact that M_2 is biased in very strong inversion with a high value of its gate voltage. This results in a mobility reduction due to the vertical field which results in a reduction of the transconductance. Note that this effect is not accounted for in the sEKV model, but is included in the EKV 2.6 compact model used for the simulations.

The transfer function magnitude and phase are plotted in Figure 1.4, which shows a good fit between the simulation and the theoretical estimation.

We can compare the theoretical input-referred noise to that obtained from simulations. The simulation results are presented in Figure 1.5. We see a very good agreement. Additionally, the corner frequency is at 1 MHz as set in the design.

i Note

In ngspice it is unfortunately not possible to turn off the noise for a given MOSFET. It is therefore important to generate the raw file with the noise contributions of all devices and then pick the contributions of M_1 and M_2 only, avoiding that of M_3 .

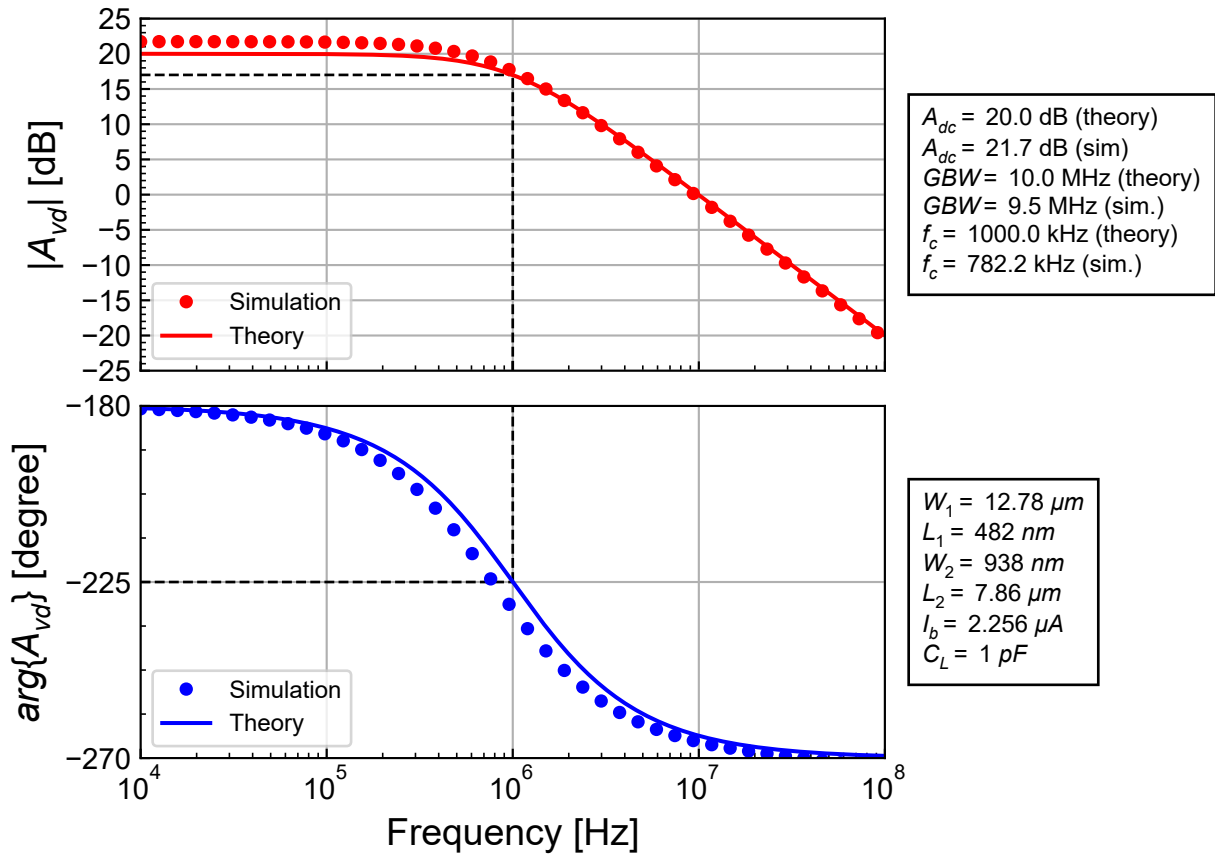


Figure 1.4: Simulated gain response compared to theoretical estimation for the long-channel case.

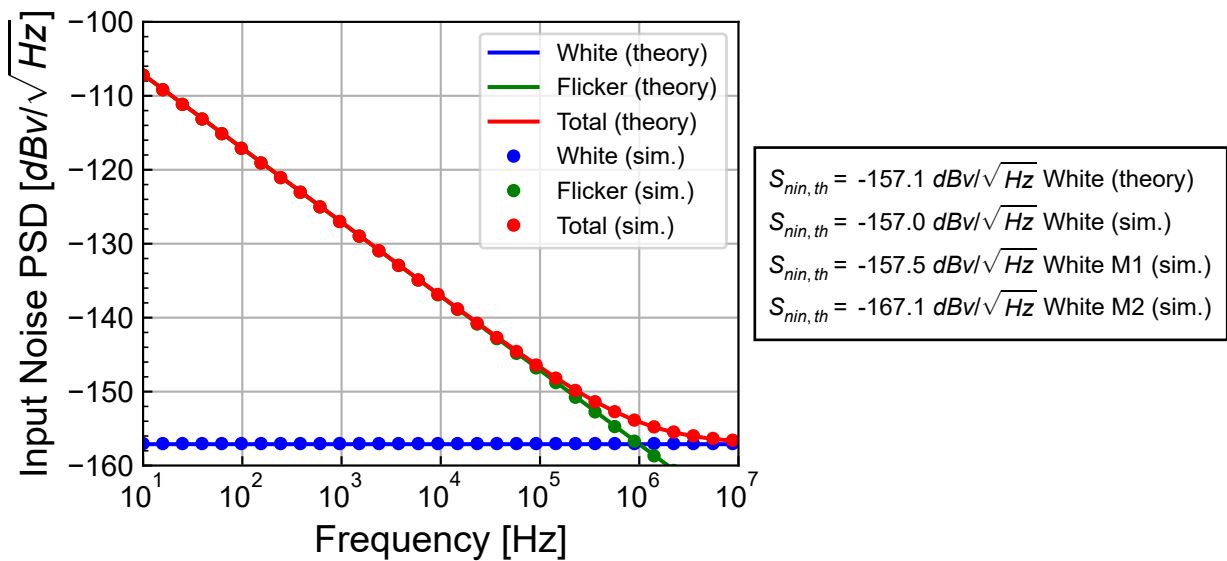


Figure 1.5: Simulated input-referred noise PSD.

2 Problem 2

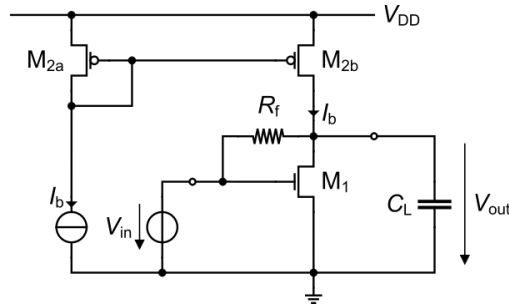


Figure 2.1: Schematic of an elementary gain stage with resistive feedback.

Figure 2.1 shows the schematic of another simple common-source (CS) gain-stage with a feedback resistance R_F . We first will analyze the small-signal operation of this circuit and then will design it for the specifications given in Table 2.1 for a generic 180nm bulk CMOS process. Finally we want to validate the design with circuit simulation.

2.1 Analysis

- Draw the small-signal schematic of the circuit of Figure 2.1 including all the noise sources.
- Derive the small-signal transfer function $A_v(s) \triangleq \Delta V_{out}/\Delta V_{in}$. Give the DC gain A_{dc} and cut-off frequency f_c assuming that $G_{m1} \cdot R_f \gg 1$.
- Calculate the input-referred noise resistance R_{nin} and split it in terms of the input-referred thermal noise resistance R_{nt} and flicker noise resistance R_{nf} .
- Calculate the input-referred thermal noise excess factor $\gamma_{neq} \triangleq G_{m1} \cdot R_{nt}$.
- How should M_1 , M_{2a} and M_{2b} be biased to minimize the input-referred thermal noise excess factor?

2.1.1 Small-signal equivalent circuit

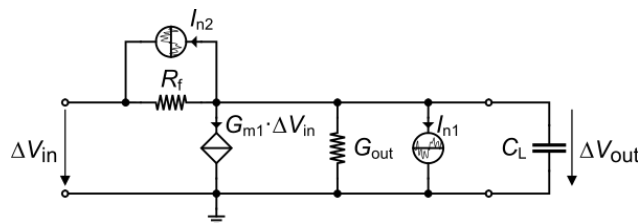


Figure 2.2: Small-signal schematic of the elementary gain stage with resistive feedback including all the noise sources.

The equivalent small-signal schematic is shown in Figure 2.2. Conductance G_{out} is the sum of the output conductances of M_1 and M_{2b} $G_{out} = G_{ds1} + G_{ds2}$. Note that the noise current source I_{n1} includes the noise of M_1 , M_{2a} and M_{2b} .

2.1.2 Small-signal voltage gain

The small-signal voltage gain assuming there is no load is given by

$$A_v(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A_{dc}}{1 + s/\omega_c}. \quad (2.1)$$

with

$$A_{dc} = \frac{1 - G_{m1} R_f}{1 + G_{out} R_f}, \quad (2.2)$$

$$\omega_c = \frac{1 + G_{out} R_f}{R_f C_L}. \quad (2.3)$$

The DC gain is maximized by setting $G_{m1} R_f \gg 1$ and $G_{out} R_f \ll 1$, resulting in

$$A_{dc} \cong -G_{m1} R_f, \quad (2.4)$$

$$\omega_c \cong \frac{1}{R_f C_L}. \quad (2.5)$$

2.1.3 Input-referred noise

The input-referred noise resistance is given by

$$R_{nin} = \left(\frac{R_f}{G_{m1} R_f - 1} \right)^2 \cdot (G_{n1} + G_{n2}), \quad (2.6)$$

where G_{n1} includes the thermal and flicker noise coming from M_1 , M_{2a} and M_{2b} and $G_{n2} = 1/R_f$.

2.1.3.1 Thermal noise

Assuming that $G_{m1} R_f \gg 1$, the input-referred thermal noise resistance is given by

$$R_{nt} = \frac{\gamma_{n1}}{G_{m1}} \cdot (1 + \eta_{th}) = \frac{\gamma_{neq}}{G_{m1}} \quad (2.7)$$

and the amplifier thermal excess noise factor by

$$\gamma_{neq} = \gamma_{n1} \cdot (1 + \eta_{th}), \quad (2.8)$$

where

$$\eta_{th} = \frac{1}{\gamma_{n1} G_{m1} R_f} + \frac{2\gamma_{n2}}{\gamma_{n1}} \cdot \frac{G_{m2}}{G_{m1}}. \quad (2.9)$$

The first term corresponds to the contribution of the feedback resistance relative to that of M_1 , while the second term corresponds to the contributions of M_{2a} and M_{2b} relative to that of M_1 . We see that the contribution of R_f can be made negligible by making $G_{m1} R_f \gg 1$ (which is actually what was assumed above). The contribution of M_{2a} and M_{2b} can be minimized by making $G_{m1} \gg G_{m2}$. This can be realized by biasing M_1 in weak inversion and M_{2a} - M_{2b} in strong inversion.

2.1.3.2 Flicker noise

The input-referred flicker noise resistance is given by

$$R_{nf} = \frac{\rho_n}{W_1 L_1 f} \cdot (1 + \eta_{fl}), \quad (2.10)$$

with

$$\eta_{fl} = 2 \frac{\rho_p}{\rho_n} \cdot \left(\frac{G_{m2}}{G_{m1}} \right)^2 \cdot \frac{W_1 L_1}{W_2 L_2} \quad (2.11)$$

Finally the corner frequency is given by

$$f_k = \frac{\rho_n}{W_1 L_1} \cdot \frac{G_{m1}}{\gamma_{n1}} \cdot \frac{1 + \eta_{fl}}{1 + \eta_{th}} \quad (2.12)$$

2.2 Design

We now will design the amplifier for the specifications given in Table 2.1.

Table 2.1: Specifications for problem 2.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	10	-
DC gain in dB	$A_{dc,dB} = 20 \log(A_{dc})$	20	dB
Cut-off frequency	f_c	1	MHz
Load capacitance	C_L	1	pF

Assuming that $G_{out} R_f \ll 1$, the DC gain depends only on G_{m1} and R_f and not on G_{out} . On the other hand, for the same assumption $G_{out} R_f \ll 1$, if the load capacitance is set, the cut-off frequency only depends on R_f . We can therefore set the value of the feedback resistor to $R_f = 1/(2\pi f_c C_L) = 159.155 \text{ k}\Omega$, which we round to $R_f = 160 \text{ k}\Omega$.

Assuming that $G_m R_f \gg 1$ and $G_{out} R_f \ll 1$, the transconductance of M_1 is set by the DC gain as $G_{m1} = |A_{dc}|/R_f = 62.500 \text{ }\mu A/V$. The minimum bias current for achieving the required G_{m1} is given by $I_{b,min} = G_{m1} nU_T = 2.056 \text{ }\mu A$. We choose to bias M_1 in weak inversion for maximum current efficiency and therefore set its inversion coefficient to $IC_1 = 0.1$. We can deduce the bias current I_b from the G_m/I_b ratio as $I_b = G_{m1} nU_T/gmsid(IC_1) = 2.244 \text{ }\mu A$, where $gmsid$ is the normalized G_m/I_D function. To account for the parasitic capacitance at the output node, we take some margin on G_{m1} by slightly increasing the bias current to $I_b = 2.5 \text{ }\mu A$. We can deduce I_{spec} and W/L for M_1 as $I_{spec1} = I_b/IC_1 = 25.000 \text{ }\mu A$ and $W/L = 34.965$.

Having increased I_b we can re-estimate $G_{m1} = 69.618 \text{ }\mu A/V$, which is now slightly larger offering some margin.

When choosing L_1 , we need to make sure that the assumption $G_{out} R_f \ll 1$ is fulfilled. Since M_{2a} - M_{2b} will be biased in strong inversion it will result in a long transistor. We can therefore assume that $G_{out} \cong G_{ds1} = I_b/(\lambda L_{eff1})$. Setting $G_{out} R_f$ to $1/10$, we get $L_{eff1} = 533 \text{ nm}$ and $L_1 = 609 \text{ nm}$. We finally get $W_{eff1} = 18.648 \text{ }\mu m$ and $W_1 = 18.609 \text{ }\mu m$.

In order to minimize the contribution of M_{2a} - M_{2b} to the input-referred noise we choose $G_{m2}/G_{m1} = 1/10$ resulting in $G_{m2} = 6.962 \text{ }\mu A/V$. Having G_{m2} and I_b , we can deduce $G_{m2} nU_T/I_b = 0.094$ from which we get M_2 's inversion coefficient $IC_2 = 102.291$ assuming a long-channel device. We can now size M_2 , by first calculating $I_{spec2} = 24 \text{ nA}$ and the aspect ratio $W/L = 0.141$. Choosing $W_2 = W_{min} = 200 \text{ nm}$, we get $L_{eff2} = 1.799 \text{ }\mu m$ and $L_2 = 1.871 \text{ }\mu m$.

The thermal noise excess factors only depend on the inversion coefficients and the slope factors resulting in $\gamma_{n1} = 0.653$ and $\gamma_{n2} = 0.850$. This leads to $\eta_{th} = 0.398$ and $\gamma_{neq} = 0.913$. The input-referred thermal noise resistance and PSD are given by $R_{nt} = 13.118 \text{ k}\Omega$ and $\sqrt{S_{nth}} = 14.739 \text{ nV}/\sqrt{\text{Hz}}$.

The flicker noise PSD at 100 Hz is given by $\sqrt{S_{nf}(100\text{Hz})} = 2.113 \text{ }\mu\text{V}/\sqrt{\text{Hz}}$. The corner frequency is given by $f_k = 2.055 \text{ MHz}$.

2.3 Simulations

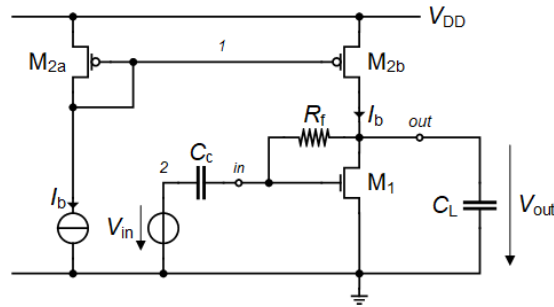


Figure 2.3: Schematic of the gain stage used for simulation.

We can now check whether we get the correct DC gain and bandwidth using ngspice simulations with the schematic shown in Figure 2.3.

The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=2.5u CL=1.0p Rf=160k
.param W1=18.61u L1=609n AD1=5.13e-12 PD1=2.64e-05 W2=200n L2=1.87u AD2=3.97e-13 PD2=2.78e-06
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.5.

Table 2.2: Operating point information.

Node	Voltage
vdd	1.8
in	0.42125
out	0.42125
1	0.48426

The operating information for each transistor can be extracted and are given in Table 1.6 and Table 1.7.

Table 2.3: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D [μA]	I_{spec} [μA]	IC	n	V_{Dsat} [mV]
M1	2.501	25.706	0.097	1.27	120
M2a	2.500	0.017	148.898	1.31	735
M2b	2.501	0.017	148.905	1.31	735

Table 2.4: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} [$\mu A/V$]	G_m [$\mu A/V$]	G_{mb} [$\mu A/V$]	G_{ds} [nA/V]
M1	1.27	88.416	68.588	19.561	266.734
M2a	1.31	7.402	5.324	2.054	24.848
M2b	1.31	7.407	5.327	2.055	24.196

We see that the transconductance of M_1 is slightly higher than the theoretical value because of the margin we have taken on the bias current. The transconductance of M_2 is lower than the theoretical value resulting in a higher DC gain. This is due to the fact that M_2 is biased in very strong inversion with a high value of its gate voltage. This results in a mobility reduction due to the vertical field which results in a reduction of the transconductance. Note that this effect is not accounted for in the sEKV model, but is clearly included in the EKV 2.6 compact model used for the simulations.

The transfer function magnitude and phase are plotted in Figure 2.4, which shows a good fit between the simulation and the theoretical estimation.

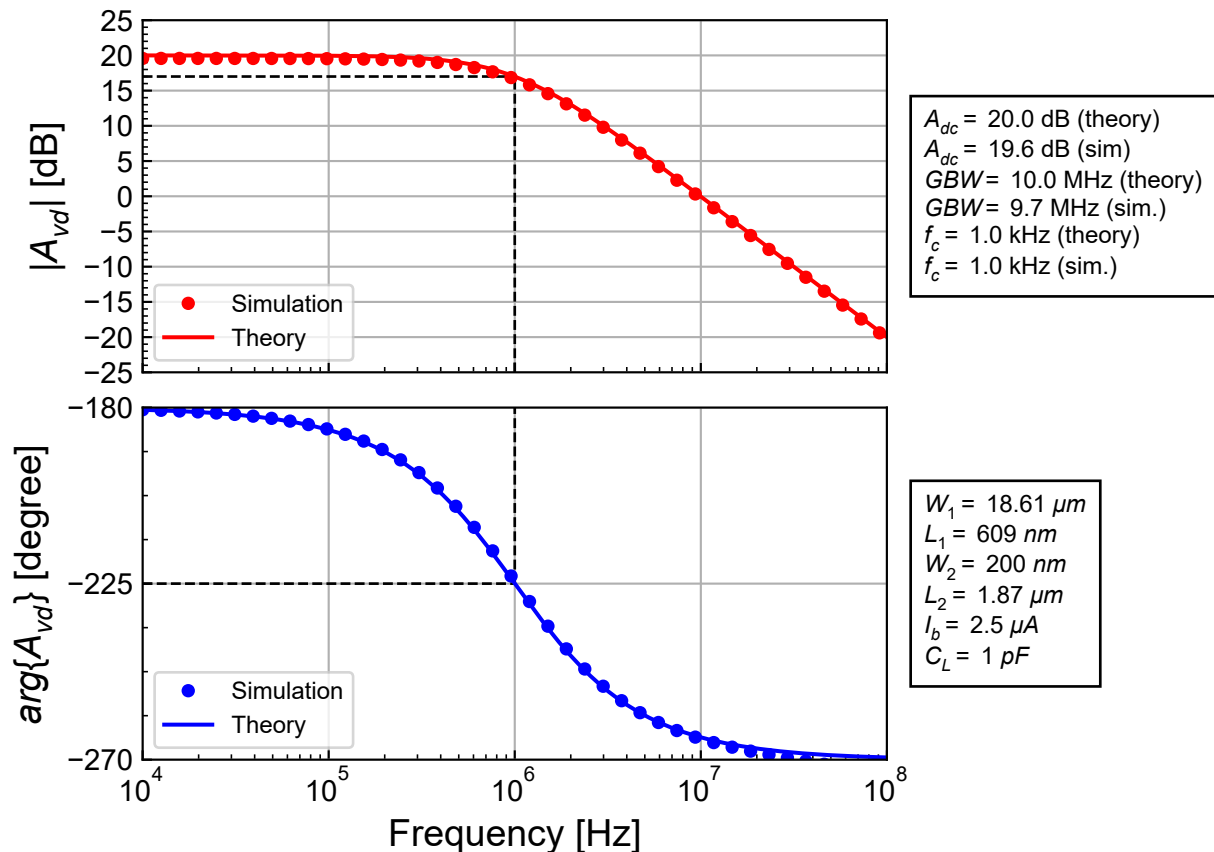


Figure 2.4: Simulated gain response compared to theoretical estimation for the long-channel case.

We can compare the theoretical input-referred noise to that obtained from simulations. The simulation results are presented in Figure 1.5. We see that there is a good agreement for both the white and flicker noise. The simulated white noise is slightly larger due to the lower transconductance G_{m1} corresponding to the simulation (see Table 2.4). The simulated flicker noise is slightly lower than the theoretical estimation due to the larger G_{m1}/G_{m2} ratio corresponding to the simulation $G_{m1}/G_{m2} = 12.9$ instead of 10.0 taken for the design.

i Note

In ngspice it is unfortunately not possible to turn off the noise for a given MOSFET. It is therefore important to generate the raw file with the noise contributions of all devices and then pick the contributions of M_1 and M_2 only, avoiding that of M_3 .

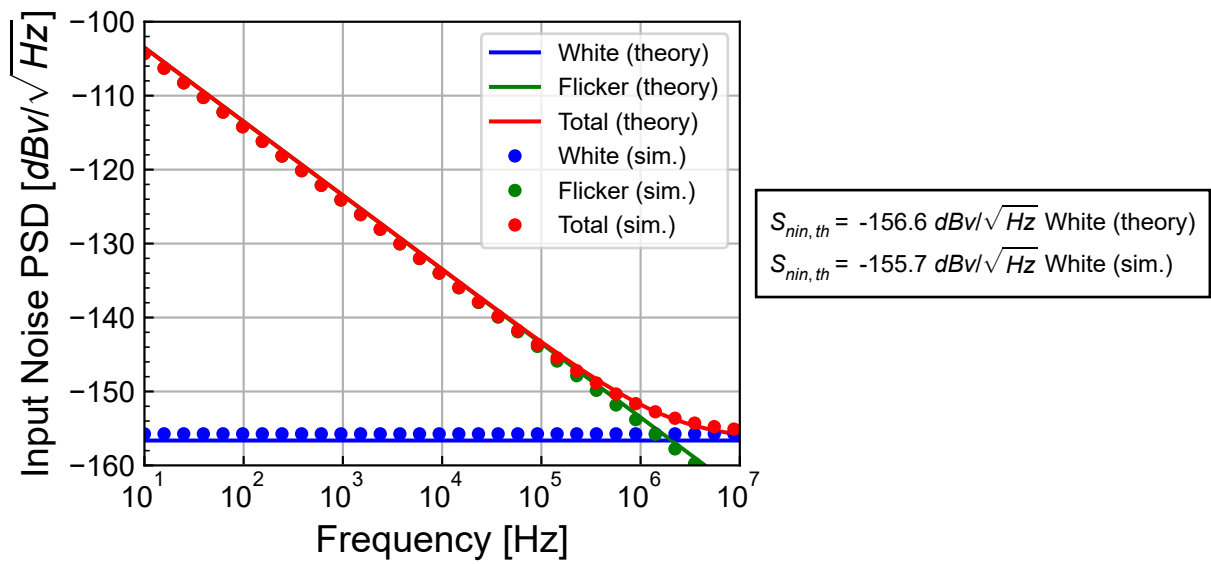


Figure 2.5: Simulated input-referred noise PSD.

3 Conclusion

In this exercise we have analyzed, designed and simulated two basic common-source gain stages for specifications on the DC gain and bandwidth. We have checked by simulations that the designed circuits achieved the desired specifications. This exercise has also shown how important it is to analyze a circuit in order to perform the design and then also to better understand the possible discrepancies appearing between simulation and theoretical estimation.