

# **Fundamentals of Analog VLSI Design**

## **Exercise 3 - Solution**

**Design and Optimization of the Common-source Gain Stage**

Christian Enz (christian.enz@epfl.ch)

01.10.2025

# Table of contents

<b>Introduction</b>	<b>3</b>
<b>1 Problem 1: Imposing the gain-bandwidth product (unity gain frequency)</b>	<b>5</b>
1.1 Analysis . . . . .	5
1.2 Specifications . . . . .	5
1.3 Long-channel case . . . . .	6
1.3.1 Design . . . . .	6
1.3.2 Simulations . . . . .	6
1.4 Short-channel case (including velocity saturation) . . . . .	9
1.4.1 Design . . . . .	9
1.4.2 Simulations . . . . .	10
<b>2 Problem 2: Imposing the power consumption</b>	<b>13</b>
2.1 Specifications . . . . .	13
2.2 Long-channel case . . . . .	13
2.2.1 Design . . . . .	13
2.2.2 Simulations . . . . .	13
2.3 Short-channel case (including velocity saturation) . . . . .	14
2.3.1 Design . . . . .	14
2.3.2 Simulations . . . . .	15
<b>3 Problem 3: Imposing the gain bandwidth product and the current budget</b>	<b>17</b>
3.1 Specifications . . . . .	17
3.2 Design . . . . .	17
3.3 Simulations . . . . .	17
<b>4 Problem 4: Imposing the input-referred noise</b>	<b>19</b>
4.1 Specifications . . . . .	19
4.2 Design . . . . .	19
4.3 Simulations . . . . .	20
<b>5 Problem 5: Minimum current for a given gain-bandwidth product with self-loading</b>	<b>22</b>
5.1 Specifications . . . . .	23
5.2 Design . . . . .	23
5.3 Simulations . . . . .	24
<b>6 Problem 6: Minimum current for a given DC gain and gain-bandwidth product with self-loading</b>	<b>28</b>
6.1 Specifications . . . . .	29
6.2 Design . . . . .	29
6.3 Simulations . . . . .	30
<b>7 Conclusion</b>	<b>32</b>
<b>References</b>	<b>33</b>

# Introduction

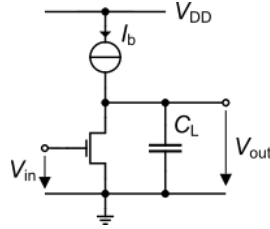


Figure 1: Common-source (CS) gain stage.

In this exercise we want to apply the  $G_m/I_D$  design methodology using the inversion coefficient  $IC$  to the simple common source (CS) amplifier shown in Figure 1 for various specifications. For the design we assume a generic 180 nm bulk CMOS process. The physical parameters are given in Table 1, the global process parameters in Table 2 and finally the MOSFET parameters in Table 3.

## ! Important

For this process, the transistor dimensions are rounded to 10nm.

Table 1: Physical parameters

Parameter	Value	Unit
$T$	300	$K$
$U_T$	25.875	$mV$

Table 2: Global process parameters

Parameter	Value	Unit
$V_{DD}$	1.8	$V$
$C_{ox}$	8.443	$\frac{fF}{\mu m^2}$
$H_{dif}$	200	$nm$
$W_{min}$	200	$nm$
$L_{min}$	180	$nm$

Table 3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
$n$	1.27	1.31	-
$I_{spec\Box}$	715	173	$nA$
$V_{T0}$	0.455	0.445	$V$
$L_{sat}$	26	36	$nm$
$\lambda$	15	20	$\frac{V}{\mu m}$

Table 3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
Overlap capacitances parameters			
$C_{GD0}$	0.366	0.329	$\frac{fF}{\mu m}$
$C_{GS0}$	0.366	0.329	$\frac{fF}{\mu m}$
$C_{GB0}$	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
$C_J$	1	1.121	$\frac{fF}{\mu m^2}$
$C_{JSW}$	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
$K_F$	8.1e-24	6.8e-23	$J$
$AF$	1	1	-
$\rho$	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
$A_{VT}$	5	5	$mV \cdot \mu m$
$A_\beta$	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
$R_{sh}$	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
$\Delta W$	39	54	$nm$
$\Delta L$	-76	-72	$nm$

# 1 Problem 1: Imposing the gain-bandwidth product (unity gain frequency)

In this first example we will design the CS gain stage shown in Figure 1 for the specifications at room temperature given in Table 1.1 by imposing the inversions coefficient and the load capacitance.

## 1.1 Analysis

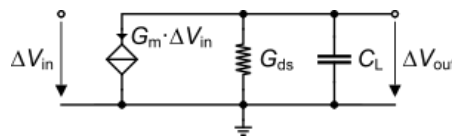


Figure 1.1: Small-signal schematic of the common-source (CS).

The small-signal schematic of the CS amplifier is shown in Figure 1.1. The transfer function is given by

$$H(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A_{dc}}{1 + \frac{s}{\omega_c}}, \quad (1.1)$$

where  $A_{dc} = -G_m/G_{ds}$  is the dc gain and  $\omega_c = G_{ds}/C_L$  the cut-off frequency.

The magnitude of the frequency response is then given by

$$|H(\omega)| = \frac{|A_{dc}|}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^2}} \approx \frac{\omega_u}{\omega} \quad (1.2)$$

for  $\omega_c \ll \omega$  where

$$\omega_u = |A_{dc}| \cdot \omega_c = \frac{G_m}{C_L} \quad (1.3)$$

is the unity-gain frequency or gain-bandwidth product.

## 1.2 Specifications

The specifications for Problem 1 are given in Table 1.1.

Table 1.1: Specifications for problem 1.

Specification	Symbol	Value	Unit
Gain-bandwidth product	$GBW$	10	$MHz$
Inversion coefficient	$IC$	1	-
Load capacitance	$C_L$	1	$pF$

## 1.3 Long-channel case

### 1.3.1 Design

For the long-channel case, we take  $L = 1 \mu\text{m}$  which corresponds to an effective length  $L_{eff} = 924 \text{ nm}$ .

The gain-bandwidth product  $GBW$  and the load capacitance  $C_L$  set the required transconductance as  $G_m = 62.832 \mu\text{A}/\text{V}$ . Assuming a long-channel transistor we can neglect the effect of velocity saturation and calculate the current efficiency for the chosen inversion coefficient as  $G_m nU_T/I_D = 0.618$ , from which we get  $I_b = 3.344 \mu\text{A}$ . From the bias current and the inversion coefficient we get the specific current as  $I_{spec} = 3.344 \mu\text{A}$  and the aspect ratio  $W/L = 4.677$ . Knowing the length, we get the effective width  $W_{eff} = 4.319 \mu\text{m}$  and drawn width  $W = 4.28 \mu\text{m}$ .

We can check what is the resulting dc gain by estimating the output conductance  $G_{ds} = I_b/(\lambda_n L) = 0.241 \mu\text{A}/\text{V}$ . The resulting DC gain is then  $A_{dc} = G_m/G_{ds} = -260.391$  or 48.313 dB.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct  $C_L$  to get the correct  $GBW$ . This results in  $C_{DBJ} = 3.6 \text{ fF}$ ,  $C_{GD} = 1.6 \text{ fF}$ ,  $C_D = 5.2 \text{ fF}$ . To account for the parasitic capacitance at the drain  $C_D = 5.2 \text{ fF}$ , we need to reduce the load capacitance. The effective load capacitance that needs to be added is then  $C_{L0} = 0.995 \text{ pF}$  instead of  $C_L = 1.000 \text{ pF}$ .

### 1.3.2 Simulations

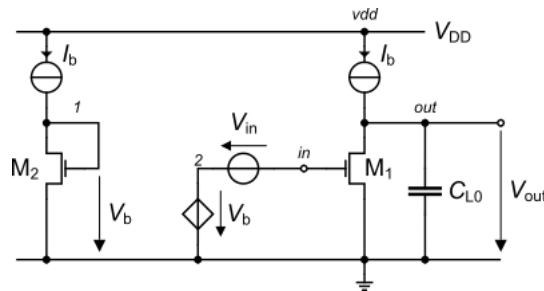


Figure 1.2: Schematic of the common-source (CS) gain stage used for simulation.

We can now check whether we get the correct  $GBW$  and DC gain using ngspice simulations with the schematic shown in Figure 1.2, where transistor  $M_2$  is used to correctly bias the gate of the CS transistor  $M_1$  so that it draws the desired bias current  $I_b$ .

The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=3.344u
.param CL=994.80f W=4.28u L=1.00u AD=1.73e-12 PD=9.44e-06
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.2.

Table 1.2: Operating point information.

Node	Voltage
vdd	1.8
in	0.508564

Table 1.2: Operating point information.

Node	Voltage
out	0.508564
1	0.508564
2	0.508564

The operating information for each transistor can be extracted and are given in Table 1.3 and Table 1.4.

Table 1.3: Operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D$ [ $\mu A$ ]	$I_{spec}$ [ $\mu A$ ]	$IC$	$n$	$V_{Dsat}$ [ $mV$ ]
M1	3.344	3.277	1.023	1.27	156
M2	3.344	3.277	1.023	1.27	156

Table 1.4: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$n$	$G_{ms}$ [ $\mu A/V$ ]	$G_m$ [ $\mu A/V$ ]	$G_{mb}$ [ $\mu A/V$ ]	$G_{ds}$ [ $\mu A/V$ ]
M1	1.27	78.616	61.163	17.292	0.160
M2	1.27	78.616	61.163	17.292	0.160

We see that the simulated transconductance of  $M_1$   $G_m = 61.163 \mu A/V$  is slightly lower than the theoretical estimation  $G_m = 62.832 \mu A/V$ .

We can now proceed with the simulation of the transfer function which is shown in Figure 1.3.

From Figure 1.3, we see that the gain-bandwidth product  $GBW = 9.7 MHz$  is slightly lower than the specifications  $GBW = 10 MHz$  despite we have accounted for the junction capacitance at the output. This comes from the fact that the simulated transconductance  $G_m = 61.163 \mu A/V$  is slightly lower than the theoretical estimation  $G_m = 62.832 \mu A/V$ .

We also see that there is some discrepancy of the phase at high frequency (above the  $GBW$ ). This coming from the gate-to-drain capacitance (the overla capacitance  $C_{GD0}$ ) which introduces a positive zero. We can add this zero in the theoretical transfer leading to the transfer function magnitude and phase are plotted in Figure 1.4. We now see that we have a better fit at high frequency (dashed blue line). The gate-to-drain capacitance seems to be larger.

If we want to meet the specifications we can slightly increase the bias current to  $I_b = 3.5 \mu A$ . The transfer function is now given in Figure 1.5. We see that we are now right on spec.

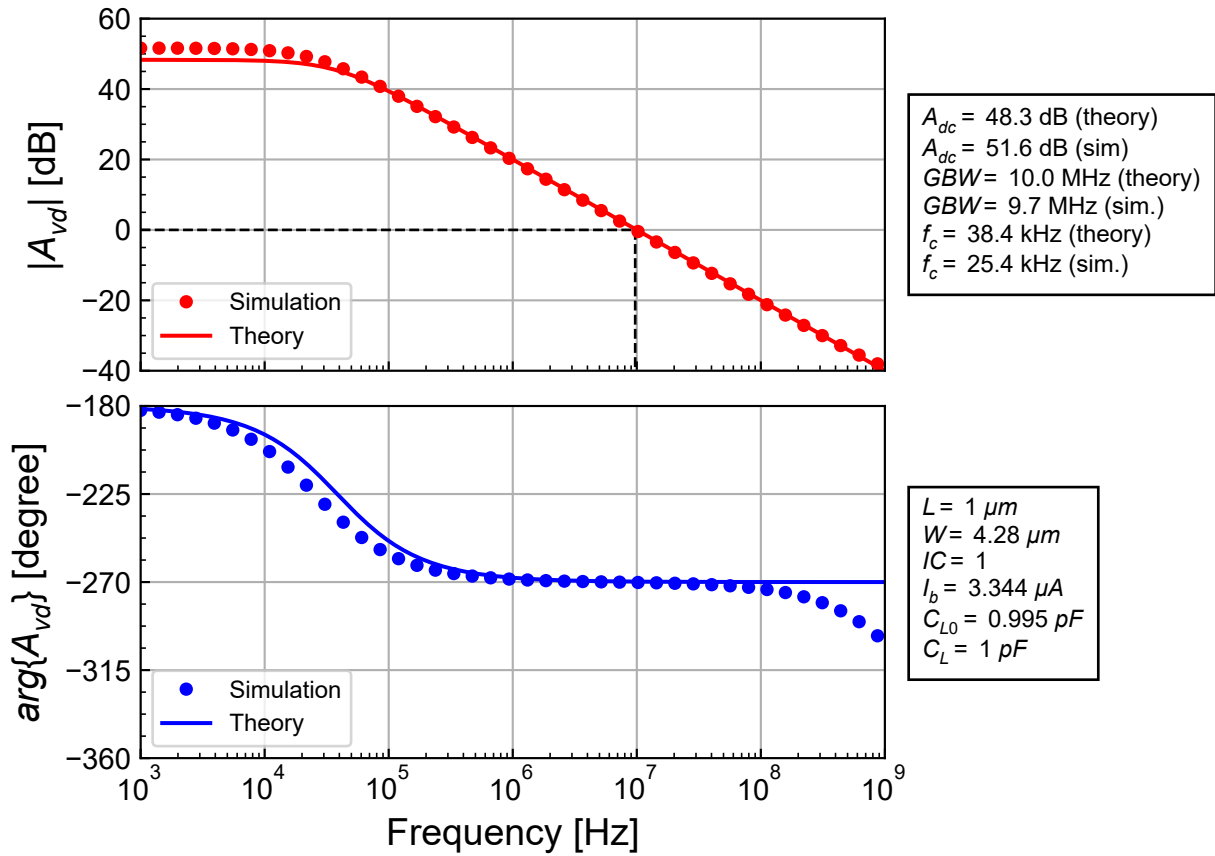


Figure 1.3: Simulated gain response compared to theoretical estimation for the long-channel case.

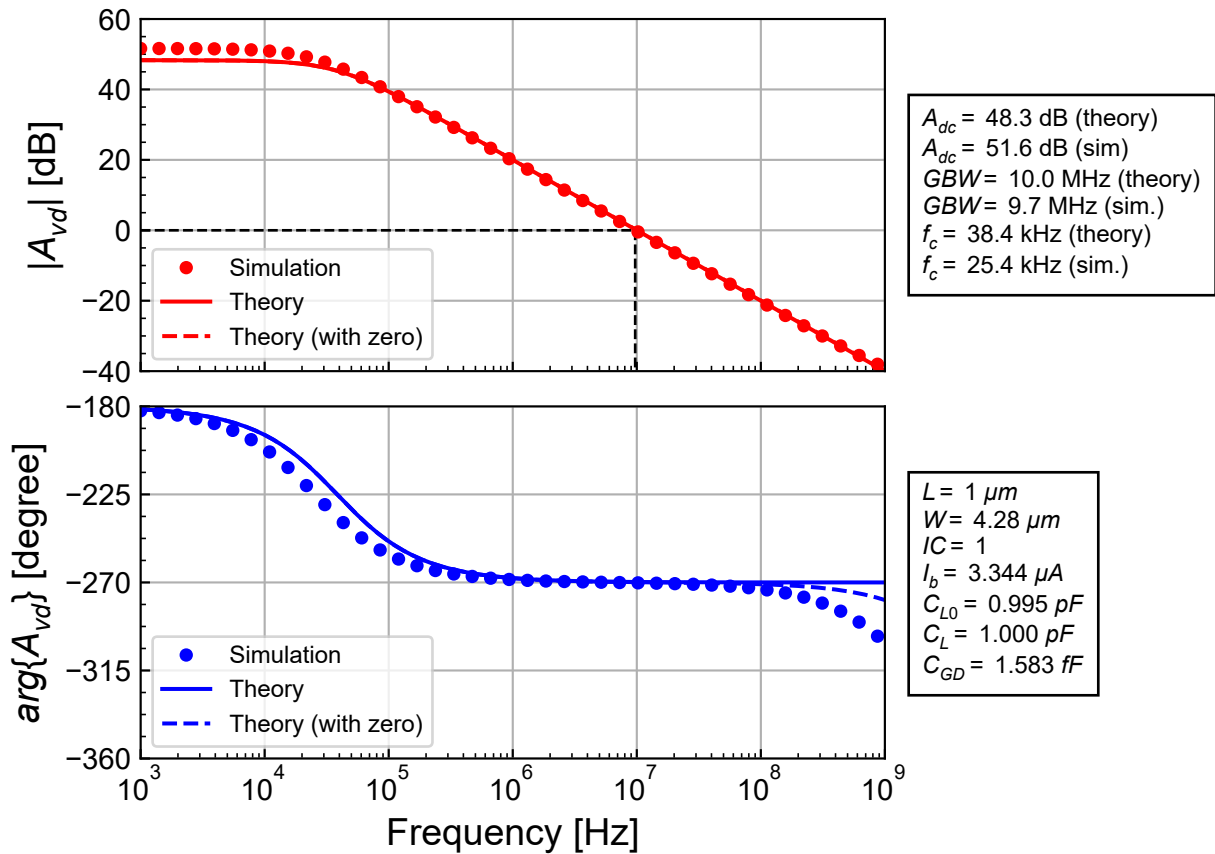


Figure 1.4: Simulated gain response compared to theoretical estimation for the long-channel case.

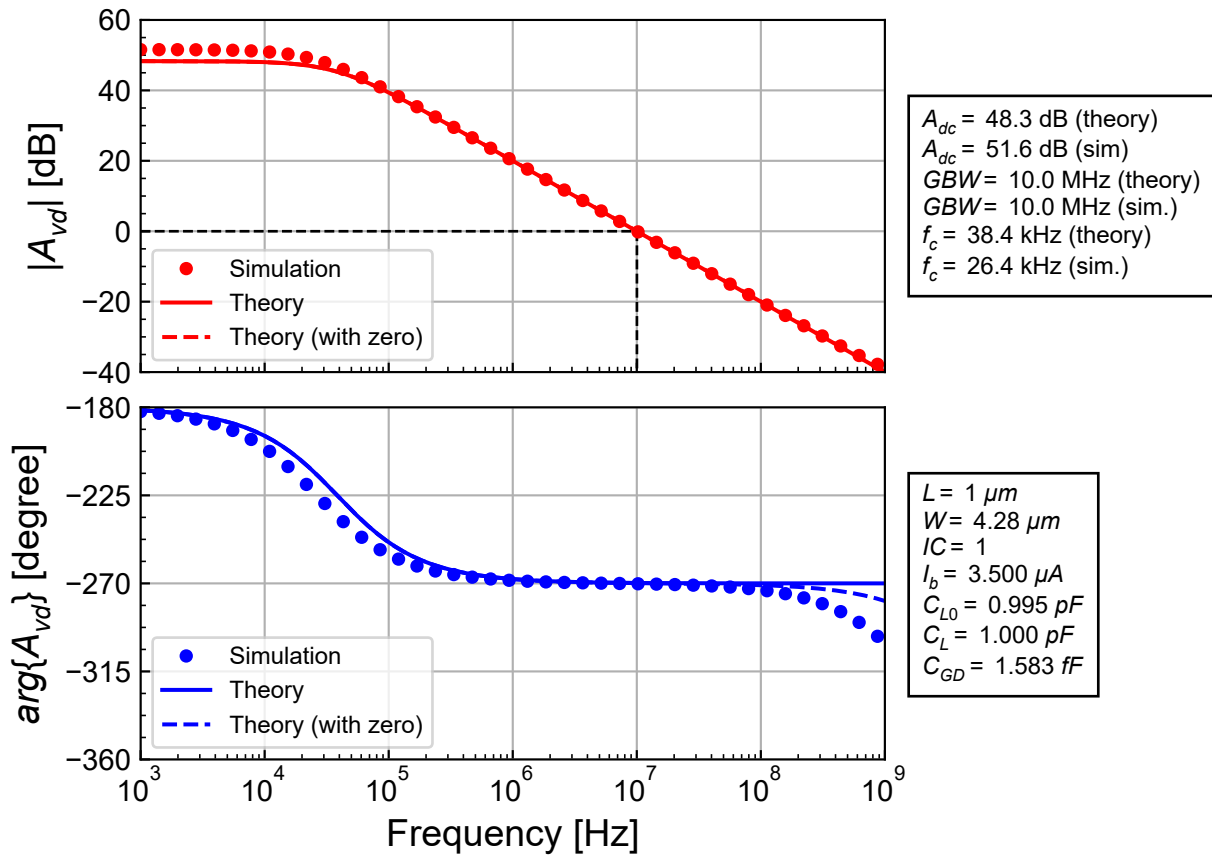


Figure 1.5: Simulated gain response compared to theoretical estimation for the long-channel case.

## 1.4 Short-channel case (including velocity saturation)

### 1.4.1 Design

The required transconductance hasn't changed because it is set by the desired gain-bandwidth product and load capacitance  $G_m = 62.832 \mu A/V$ .

For the short-channel case we will use the shortest channel length for this technology, namely  $L = 0.18 \mu m$  corresponding to an effective length  $L_{eff} = 104 nm$ . The velocity parameter for the chosen length is then given by  $\lambda_c = L_{satn}/L_{eff} = 0.250$ . The procedure is then the same: we first get the bias current from the current efficiency but including the effect of velocity saturation  $G_m nU_T/I_D = 0.606$ . We see that the current efficiency  $G_m nU_T/I_D$  is only slightly smaller than for the long-channel case due to velocity saturation. The bias current is then given by  $I_b = 3.410 \mu A$ . Despite we use a shorter channel-length, the required bias current is about the same than the one from the long-channel case. This is simply due to the fact the effect of velocity saturation is small in moderate and hence has little effect on the current efficiency.

From the bias current and the inversion coefficient we get the specific current as  $I_{spec} = 3.410 \mu A$  and the aspect ratio  $W_{eff}/L_{eff} = 4.770$ . For the chosen length we get the effective width  $W_{eff} = 0.499 \mu m$  and drawn width  $W = 0.46 \mu m$ .

We can check what is the resulting dc gain by estimating the output conductance  $G_{ds} = I_b/(\lambda_n L_{eff}) = 2.186 \mu A/V$ . The DC gain is now  $A_{dc} = -28.740$  or  $29.170 dB$ , which, as expected, is significantly lower than for the long-channel case.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct  $C_L$  to get the correct  $GBW$ . This results in  $C_{DBJ} = 1 fF$ ,  $C_{GD} =$

0.183  $fF$ ,  $C_D = 1 fF$ . The effective load capacitance that needs to be added is then  $C_{L0} = 0.999 pF$ .

### 1.4.2 Simulations

We can check whether we get the correct GBW and dc gain using simulations with the following values of the parameters:

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.5.

Table 1.5: Operating point information.

Node	Voltage
vdd	1.8
in	0.511076
out	0.511076
1	0.511076
2	0.511076

The operating information for each transistor can be extracted and are given in Table 1.6 and Table 1.7.

Table 1.6: Operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D [\mu A]$	$I_{spec} [\mu A]$	$IC$	$n$	$V_{Dsat} [mV]$
M1	3.500	3.273	1.072	1.27	157
M2	3.500	3.273	1.072	1.27	157

Table 1.7: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$n$	$G_{ms} [\mu A/V]$	$G_m [\mu A/V]$	$G_{mb} [\mu A/V]$	$G_{ds} [\mu A/V]$
M1	1.27	81.190	63.169	17.855	0.167
M2	1.27	81.190	63.169	17.855	0.167

We see that the simulated transconductance of M<sub>1</sub>  $G_m = 63.169 \mu A/V$  is slightly larger than the theoretical estimation  $G_m = 62.832 \mu A/V$ .

```
.param VDD=1.8 Ib=3.410u
.param CL=999f W=0.46u L=0.18u AD=2.00e-13 PD=1.80e-06
```

The transfer function magnitude and phase are plotted in Figure 1.6, which shows a reasonable fit between the simulation and the theoretical estimation. The simulated gain-bandwidth product  $GBW$  is slightly lower than target and the simulated DC gain is slightly larger than the theoretical estimation.

From Figure 1.6, we see that the simulated DC gain is slightly larger than the theoretical estimation. We also see that the gain-bandwidth product specs is not met. If we want to meet the specifications we can slightly increase the bias current to  $I_b = 4.0 \mu A$ . The transfer function is now given in Figure 1.7. We see that we are now right on spec.

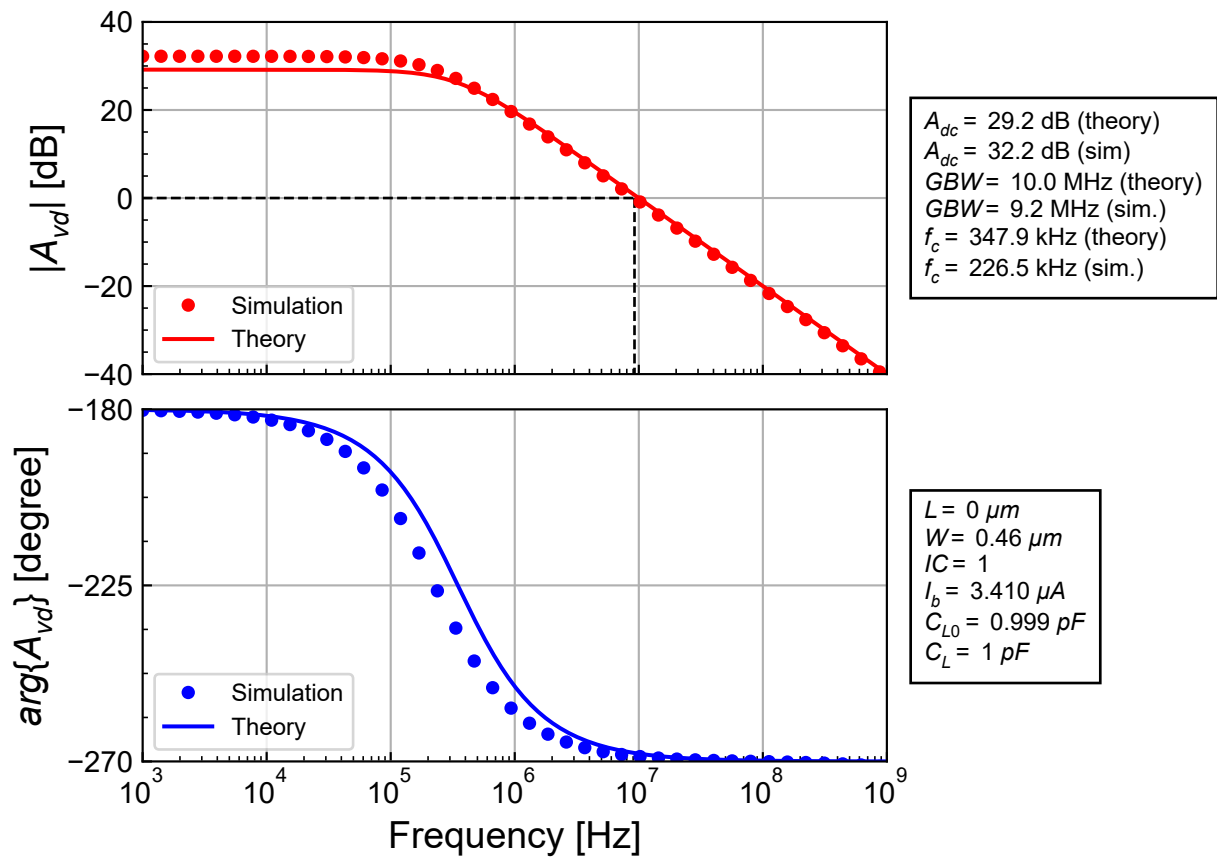


Figure 1.6: Simulated gain response compared to theoretical estimation for the short-channel case.

#### **i** Note

We also see that for the short-channel case, we don't see the zero which has moved to much higher frequency. This is due to the much smaller transistor width which significantly reduces the gate-to-drain capacitance.

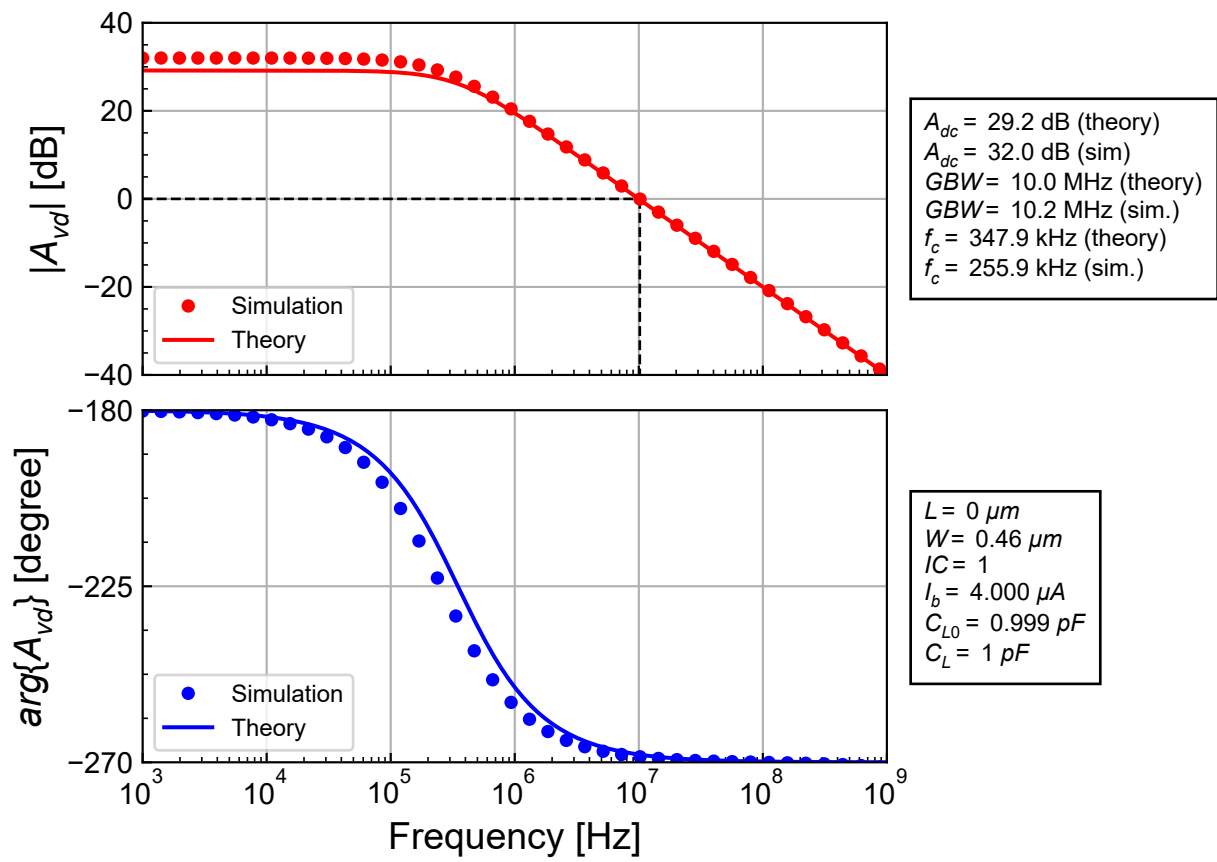


Figure 1.7: Simulated gain response compared to theoretical estimation for the short-channel case.

## 2 Problem 2: Imposing the power consumption

### 2.1 Specifications

We now impose the power consumption, the inversion coefficient and the load capacitance according to the specifications given in Table 2.1.

Table 2.1: Specifications for problem 2.

Specification	Symbol	Value	Unit
Power consumption	$P$	20	$\mu W$
Inversion coefficient	$IC$	1	-
Load capacitance	$C_L$	1	$pF$

### 2.2 Long-channel case

#### 2.2.1 Design

For the long-channel case, we choose  $L = 1 \mu m$  which corresponds to an effective width  $L_{eff} = 0.924 \mu m$ . The maximum available current is directly given by  $I_b = P/V_{DD} = 11.111 \mu A$ . Since the inversion coefficient is chosen as  $IC = 1$ , we get the specific current as  $I_{spec} = 11.111 \mu A$ . The normalized transconductance is the given by the chosen inversion coefficient as  $g_{ms} = G_{ms}/G_{spec} = 0.618$ , from which we derive the transconductance  $G_m = 208.747 \mu A/V$  and the gain-bandwidth product for the given load capacitance  $GBW = G_m/C_L = 33.223 MHz$ . The aspect ratio is then given by  $W_{eff}/L_{eff} = 15.540$ . The effective width  $W_{eff} = 14.359 \mu m$  and drawn width  $W = 14.32 \mu m$ .

We can calculate the dc gain by first estimating the output conductance  $G_{ds} = I_b/(\lambda_n L_{eff}) = 0.802 \mu A/V$ . The dc gain is then given by  $A_{dc} = G_m/G_{ds} = -260.391$  or  $48.313 dB$ .

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct  $C_L$  to get the correct  $GBW$ . This results in  $C_{DBJ} = 12 fF$ ,  $C_{GD} = 5.248 fF$ ,  $C_D = 17 fF$ . The effective load capacitance that needs to be added is then  $C_{L0} = 0.983 pF$ .

#### 2.2.2 Simulations

We can now check whether we get the correct  $GBW$  and  $DC$  gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=11.111u
.param CL=983.10f W=14.32u L=1.00u AD=5.74e-12 PD=2.95e-05
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.2.

Table 2.2: Operating point information.

Node	Voltage
vdd	1.8
in	0.508531
out	0.508531
1	0.508531
2	0.508531

The operating information for each transistor can be extracted and are given in Table 1.3 and Table 1.4.

Table 2.3: Operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D$ [ $\mu A$ ]	$I_{spec}$ [ $\mu A$ ]	$IC$	$n$	$V_{Dsat}$ [ $mV$ ]
M1	11.111	10.895	1.022	1.27	156
M2	11.111	10.895	1.022	1.27	156

Table 2.4: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$n$	$G_{ms}$ [ $\mu A/V$ ]	$G_m$ [ $\mu A/V$ ]	$G_{mb}$ [ $\mu A/V$ ]	$G_{ds}$ [ $\mu A/V$ ]
M1	1.27	261.256	203.257	57.466	0.533
M2	1.27	261.256	203.257	57.466	0.533

We see that the simulated transconductance of M<sub>1</sub>  $G_m = 203.257 \mu A/V$  is slightly lower than the theoretical estimation  $G_m = 208.747 \mu A/V$ .

The transfer function magnitude and phase are plotted in Figure 1.4, which shows a good fit between the simulation and the theoretical estimation.

## 2.3 Short-channel case (including velocity saturation)

### 2.3.1 Design

For the short-channel case we will use the shortest channel length for this technology, namely  $L = 180 \text{ nm}$ . The velocity parameter for the chosen length is then given by  $\lambda_c = L_{satn}/L = 0.250$ . The procedure is basically the same except that we now need to account for velocity saturation in the estimation of the transconductance. Since the inversion coefficient is chosen as  $IC = 1$ , we get the specific current as  $I_{spec} = 11.111 \mu A$ . The normalized transconductance is the given by the chosen inversion coefficient as  $g_{ms} = G_{ms}/G_{spec} = 0.606$ , from which we derive the transconductance  $G_m = 0.205 \text{ mA/V}$  and the gain-bandwidth product for the given load capacitance  $GBW = G_m/C_L = 32.580 \text{ MHz}$ . The aspect ratio is then given by  $W_{eff}/L_{eff} = 15.540$ . The effective width  $W_{eff} = 1.619 \mu m$  and drawn width  $W = 1.58 \mu m$ .

We can calculate the dc gain by first estimating the output conductance  $G_{ds} = I_b/(\lambda_n L_{eff}) = 7.123 \mu A/V$ . The dc gain is then given by  $A_{dc} = G_m/G_{ds} = -28.740$  or  $29.170 \text{ dB}$ .

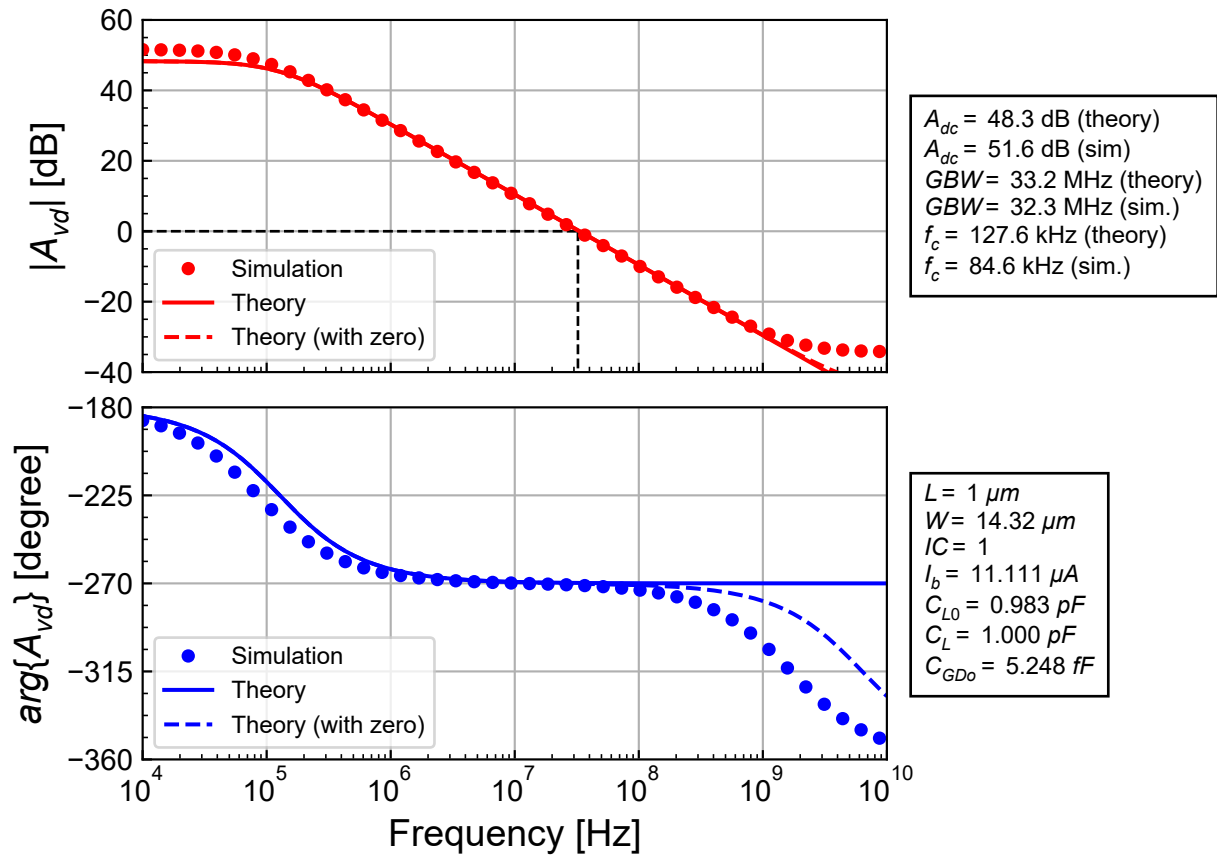


Figure 2.1: Simulated gain response compared to theoretical estimation for the long-channel case.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct  $C_L$  to get the correct  $GBW$ . This results in  $C_{DBJ} = 1.5 \text{ fF}$ ,  $C_{GD} = 0.579 \text{ fF}$ ,  $C_D = 2.0 \text{ fF}$ . The effective load capacitance that needs to be added is then  $C_{L0} = 0.998 \text{ pF}$ .

### 2.3.2 Simulations

We can check whether we get the correct  $GBW$  and dc gain using simulations with the following values of the parameters:

```
.param VDD=1.8 Ib=11.111u
.param CL=997.97f W=1.58u L=0.18u AD=6.48e-13 PD=4.04e-06
```

The transfer function magnitude and phase are plotted in Figure 2.2, which shows a reasonable fit between the simulation and the theoretical estimation.

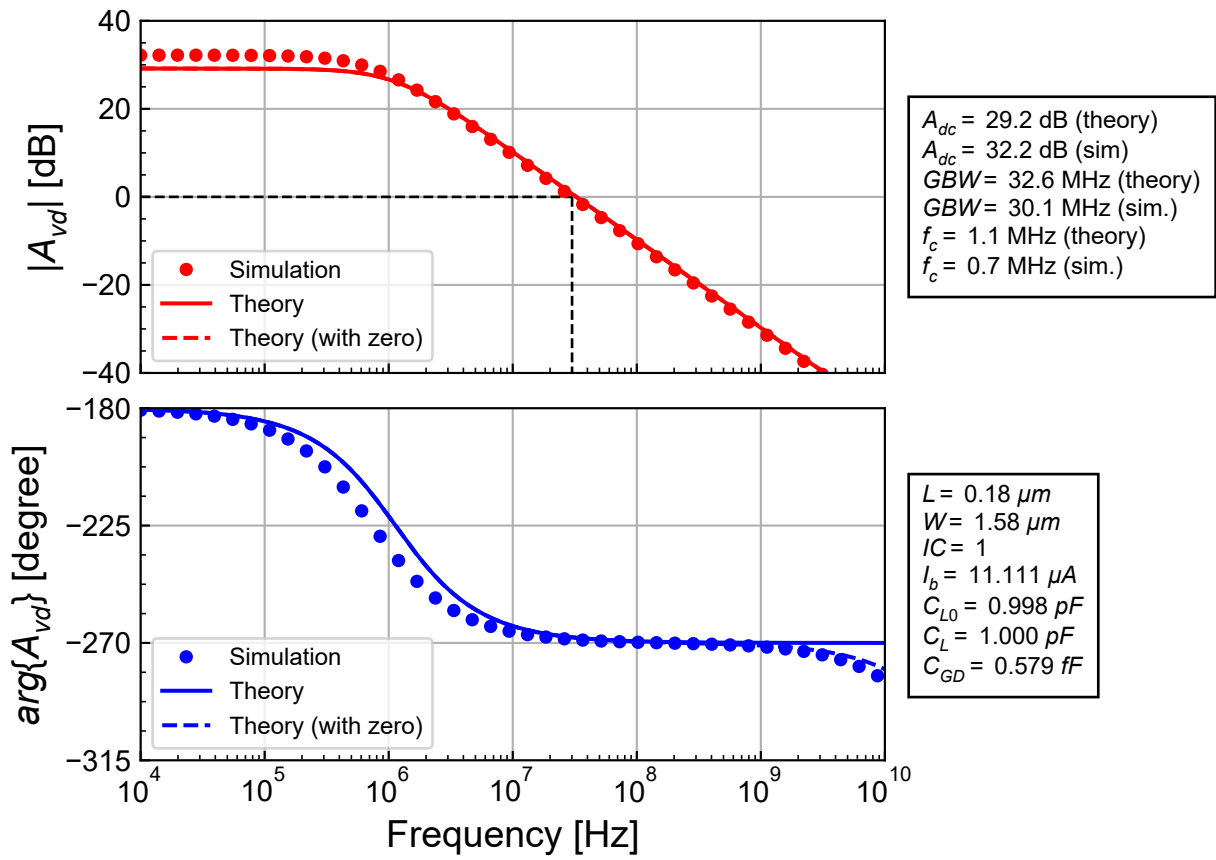


Figure 2.2: Simulated gain response compared to theoretical estimation for the short-channel case.

## 3 Problem 3: Imposing the gain bandwidth product and the current budget

### 3.1 Specifications

We now don't impose the inversion coefficient but the gain bandwidth product and the current budget. We keep the same load capacitance and consider a long channel. The specifications are now given in Table 3.1.

Table 3.1: Specifications for problem 3.

Specification	Symbol	Value	Unit
Gain-bandwidth product	$GBW$	1	$MHz$
Bias current	$I_b$	400	$nA$
Load capacitance	$C_L$	1	$pF$
Transistor length	$L$	1	$\mu m$

### 3.2 Design

We first get the transconductance required to achieve the target gain-bandwidth product as  $G_m = 6.283 \mu A/V$ . Knowing the bias current and the transconductance we can calculate the current efficiency as  $G_m nU_T/I_D = 0.517$ , from which we can derive the corresponding inversion coefficient  $IC = 1.810$ . We see that we are in the moderate inversion region. The specific current is then given by  $I_{spec} = 221 nA$ , the aspect ratio by  $W_{eff}/L_{eff} = 0.309$ , the effective width by  $W_{eff} = 289 nm$  and finally the drawn width  $W = 250 nm$ .

We can calculate the dc gain by first estimating the output conductance  $G_{ds} = I_b/(\lambda_n L_{eff}) = 28.860 nA/V$ . The dc gain is then given by  $A_{dc} = G_m/G_{ds} = -217.712$  or  $46.758 dB$ .

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct  $C_L$  to get the correct  $GBW$ . This results in  $C_{DBJ} = 391.2 aF$ ,  $C_{GD} = 105.918 aF$ ,  $C_D = 497.1 aF$ . The effective load capacitance that needs to be added is then  $C_{L0} = 999.503 fF$ . We observe that the parasitic capacitance at the drain are negligible compared to the load capacitance.

### 3.3 Simulations

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=0.400u
.param CL=999.50f W=0.25u L=1.00u AD=1.16e-13 PD=1.38e-06
```

The transfer function magnitude and phase are plotted in Figure 1.4, which shows a good fit between the simulation and the theoretical estimation.

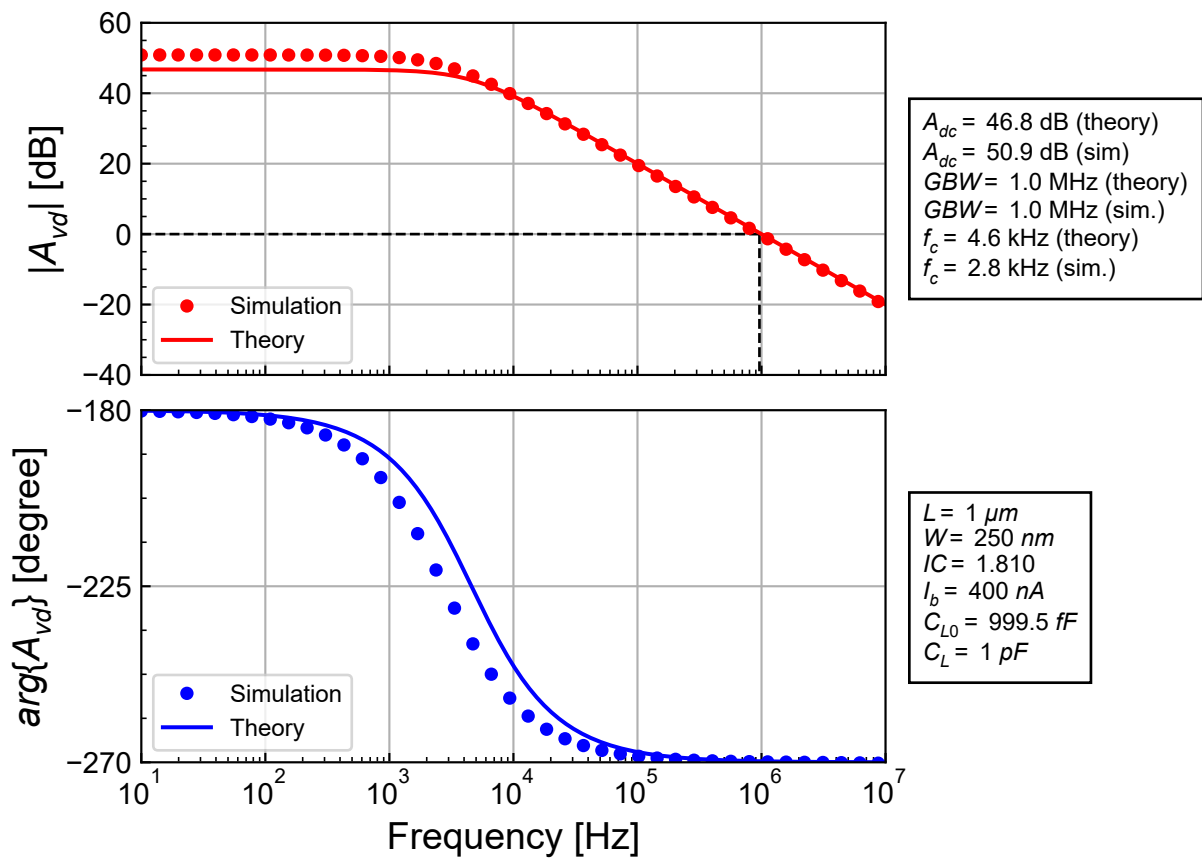


Figure 3.1: Simulated gain response compared to theoretical estimation for the long-channel case.

## 4 Problem 4: Imposing the input-referred noise

### 4.1 Specifications

In this example, we impose the input-referred noise by setting the white noise and the corner frequency. The specifications are given in Table 4.1.

Table 4.1: Specifications for problem 4.

Specification	Symbol	Value	Unit
Corner frequency	$f_k$	100	$kHz$
Input referred white PSD	$\sqrt{S_{n,th}}$	30	$\frac{nV}{\sqrt{Hz}}$
	$10 \log(S_{n,th})$	-150.46	$\frac{dBV}{\sqrt{Hz}}$
Inversion coefficient	$IC$	1	-
Load capacitance	$C_L$	1	$pF$

### 4.2 Design

We need the flicker noise parameter  $K_f = 8.100e-24 J$  and the oxide capacitance per unit area  $C_{ox} = 8.443 fF/\mu m^2$ .

Before the transconductance is derived from the thermal noise specification, we need to know the thermal noise excess factor  $\gamma_n$  for the given  $IC$  (we assume long-channel case) which is  $\gamma_n = 0.717$ . The transconductance is then given by  $G_m = 4kT\gamma_n/S_{nin,th} = 13.186 \mu A/V$ , where  $S_{nin,th} = V_{nin,th}^2$ . Once we have the transconductance, the procedure is similar to the previous one.

Having imposed the inversion coefficient  $IC = 1$ , we can deduce the current efficiency as  $G_m nU_T/I_D = 0.618$ . By definition of the current efficiency we can get the corresponding bias current  $I_b = 702 nA$ . The specific current and aspect ratio are then given by  $I_{spec} = 702 nA$  and  $W_{eff}/L_{eff} = 0.982$ .

The corner frequency will actually set the flicker noise which is inversely proportional to the gate area. We can therefore calculate the gate area from the flicker noise remembering that the corner frequency is the frequency at which the flicker noise becomes equal to the white noise. The gate area is obtained as  $W_{eff} L_{eff} = 10.660 \mu m^2$ . Knowing the  $W/L$  ratio we can calculate the effective width and length as  $W_{eff} = 3.235 \mu m$  and  $L_{eff} = 3.295 \mu m$ . The drawn width and length follow as  $W = 3.20 \mu m$  and  $L = 3.37 \mu m$ .

The gain-bandwidth product is given by  $GBW = 2.099 MHz$ .

We can calculate the dc gain by first estimating the output conductance  $G_{ds} = I_b/(\lambda_n L_{eff}) = 0.014 \mu A/V$ . The dc gain is then given by  $A_{dc} = G_m/G_{ds} = -928.687$  or  $59.357 dB$ .

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct  $C_L$  to get the correct  $GBW$ . This results in  $C_{DBJ} = 2.7 fF$ ,  $C_{GD} = 1.186 fF$ ,  $C_D = 3.9 fF$ . The effective load capacitance that needs to be added is then  $C_{L0} = 0.996 pF$ .

### 4.3 Simulations

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=702n
.param CL=996.07f W=3.20u L=3.37u AD=1.29e-12 PD=7.27e-06
```

The transfer function magnitude and phase are plotted in Figure 4.2, which shows a good fit between the simulation and the theoretical estimation.

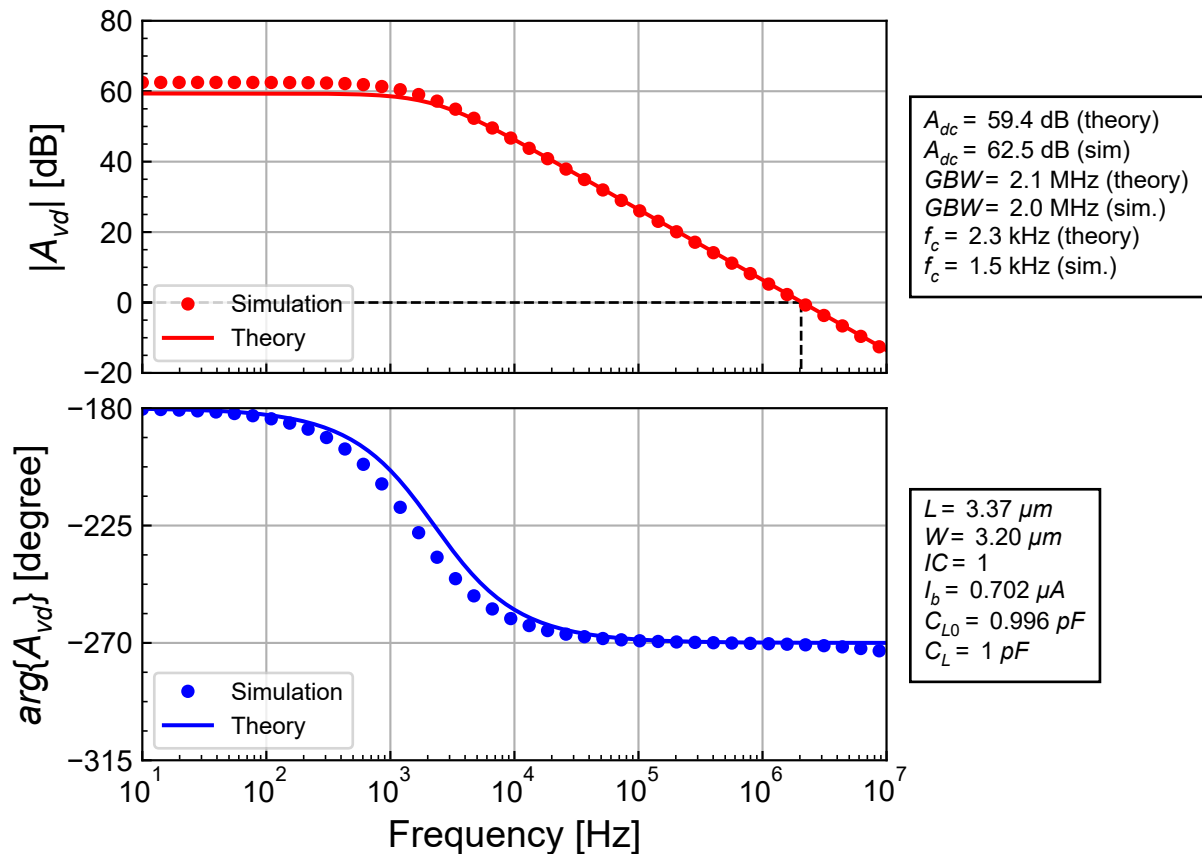


Figure 4.1: Simulated gain response compared to theoretical estimation for the long-channel case.

We can now check the input-referred noise PSD which is plotted in Figure 4.2. We can see that simulation perfectly matches the theoretical estimation.

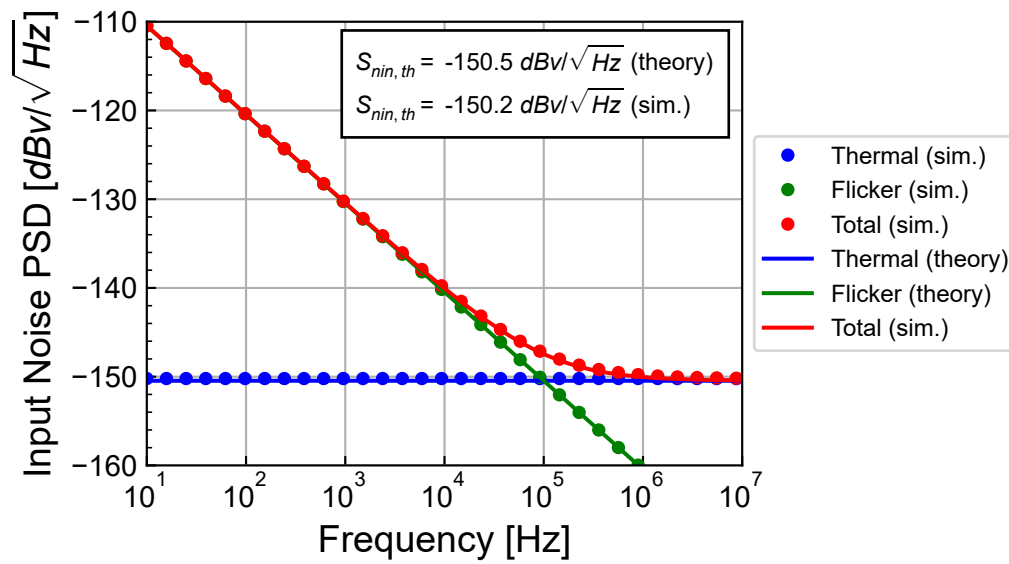


Figure 4.2: Simulated input-referred noise PSD compared to theoretical estimation.

## References

- [1] C. Enz, “Common-source Open-loop Optimization.” [https://github.com/chrisenz/Analog-Circuit-Design/blob/main/Amplifiers/Basic/CS%20OL%20Optimization/CS\\_OL\\_optimization.pdf](https://github.com/chrisenz/Analog-Circuit-Design/blob/main/Amplifiers/Basic/CS%20OL%20Optimization/CS_OL_optimization.pdf), 2025.
- [2] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design*, 1st ed. John Wiley, 2006.