Fundamentals of Analog VLSI Design
Exercise 3 - Solution

Design and Optimization of the Common-source Gain Stage

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Introduction

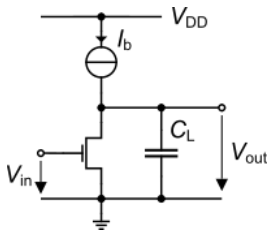

Figure 1: Common-source (CS) gain stage.

In this exercise we want to apply the G_m/I_D design methodology using the inversion coefficient IC to the simple common source (CS) amplifier shown in Figure 1 for various specifications. For the design we assume a generic 180 nm bulk CMOS process. The physical parameters are given in Table 1, the global process parameters in Table 2 and finally the MOSFET parameters in Table 3.

> **!** Important
>
> For this process, the transistor dimensions are rounded to 10nm.

Table 1: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 2: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
H_{dif}	200	nm
W_{min}	200	nm
L_{min}	180	nm

Table 3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$

Table 3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	6.8e-23	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

1 Problem 1: Imposing the gain-bandwidth product (unity gain frequency)

In this first example we will design the CS gain stage shown in Figure 1 for the specifications at room temperature given in Table 1.1 by imposing the inversions coefficient and the load capacitance.

1.1 Analysis

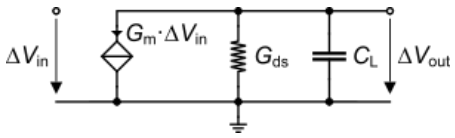

Figure 1.1: Small-signal schematic of the common-source (CS).

The small-signal schematic of the CS amplifier is shown in Figure 1.1. The transfer function is given by

$$H(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A_{dc}}{1+\frac{s}{\omega_c}}, \tag{1.1}$$

where $A_{dc} = -G_m/G_{ds}$ is the dc gain and $\omega_c = G_{ds}/C_L$ the cut-off frequency.

The magnitude of the frequency response is then given by

$$|H(\omega)| = \frac{|A_{dc}|}{\sqrt{1+\left(\frac{\omega}{\omega_c}\right)^2}} \cong \frac{\omega_u}{\omega} \tag{1.2}$$

for $\omega_c \ll \omega$ where

$$\omega_u = |A_{dc}| \cdot \omega_c = \frac{G_m}{C_L} \tag{1.3}$$

is the unity-gain frequency or gain-bandwidth product.

1.2 Specifications

The specifications for Problem 1 are given in Table 1.1.

Table 1.1: Specifications for problem 1.

Specification	Symbol	Value	Unit
Gain-bandwidth product	GBW	10	MHz
Inversion coefficient	IC	1	-
Load capacitance	C_L	1	pF

1.3 Long-channel case

1.3.1 Design

For the long-channel case, we take $L = 1\ \mu m$ which corresponds to an effective length $L_{eff} = 924\ nm$.

The gain-badwidth product GBW and the load capacitance C_L set the required transconductance as $G_m = 62.832\ \mu A/V$. Assuming a long-channel transistor we can neglect the effect of velocity saturation and calculate the current efficiency for the chosen inversion coefficient as $G_m\, nU_T/I_D = 0.618$, from which we get $I_b = 3.344\ \mu A$. From the bias current and the inversion coefficient we get the specific current as $I_{spec} = 3.344\ \mu A$ and the aspect ratio $W/L = 4.677$. Knowing the length, we get the effective width $W_{eff} = 4.319\ \mu m$ and drawn width $W = 4.28\ \mu m$.

We can check what is the resulting dc gain by estimating the output conductance $G_{ds} = I_b/(\lambda_n\, L) = 0.241\ \mu A/V$. The resulting DC gain is then $A_{dc} = G_m/G_{ds}$ = -260.391 or 48.313 dB.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct C_L to get the correct GBW. This results in $C_{DBJ} = 3.6\ fF$, $C_{GD} = 1.6\ fF$, $C_D = 5.2\ fF$. To account for the parasitic capacitance at the drain $C_D = 5.2\ fF$, we need to reduce the load capacitance. The effective load capacitance that needs to be added is then $C_{L0} = 0.995\ pF$ instead of $C_L = 1.000\ pF$.

1.3.2 Simulations

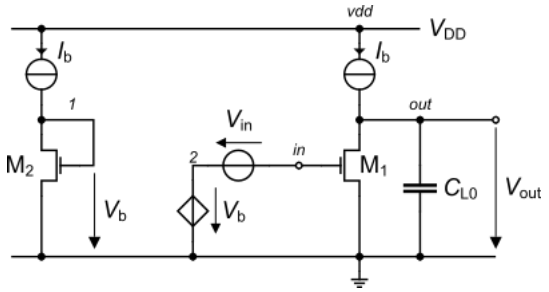

Figure 1.2: Schematic of the common-source (CS) gain stage used for simulation.

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2, where transistor M_2 is used to correctly bias the gate of the CS transistor M_1 so that it draws the desired bias current I_b.

The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=3.344u
.param CL=994.80f W=4.28u L=1.00u AD=1.73e-12 PD=9.44e-06
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.2.

Table 1.2: Operating point information.

Node	Voltage
vdd	1.8
in	0.508564

Table 1.2: Operating point information.

Node	Voltage
out	0.508564
1	0.508564
2	0.508564

The operating information for each transistor can be extracted and are given in Table 1.3 and Table 1.4.

Table 1.3: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[\mu A]$	I_{spec} $[\mu A]$	IC	n	V_{Dsat} $[mV]$
M1	3.344	3.277	1.023	1.27	156
M2	3.344	3.277	1.023	1.27	156

Table 1.4: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[\mu A/V]$
M1	1.27	78.616	61.163	17.292	0.160
M2	1.27	78.616	61.163	17.292	0.160

We see that the simulated transconductance of M_1 $G_m = 61.163\ \mu A/V$ is slightly lower than the theoretical estimation $G_m = 62.832\ \mu A/V$.

We can now proceed with the simulation of the transfer function which is shown in Figure 1.3.

From Figure 1.3, we see that the gain-bandwidth product $GBW = 9.7\ MHz$ is slightly lower than the specifications $GBW = 10\ MHz$ despite we have accounted for the junction capacitance at the output. This comes from the fact that the simulated transconductance $G_m = 61.163\ \mu A/V$ is slightly lower than the theoretical estimation $G_m = 62.832\ \mu A/V$.

We also see that there is some discrepancy of the phase at high frequancy (above the GBW). This coming from the gate-to-drain capacitance (the overla capacitance C_{GDo}) which introduces a positive zero. We can add this zero in the theoretical transfer leading to the transfer function magnitude and phase are plotted in Figure 1.4. We now see that we have a better fit at high frequency (dashed blue line). The gate-to-drain capacitance seems to be larger.

If we want to meet the specifications we can slightly increase the bias current to $I_b = 3.5\ \mu A$. The transfer function is now given in Figure 1.5. We see that we are now right on spec.

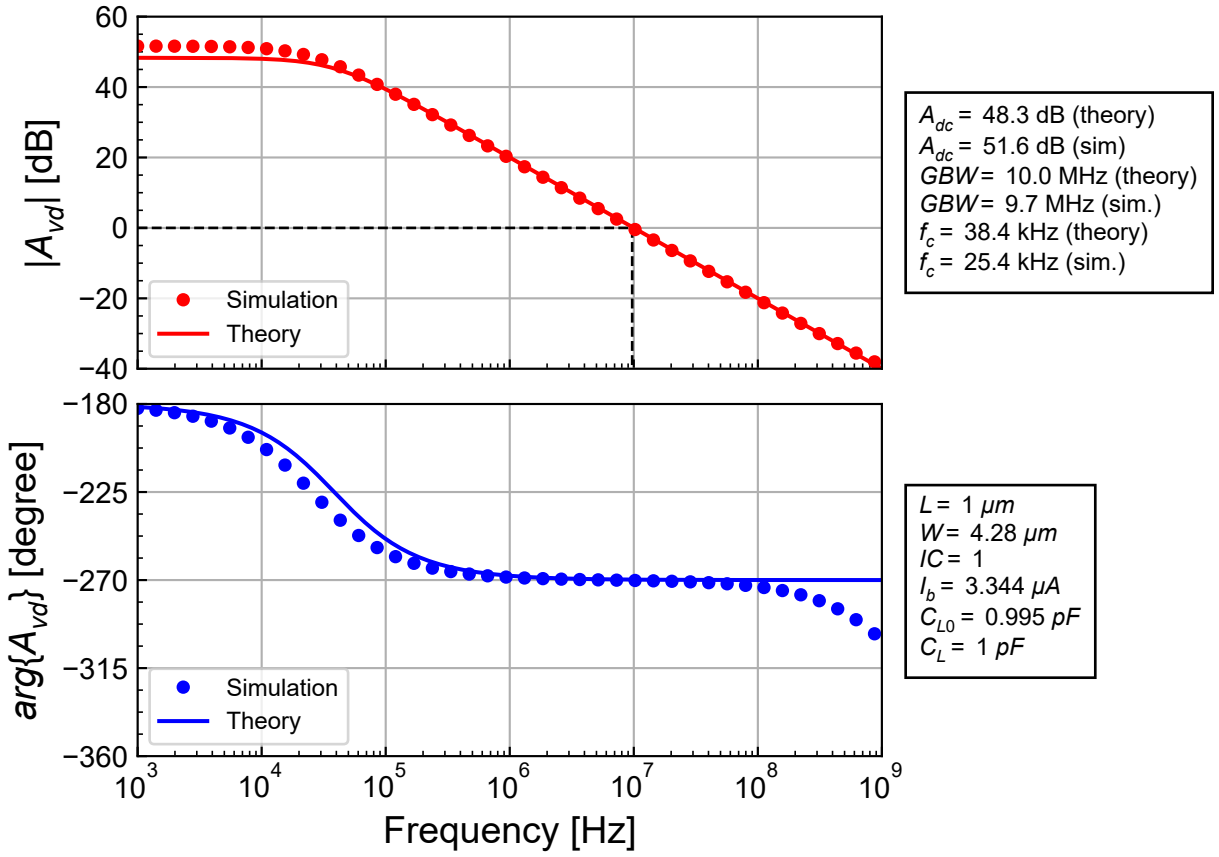

Figure 1.3: Simulated gain response compared to theoretical estimation for the long-channel case.

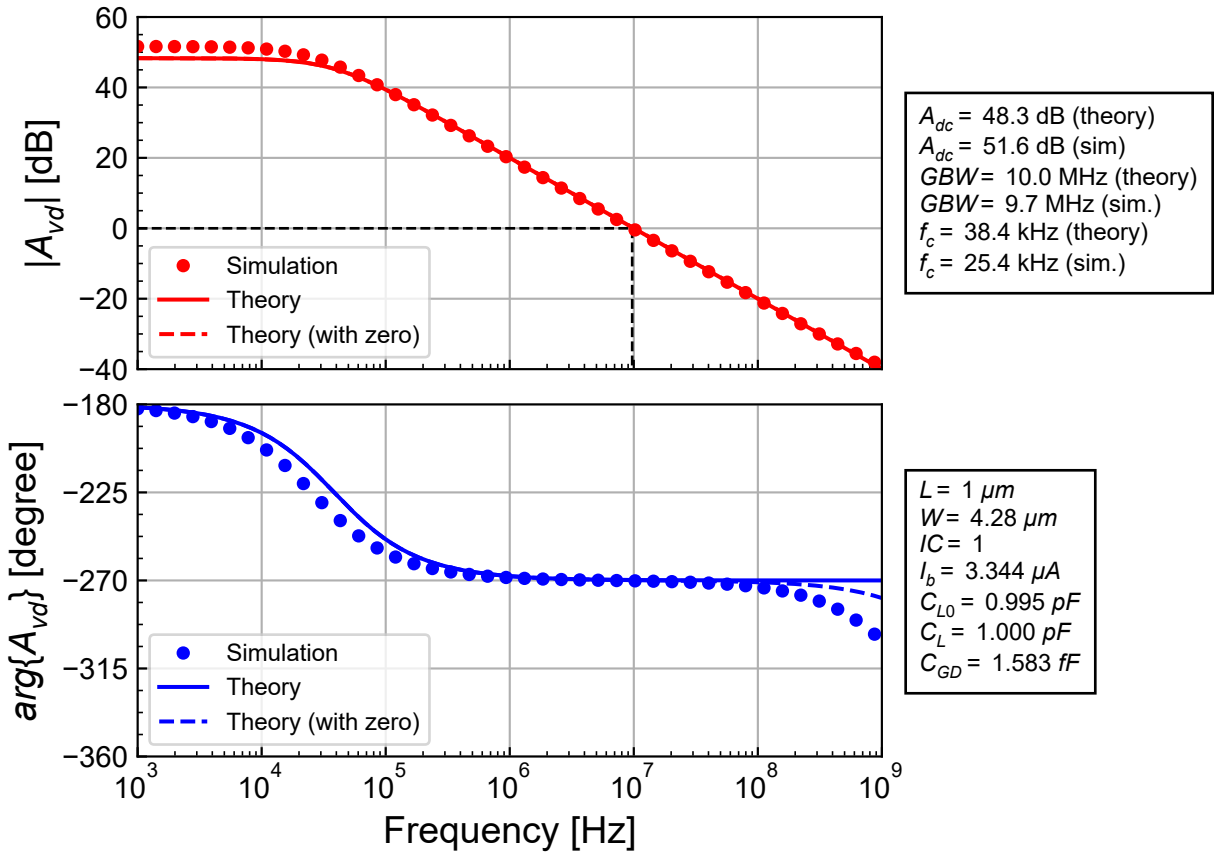

Figure 1.4: Simulated gain response compared to theoretical estimation for the long-channel case.

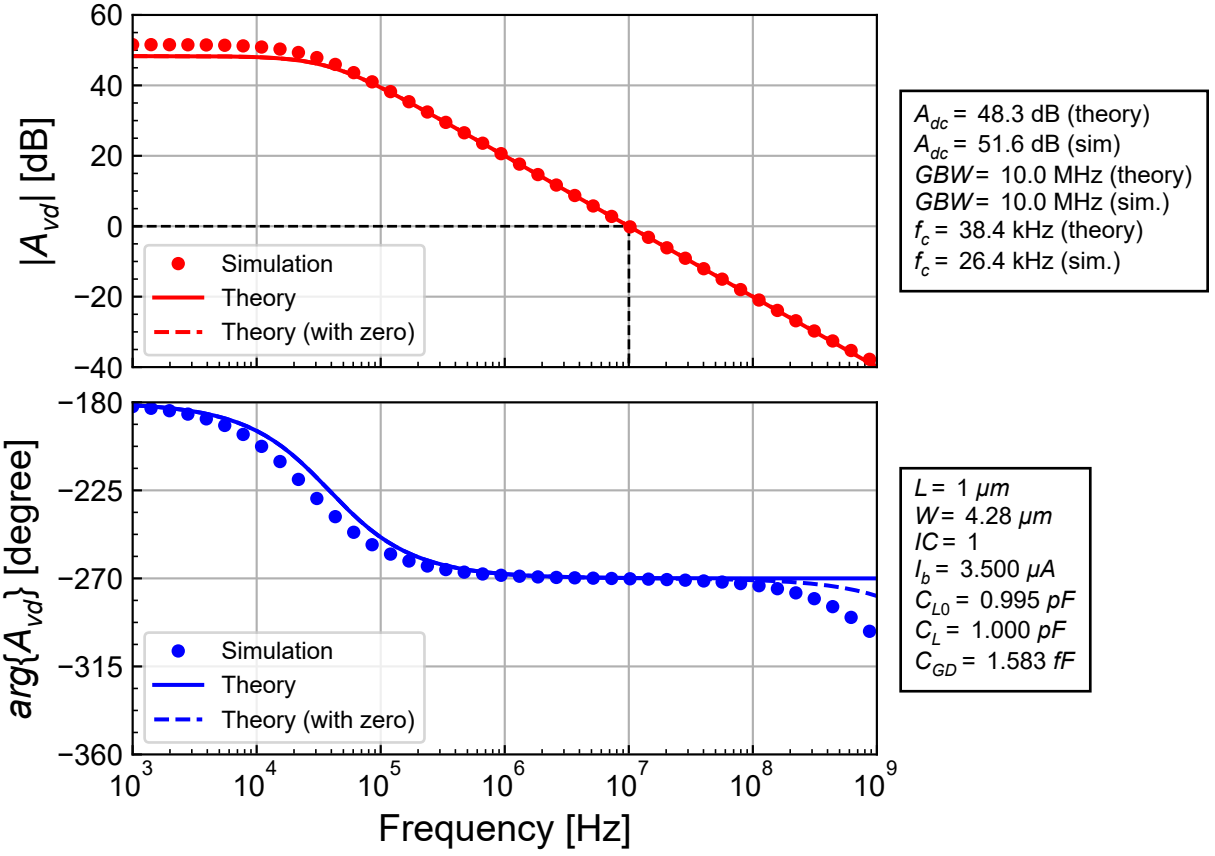

Figure 1.5: Simulated gain response compared to theoretical estimation for the long-channel case.

1.4 Short-channel case (including velocity saturation)

1.4.1 Design

The required transconductance hasn't changed because it is set by the desired gain-bandwidth product and load capacitance $G_m = 62.832\ \mu A/V$.

For the short-channel case we will use the shortest channel length for this technology, namely $L = 0.18\ \mu m$ corresponding to an effective length $L_{eff} = 104\ nm$. The velocity parameter for the chosen length is then given by $\lambda_c = L_{satn}/L_{eff} = 0.250$. The procedure is then the same: we first get the bias current from the current efficiency but including the effect of velocity saturation $G_m\, nU_T/I_D = 0.606$. We see that the current efficiency $G_m\, nU_T/I_D$ is only slightly smaller than for the long-channel case due to velocity saturation. The bias current is then given by $I_b = 3.410\ \mu A$. Despite we use a shorter channel-length, the required bias current is about the same than the one from the long-channel case. This is simply due to the fact the effect of velocity saturation is small in moderate and hence has little effect on the current efficiency.

From the bias current and the inversion coefficient we get the specific current as $I_{spec} = 3.410\ \mu A$ and the aspect ratio $W_{eff}/L_{eff} = 4.770$. For the chosen length we get the effective width $W_{eff} = 0.499\ \mu m$ and drawn width $W = 0.46\ \mu m$.

We can check what is the resulting dc gain by estimating the output conductance $G_{ds} = I_b/(\lambda_n\, L_{eff}) = 2.186\ \mu A/V$. The DC gain is now A_{dc} = -28.740 or 29.170 dB, which, as expected, is significantly lower than for the long-channel case.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct C_L to get the correct GBW. This results in $C_{DBJ} = 1\ fF$, $C_{GD} =$

0.183 fF, $C_D = 1$ fF. The effective load capacitance that needs to be added is then $C_{L0} = 0.999$ pF.

1.4.2 Simulations

We can check whether we get the correct GBW and dc gain using simulations with the following values of the parameters:

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.5.

Table 1.5: Operating point information.

Node	Voltage
vdd	1.8
in	0.511076
out	0.511076
1	0.511076
2	0.511076

The operating information for each transistor can be extracted and are given in Table 1.6 and Table 1.7.

Table 1.6: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[\mu A]$	I_{spec} $[\mu A]$	IC	n	V_{Dsat} $[mV]$
M1	3.500	3.273	1.072	1.27	157
M2	3.500	3.273	1.072	1.27	157

Table 1.7: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[\mu A/V]$
M1	1.27	81.190	63.169	17.855	0.167
M2	1.27	81.190	63.169	17.855	0.167

We see that the simulated transconductance of M_1 $G_m = 63.169$ $\mu A/V$ is slightly larger than the theoretical estimation $G_m = 62.832$ $\mu A/V$.

```
.param VDD=1.8 Ib=3.410u
.param CL=999f W=0.46u L=0.18u AD=2.00e-13 PD=1.80e-06
```

The transfer function magnitude and phase are plotted in Figure 1.6, which shows a reasonable fit between the simulation and the theoretical estimation. The simulated gain-bandwidth product GBW is slightly lower than target and the simulated DC gain is slightly larger than the theoretical estimation.

From Figure 1.6, we see that the simulated DC gain is slightly larger than the theoretical estimation. We also see that the gain-bandwidth product specs is not met. If we want to meet the specifications we can slightly increase the bias current to $I_b = 4.0$ μA. The transfer function is now given in Figure 1.7. We see that we are now right on spec.

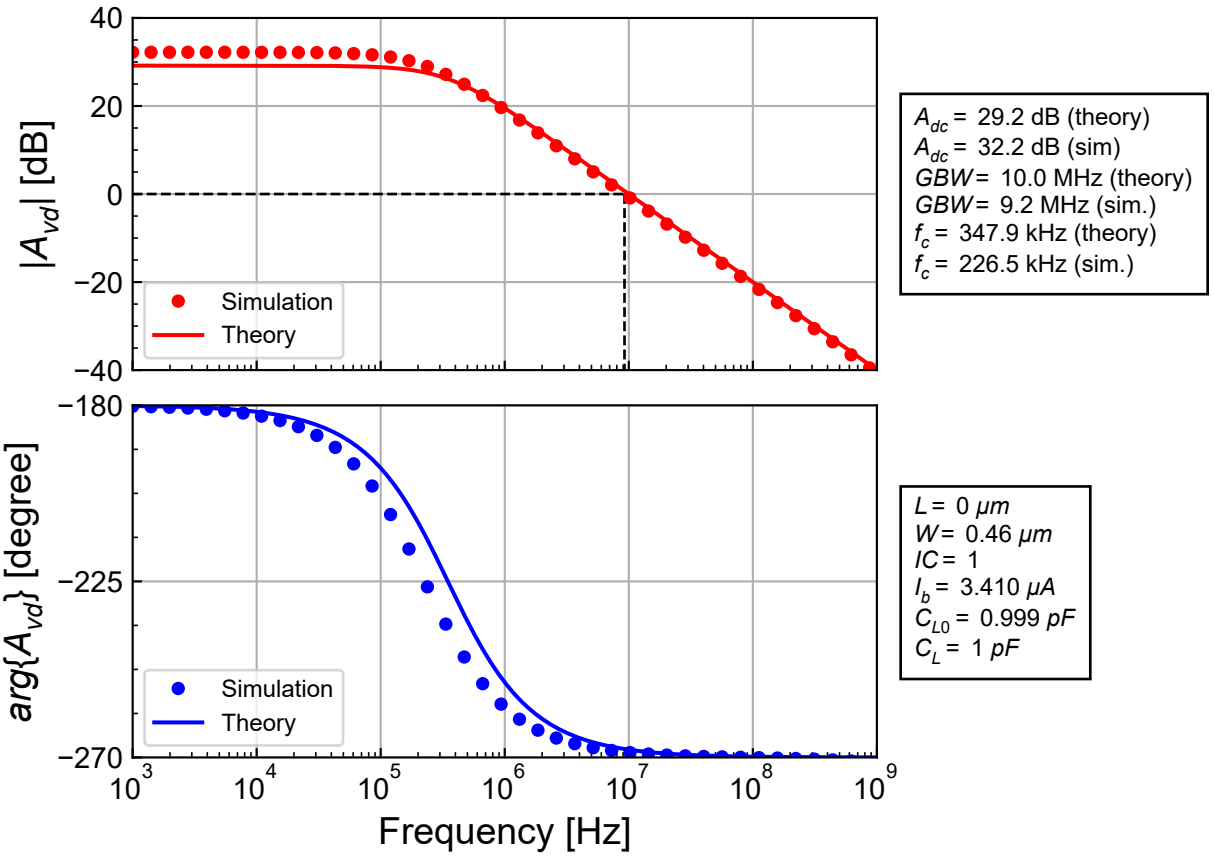

Figure 1.6: Simulated gain response compared to theoretical estimation for the short-channel case.

Note

We also see that for the short-channel case, we don't see the zero which has moved to much higher frequency. This is due to the much smaller transistor width which significantly reduces the gate-to-drain capacitance.

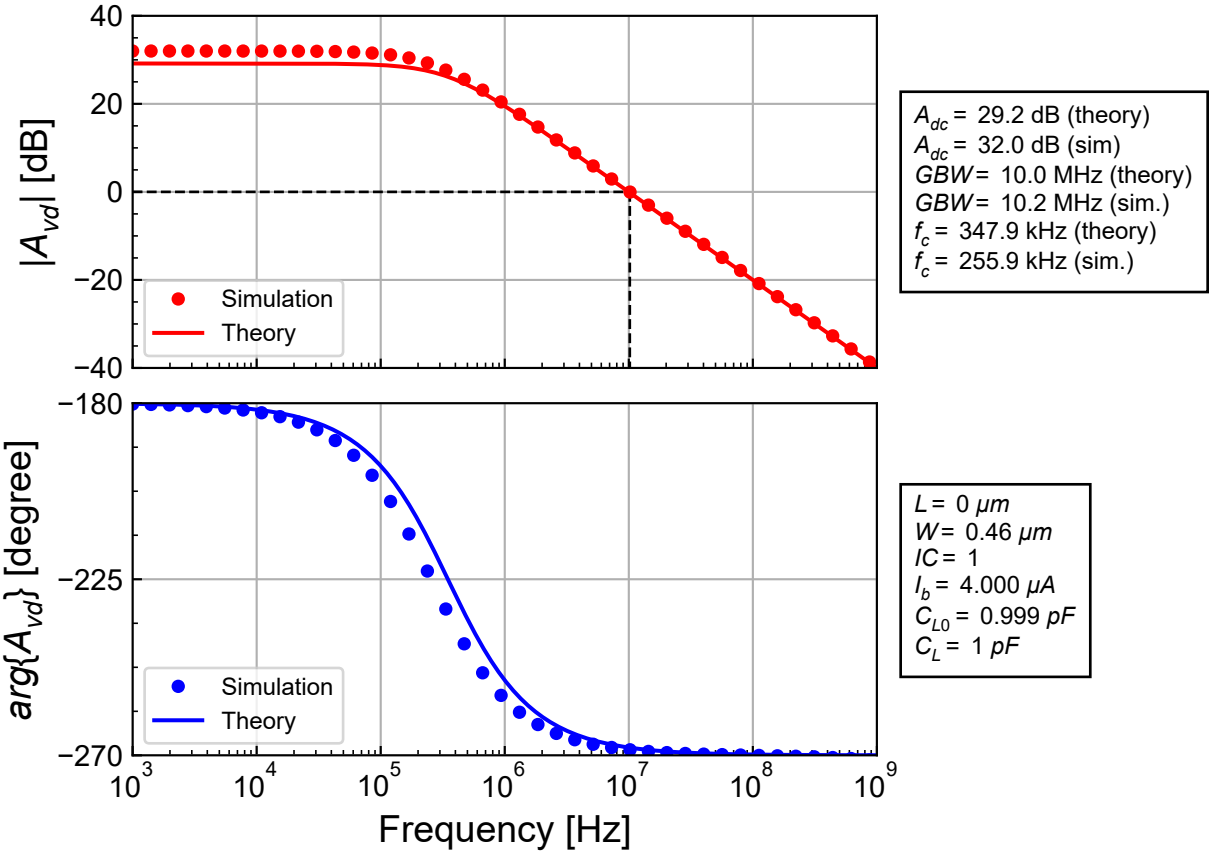

Figure 1.7: Simulated gain response compared to theoretical estimation for the short-channel case.

2 Problem 2: Imposing the power consumption

2.1 Specifications

We now impose the power consumption, the inversion coefficient and the load capacitance according to the specifications given in Table 2.1.

Table 2.1: Specifications for problem 2.

Specification	Symbol	Value	Unit
Power consumption	P	20	μW
Inversion coefficient	IC	1	-
Load capacitance	C_L	1	pF

2.2 Long-channel case

2.2.1 Design

For the long-channel case, we choose $L = 1\ \mu m$ which corresponds to an effective width $L_{eff} = 0.924\ \mu m$. The maximum available current is directly given by $I_b = P/V_{DD} = 11.111\ \mu A$. Since the inversion coefficient is chosen as $IC = 1$, we get the specific current as $I_{spec} = 11.111\ \mu A$. The normalized transconductance is the given by the chosen inversion coefficient as $g_{ms} = G_{ms}/G_{spec} = 0.618$, from which we derive the transconductance $G_m = 208.747\ \mu A/V$ and the gain-bandwidth product for the given load capacitance $GBW = G_m/C_L = 33.223\ MHz$. The aspect ratio is then given by $W_{eff}/L_{eff} = 15.540$. The effective width $W_{eff} = 14.359\ \mu m$ and drawn width $W = 14.32\ \mu m$.

We can calculate the dc gain by first estimating the output conductance $G_{ds} = I_b/(\lambda_n L_{eff}) = 0.802\ \mu A/V$. The dc gain is then given by $A_{dc} = G_m/G_{ds} =$ -260.391 or 48.313 dB.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct C_L to get the correct GBW. This results in $C_{DBJ} = 12\ fF$, $C_{GD} = 5.248\ fF$, $C_D = 17\ fF$. The effective load capacitance that needs to be added is then $C_{L0} = 0.983\ pF$.

2.2.2 Simulations

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=11.111u
.param CL=983.10f W=14.32u L=1.00u AD=5.74e-12 PD=2.95e-05
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 1.2.

Table 2.2: Operating point information.

Node	Voltage
vdd	1.8
in	0.508531
out	0.508531
1	0.508531
2	0.508531

The operating information for each transistor can be extracted and are given in Table 1.3 and Table 1.4.

Table 2.3: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[\mu A]$	I_{spec} $[\mu A]$	IC	n	V_{Dsat} $[mV]$
M1	11.111	10.895	1.022	1.27	156
M2	11.111	10.895	1.022	1.27	156

Table 2.4: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[\mu A/V]$
M1	1.27	261.256	203.257	57.466	0.533
M2	1.27	261.256	203.257	57.466	0.533

We see that the simulated transconductance of M_1 $G_m = 203.257\ \mu A/V$ is slightly lower than the theoretical estimation $G_m = 208.747\ \mu A/V$.

The transfer function magnitude and phase are plotted in Figure 1.4, which shows a good fit between the simulation and the theoretical estimation.

2.3 Short-channel case (including velocity saturation)

2.3.1 Design

For the short-channel case we will use the shortest channel length for this technology, namely $L = 180\ nm$. The velocity parameter for the chosen length is then given by $\lambda_c = L_{satn}/L = 0.250$. The procedure is basically the same except that we now need to account for velocity saturation in the estimation of the transconductance. Since the inversion coefficient is chosen as $IC = 1$, we get the specific current as $I_{spec} = 11.111\ \mu A$. The normalized transconductance is the given by the chosen inversion coefficient as $g_{ms} = G_{ms}/G_{spec} = 0.606$, from which we derive the transconductance $G_m = 0.205\ mA/V$ and the gain-bandwidth product for the given load capacitance $GBW = G_m/C_L = 32.580\ MHz$. The aspect ratio is then given by $W_{eff}/L_{eff} = 15.540$. The effective width $W_{eff} = 1.619\ \mu m$ and drawn width $W = 1.58\ \mu m$.

We can calculate the dc gain by first estimating the output conductance $G_{ds} = I_b/(\lambda_n\, L_{eff}) = 7.123$ $\mu A/V$. The dc gain is then given by $A_{dc} = G_m/G_{ds}$ = -28.740 or 29.170 dB.

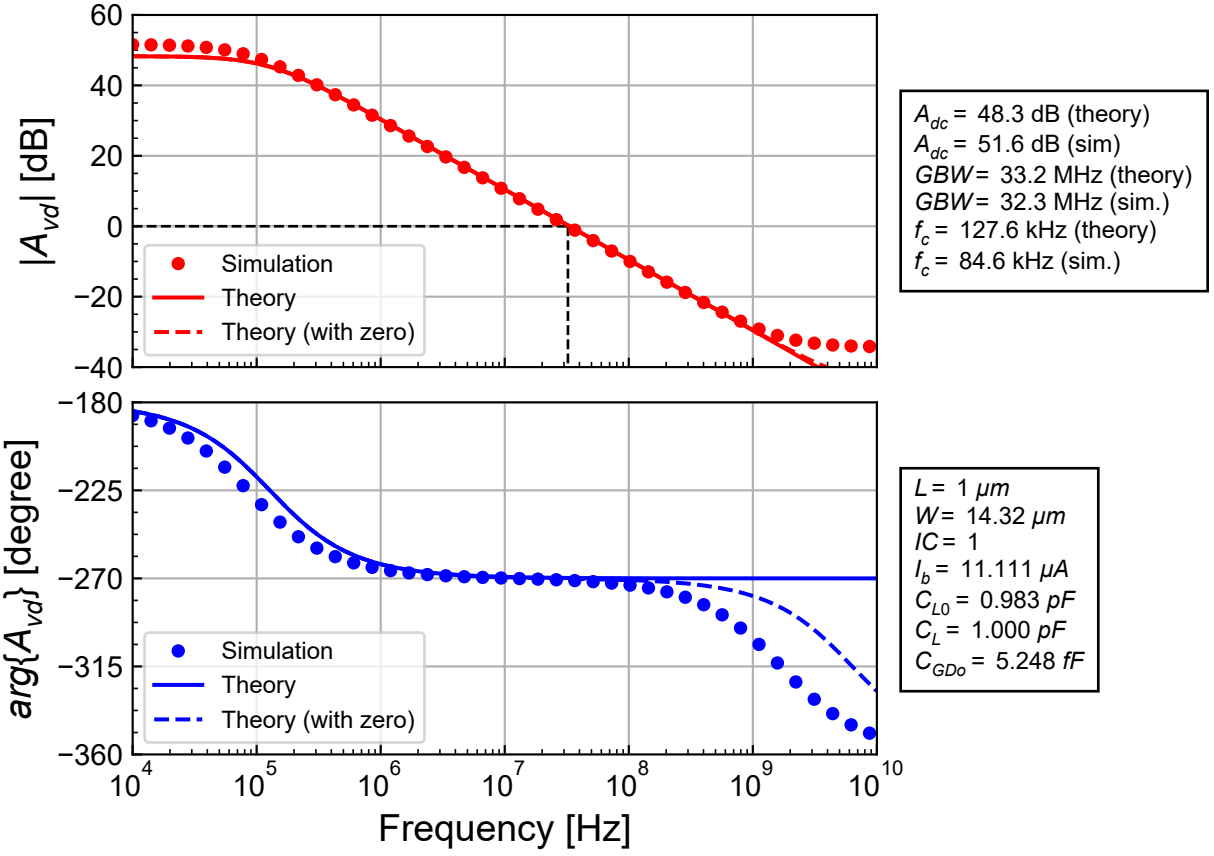

Figure 2.1: Simulated gain response compared to theoretical estimation for the long-channel case.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct C_L to get the correct GBW. This results in $C_{DBJ} = 1.5\ fF$, $C_{GD} = 0.579\ fF$, $C_D = 2.0\ fF$. The effective load capacitance that needs to be added is then $C_{L0} = 0.998\ pF$.

2.3.2 Simulations

We can check whether we get the correct GBW and dc gain using simulations with the following values of the parameters:

```
.param VDD=1.8 Ib=11.111u
.param CL=997.97f W=1.58u L=0.18u AD=6.48e-13 PD=4.04e-06
```

The transfer function magnitude and phase are plotted in Figure 2.2, which shows a reasonable fit between the simulation and the theoretical estimation.

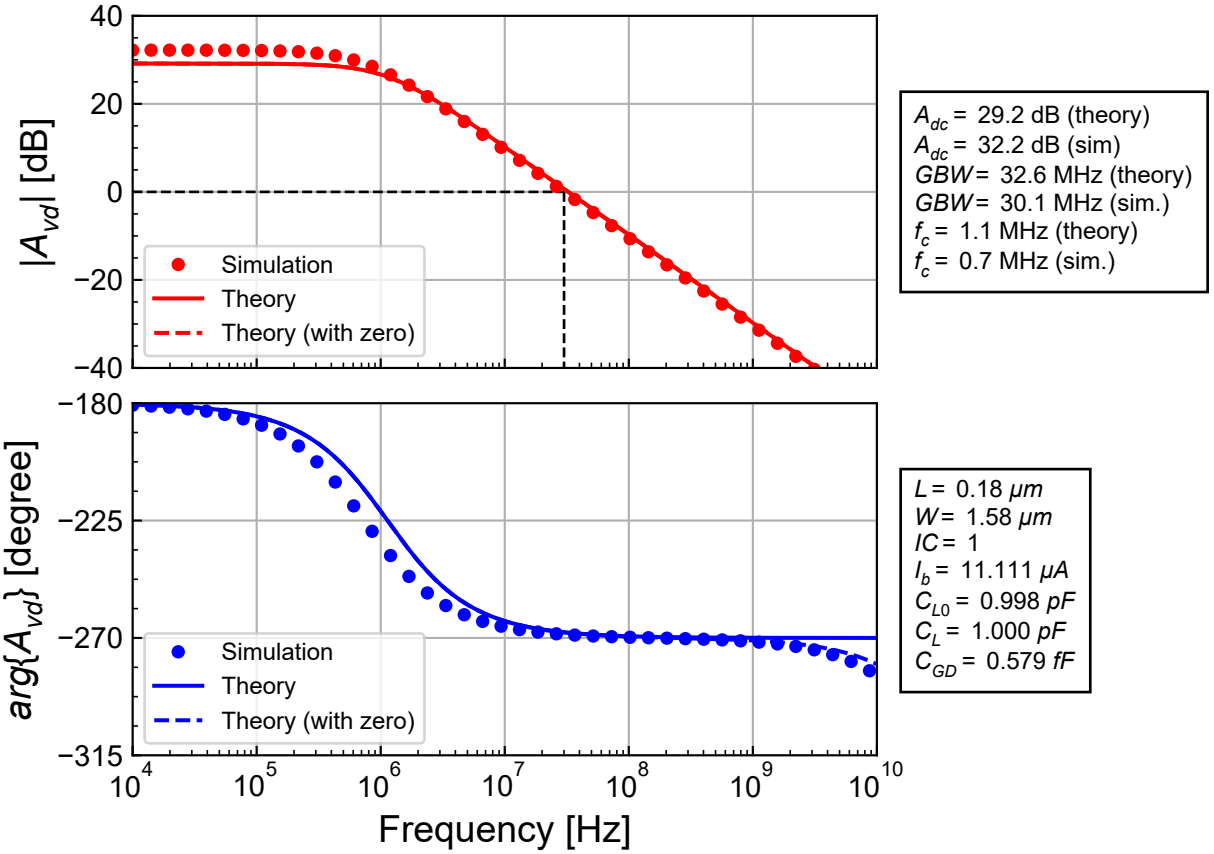

Figure 2.2: Simulated gain response compared to theoretical estimation for the short-channel case.

3 Problem 3: Imposing the gain bandwidth product and the current budget

3.1 Specifications

We now don't impose the inversion coefficient but the gain bandwidth product and the current budget. We keep the same load capacitance and consider a long channel. The specifications are now given in Table 3.1.

Table 3.1: Specifications for problem 3.

Specification	Symbol	Value	Unit
Gain-bandwidth product	GBW	1	MHz
Bias current	I_b	400	nA
Load capacitance	C_L	1	pF
Transistor length	L	1	μm

3.2 Design

We first get the transconductance required to achieve the target gain-bandwidth product as $G_m = 6.283$ $\mu A/V$. Knowing the bias current and the transconductance we can calculate the current efficiency as $G_m\, nU_T/I_D = 0.517$, from which we can derive the corresponding inversion coefficient $IC = 1.810$. We see that we are in the moderate inversion region. The specific current is then given by $I_{spec} = 221$ nA, the aspect ratio by $W_{eff}/L_{eff} = 0.309$, the effective width by $W_{eff} = 289$ nm and finally the drawn width $W = 250$ nm.

We can calculate the dc gain by first estimating the output conductance $G_{ds} = I_b/(\lambda_n\, L_{eff}) = 28.860$ nA/V. The dc gain is then given by $A_{dc} = G_m/G_{ds}$ = -217.712 or 46.758 dB.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct C_L to get the correct GBW. This results in $C_{DBJ} = 391.2$ aF, $C_{GD} = 105.918$ aF, $C_D = 497.1$ aF. The effective load capacitance that needs to be added is then $C_{L0} = 999.503$ fF. We observe that the parasitic capacitance at the drain are negligible compared to the load capacitance.

3.3 Simulations

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=0.400u
.param CL=999.50f W=0.25u L=1.00u AD=1.16e-13 PD=1.38e-06
```

The transfer function magnitude and phase are plotted in Figure 1.4, which shows a good fit between the simulation and the theoretical estimation.

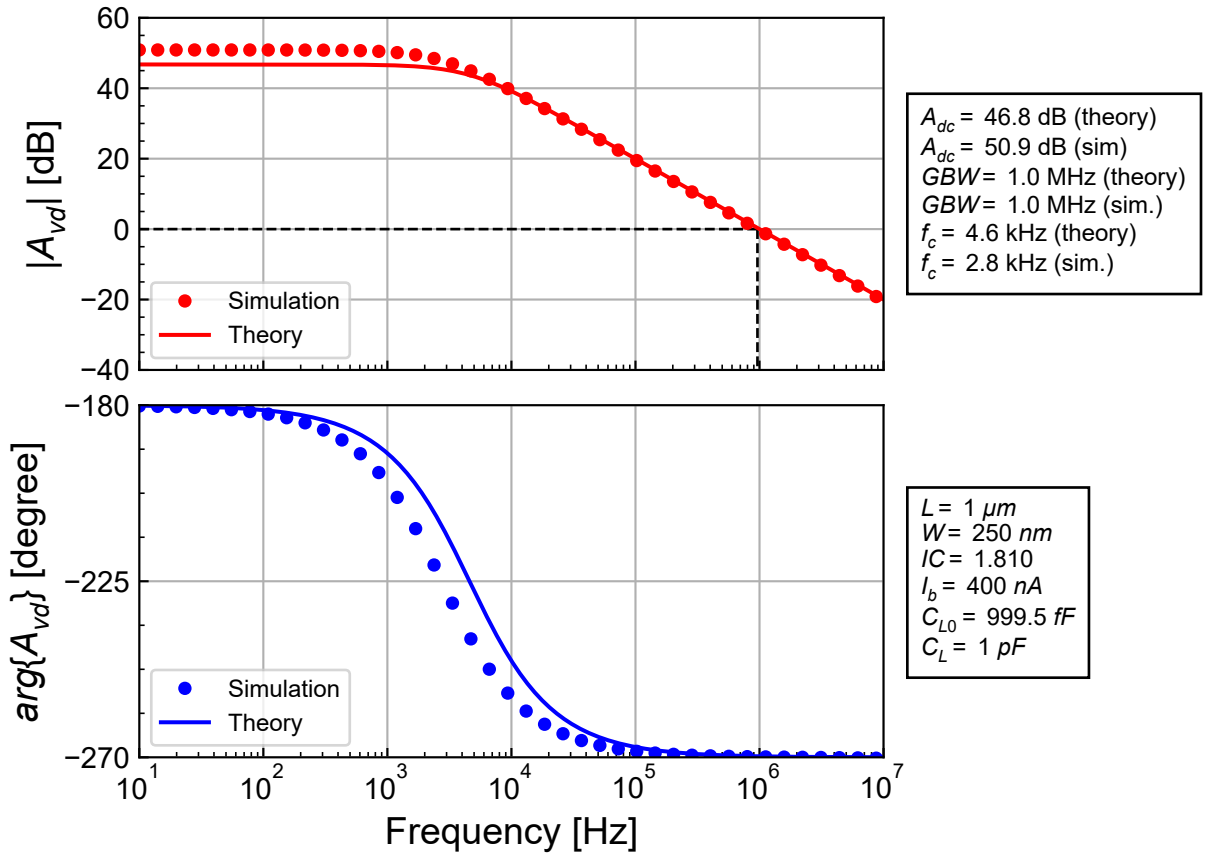

Figure 3.1: Simulated gain response compared to theoretical estimation for the long-channel case.

4 Problem 4: Imposing the input-referred noise

4.1 Specifications

In this example, we impose the input-referred noise by setting the white noise and the corner frequency. The specifications are given in Table 4.1.

Table 4.1: Specifications for problem 4.

Specification	Symbol	Value	Unit
Corner frequency	f_k	100	kHz
Input referred white PSD	$\sqrt{S_{n,th}}$	30	$\frac{nV}{\sqrt{Hz}}$
	$10\log(S_{n,th})$	-150.46	$\frac{dBv}{\sqrt{Hz}}$
Inversion coefficient	IC	1	-
Load capacitance	C_L	1	pF

4.2 Design

We need the flicker noise parameter K_f = 8.100e-24 J and the oxide capacitance per unit area C_{ox} = 8.443 $fF/\mu m^2$.

Before the transconductance is derived from the thermal noise specification, we need to know the thermal noise excess factor γ_n for the given IC (we assume long-channel case) which is $\gamma_n = 0.717$. The transconductance is then given by $G_m = 4kT\gamma_n/S_{nin,th} = 13.186\ \mu A/V$, where $S_{nin,th} = V^2_{nin,th}$. Once we have the transconductance, the procedure is similar to the previous one.

Having imposed the inversion coefficient $IC = 1$, we can deduce the current efficiency as $G_m\, nU_T/I_D = 0.618$. By definition of the current efficiency we can get the corresponding bias current $I_b = 702\ nA$. The specific current and aspect ratio are then given by $I_{spec} = 702\ nA$ and $W_{eff}/L_{eff} = 0.982$.

The corner frequency will actually set the flicker noise which is inversely proportional to the gate are. We can therefore calculate the gate area from the flicker noise remembering that the corner frequency is the frequency at which the flicker noise becomes equal to the white noise. The gate area is obtained as $W_{eff}\, L_{eff} = 10.660\ \mu m^2$. Knowing the W/L ratio we can calculate the effective width and length as $W_{eff} = 3.235\ \mu m$ and $L_{eff} = 3.295\ \mu m$. The drawn width and length follow as $W = 3.20\ \mu m$ and $L = 3.37\ \mu m$.

The gain-bandwidth product is given by $GBW = 2.099\ MHz$.

We can calculate the dc gain by first estimating the output conductance $G_{ds} = I_b/(\lambda_n\, L_{eff}) = 0.014$ $\mu A/V$. The dc gain is then given by $A_{dc} = G_m/G_{ds}$ = -928.687 or 59.357 dB.

We also calculate the area and perimeter of the drain to estimate the junction capacitance and overlap capacitance in order to correct C_L to get the correct GBW. This results in $C_{DBJ} = 2.7\ fF$, $C_{GD} = 1.186\ fF$, $C_D = 3.9\ fF$. The effective load capacitance that needs to be added is then $C_{L0} = 0.996$ pF.

4.3 Simulations

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=702n
.param CL=996.07f W=3.20u L=3.37u AD=1.29e-12 PD=7.27e-06
```

The transfer function magnitude and phase are plotted in Figure 4.2, which shows a good fit between the simulation and the theoretical estimation.

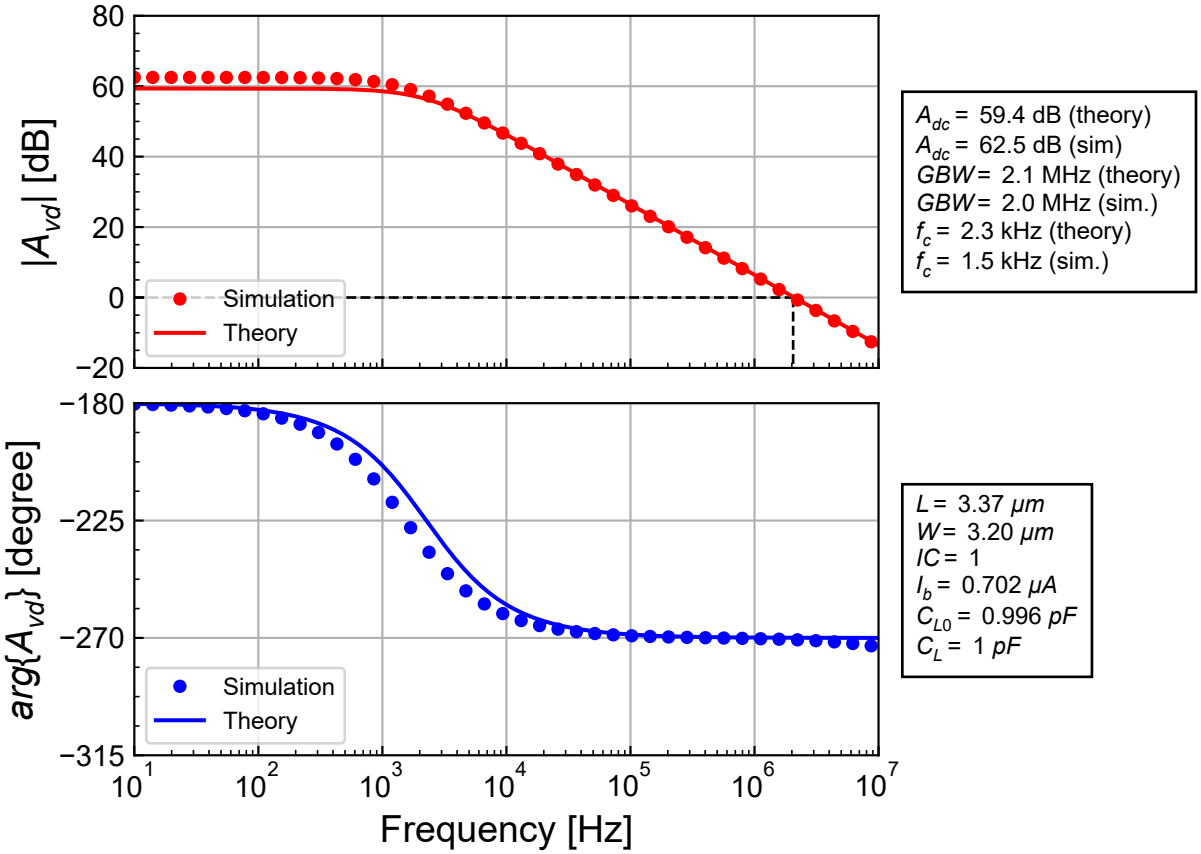

Figure 4.1: Simulated gain response compared to theoretical estimation for the long-channel case.

We can now check the input-referred noise PSD which is plotted in Figure 4.2. We can see that simulation perfectly matches the theoretical estimation.

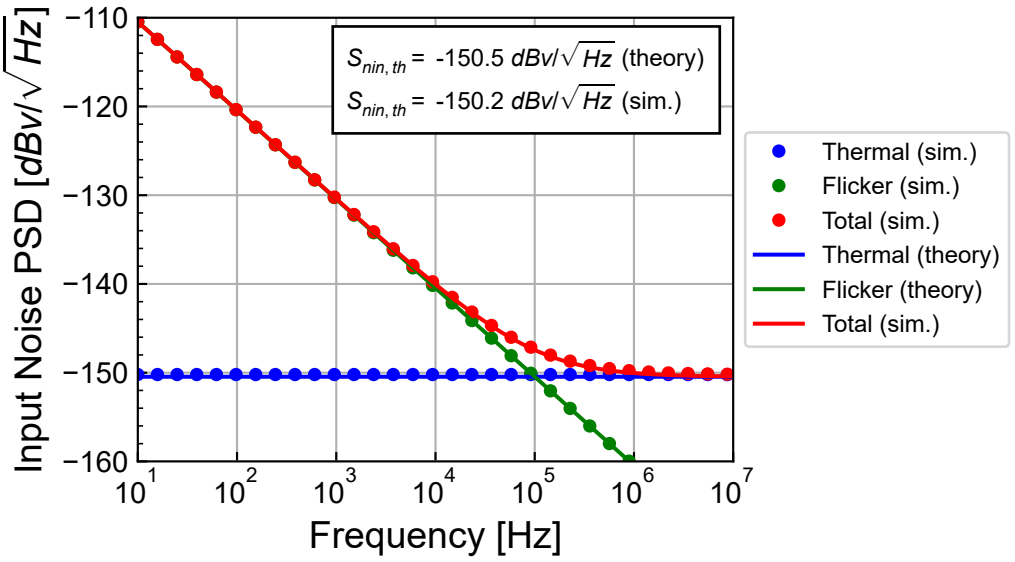

Figure 4.2: Simulated input-referred noise PSD compared to theoretical estimation.

5 Problem 5: Minimum current for a given gain-bandwidth product with self-loading

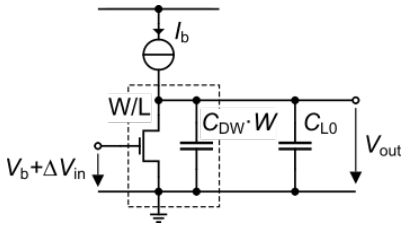

Figure 5.1: Schematic of the common-source (CS) illustrating the self-loading effect.

In this problem we want to find the minimum current required to achieve a given gain-bandwidth product accounting for the effect of self-loading as illustrated in Figure 5.1.

The total transistor parasitic capacitance at the drain can be written as

$$C_D = C_{D0} + C_{DW} \cdot W. \tag{5.1}$$

with

$$C_{D0} = 4H_{dif} \cdot C_{JSW}, \tag{5.2}$$
$$C_{DW} = 2(H_{dif} \cdot C_J + C_{JSW}) + C_{GDe}, \tag{5.3}$$

where C_{GDe} is the extrinsic capacitance per unit width which is made of the overlap capacitance C_{GDo}. In more advanced technologies we also need to add the fringing-field capacitance C_{GDf}. In this 180nm technology the fringing-field capacitance can be neglected so that $C_{GDe} \cong C_{GDo}$.

The part C_{D0} of the total parasitic capacitance at the drain C_D that doesn't scale with W needs to be added to C_{L0} so that the total load capacitance that does not scale with W is given by

$$C_L = C_{L0} + C_{D0}. \tag{5.4}$$

It can be shown [1] that when accounting for the self-loading effect, there is a minimum current for achieving a given gain-bandwidth product. The otptimum value of the inversion coefficient IC_{opt} corresponding to this minimum bias current is given by

$$IC_{opt} = \left(\sqrt{\Theta \cdot (1+\Theta)} + \Theta + \frac{1}{2}\right)^2 - \frac{1}{4} = 2\Theta \cdot (1+\Theta) + (1+2\Theta) \cdot \sqrt{\Theta \cdot (1+\Theta)}, \tag{5.5}$$

where

$$\Theta \triangleq \frac{\omega_u}{\omega_W}, \tag{5.6}$$

with

$$\omega_u \triangleq 2\pi\, GBW, \tag{5.7}$$
$$\omega_W \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{DW} \cdot L}. \tag{5.8}$$

The parameter Θ is usually $\Theta \ll 1$ and therefore (5.5) reduces to

$$IC_{opt} \cong 2\Theta + \sqrt{\Theta}. \tag{5.9}$$

We can define a normalized current and aspect ratio as

$$i_b \triangleq \frac{I_b}{I_{spec\square} \cdot \Omega}, \tag{5.10}$$

$$AR \triangleq \frac{W/L}{\Omega}, \tag{5.11}$$

where

$$\Omega \triangleq \frac{\omega_u}{\omega_L}, \tag{5.12}$$

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_L}. \tag{5.13}$$

The minimum normalized current i_{bopt} and aspect ratio AR_{opt} only depend on Θ according to

$$i_{bopt} \triangleq i_b(IC_{opt}) = \sqrt{4IC_{opt}+1} = 1 + 2\Theta + 2\sqrt{\Theta \cdot (1+\Theta)}, \tag{5.14}$$

$$AR_{opt} \triangleq AR(IC_{opt}) = \frac{\sqrt{4IC_{opt}+1}}{IC_{opt}} = \frac{1}{\sqrt{\Theta \cdot (1+\Theta)}}. \tag{5.15}$$

5.1 Specifications

The specifications for Problem 5 are given in Table 5.1.

Table 5.1: Specifications for problem 5.

Specification	Symbol	Value	Unit
Gain-bandwidth product	GBW	25	MHz
Load capacitance	C_{L0}	20	fF
Transistor length	L	1	μm

5.2 Design

For accounting for the self-loading effect we need the capacitance per width $C_{DW} = 1.167\ fF/\mu m$. All the parameters are given in Table 5.2.

Table 5.2: Parameters for problem 5.

Parameter	Value	Unit
C_{DW}	1.167	$fF/\mu m$
C_{D0}	0.16	fF
C_{L0}	20	fF
C_L	20.16	fF
f_L	171.589	MHz
f_W	2.965	GHz
Ω	0.146	-
Θ	0.00843	-

Table 5.2: Parameters for problem 5.

Parameter	Value	Unit
IC_{opt}	0.111	-
$i_{b,opt}$	1.201	-
AR_{opt}	10.846	-
$(W/L)_{opt}$	1.58	-
$I_{b,opt}$	125	nA
W_{opt}	1.46	μm
$G_{m,opt}$	3.456	$\mu A/V$
$C_{D,opt}$	1.703	fF
AD	0.58	μm^2
PD	3.72	μm
C_{DBJ}	1.328	fF
C_F	0.535	fF
C_{out}	21.863	fF
GBW (check)	25	MHz
f_z	1.028	GHz
A_{dc}	52.346	dB

5.3 Simulations

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=125n
.param CL=20.00f W=1.42u L=1.00u AD=5.84e-13 PD=3.72e-06
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 5.3.

Table 5.3: Operating point information.

Node	Voltage
vdd	1.8
in	0.412978
out	0.412978
1	0.412978
2	0.412978

The operating information for each transistor can be extracted and are given in Table 5.4 and Table 5.5.

Table 5.4: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[\mu A]$	I_{spec} $[\mu A]$	IC	n	V_{Dsat} $[mV]$
M1	0.125	1.147	0.109	1.27	121
M2	0.125	1.147	0.109	1.27	121

Table 5.5: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[\mu A/V]$
M1	1.27	4.385	3.395	0.981	0.008
M2	1.27	4.385	3.395	0.981	0.008

We see that the simulated transconductance of M_1 $G_m = 3.395\ \mu A/V$ is close to the theoretical estimation $G_m = 3.456\ \mu A/V$.

The transfer function maginitude and phase are plotted in Figure 5.2, which shows a good fit between the simulation and the theoretical estimation. The gain-bandwidth product GBW is right on target. However, the simulated DC gain is slightly larger than the theoretical estimation. We also see some discrepancy at higher frequency. This is due to the zero introduced by the gate-to-drain capacitance C_{GD}.

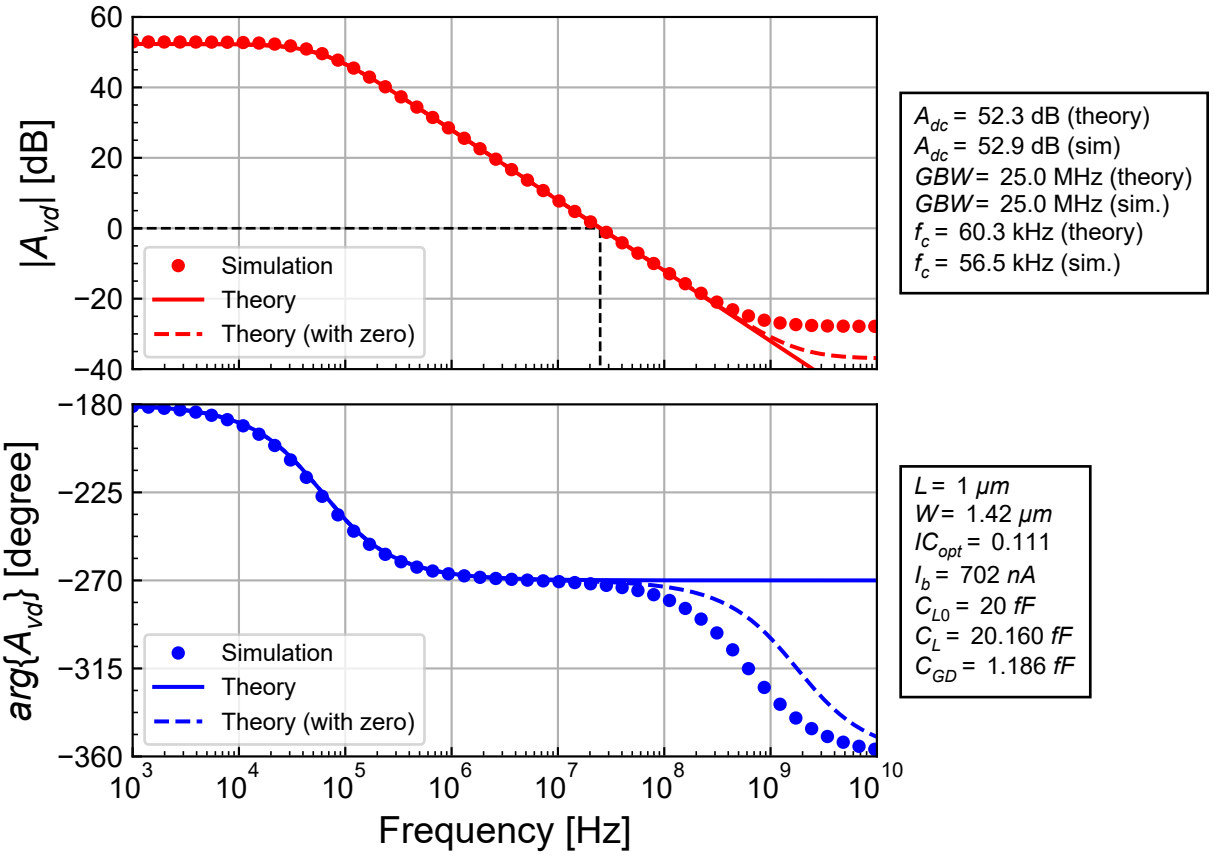

Figure 5.2: Simulated gain response compared to theoretical estimation for the long-channel case.

From Figure 5.2 we see that accounting for the gate-to-drain capacitance which corresponds actually to the overlap capacitance C_{GDo}, still underestimates the loction of the zero. This is due to a larger feedback capacitance. This is actually coming from the fact that we have ignored the transcapacitance C_m in the small-signal analysis. In the quasi-static (QS) circuit of the MOS transistor, the transconductance needs to be replaced by the a transadmittance Y_m given by

$$Y_m = G_m + s\,C_m \tag{5.16}$$

where C_m is the gate transcapacitance given by

$$C_m = C_{OX} \cdot c_m \tag{5.17}$$

where $C_{OX} \triangleq W\,L\,C_{ox}$ and c_m is the normalized gate transcapacitance given by [2]

$$c_m = \frac{q_s - q_d}{15}\,\frac{4q_s^2 + 4q_d^2 + 12q_sq_d + 10q_s + 10q_d + 5}{(q_s + q_d + q)^3}, \tag{5.18}$$

which in saturation ($q_d = 0$) reduces to

$$c_{m_{sat}} \cong \frac{4q_s^2 + 10q_s + 5}{(q_s + 1)^3}. \tag{5.19}$$

For a long-channel transistor, q_s is simply given by

$$q_s = \frac{\sqrt{4IC + 1} - 1}{2}. \tag{5.20}$$

The corresponding transfer function including the effect of the gate transcapacitance C_m is then given by

$$A(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{dc} \cdot \frac{1 - s/\omega_z}{1 + s/\omega_p} \tag{5.21}$$

where

$$A_{dc} = -G_m \cdot R_{ds}, \tag{5.22}$$

$$\omega_z = \frac{G_m}{C_F + C_m}, \tag{5.23}$$

$$\omega_p = \frac{1}{R_{ds}\,C_{out}}, \tag{5.24}$$

with $C_{out} = C_L + C_F$ the total load capacitance. We see that the transcapacitance C_m directly adds to the feedback capacitance C_F, but does not add to the load capacitance C_{out}. Therefore, the expression of the pole remains unchanged. The DC gain and the gain-bandwidth hence also remain unaffected by the transcapacitance.

The theoretical transfer function including the effect of the gate transcapacitance is shown in Figure 5.3. We now see that the theoretical estimation perfectly matches the simulation including at high frequency.

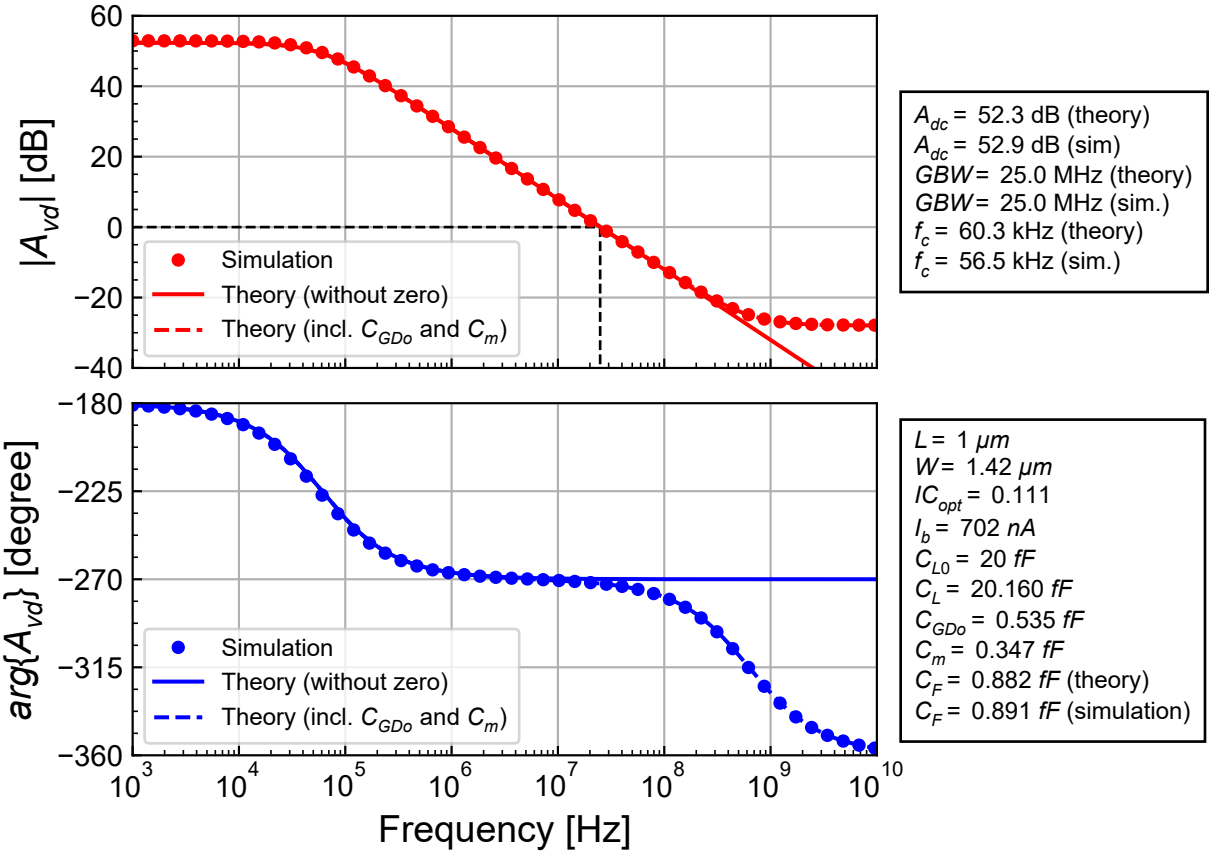

Figure 5.3: Simulated gain response compared to theoretical estimation for the long-channel case.

6 Problem 6: Minimum current for a given DC gain and gain-bandwidth product with self-loading

In this problem we want to find the minimum current required to achieve a given gain-bandwidth product and a given dc gain accounting for the effect of self-loading. We can actually use the additional degree of freedom, namely the transistor length L (which has been arbitrarily set in the previous example), to set the DC gain. To this purpose we can use the simple output conductance model given by

$$G_{ds} \cong \frac{I_D}{\lambda \cdot L}. \tag{6.1}$$

It can be shown that there is also an optimum value of the inversion coefficient for which the bias current becomes minimum [1]

$$IC_{opt} = \frac{\sqrt{\xi}}{(1-\sqrt{\xi})^2}, \tag{6.2}$$

where parameter ξ brings together the technology parameters and the specs according to

$$\xi \triangleq \underbrace{A_{dc} \cdot \omega_u}_{\text{specifications}} \cdot \underbrace{\frac{C_{DW} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda}}_{\text{technology parameters}}. \tag{6.3}$$

It can be shown that parameter ξ needs to satisfy the following inequality

$$\xi \triangleq A_{dc} \cdot \omega_u \cdot \frac{C_{DW} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} < 1.$$

This means that we can check whether the specifications on A_{dc} and ω_u can be achieved for a given technology (i.e. for a set of $I_{spec\square}$, λ and C_{DW}). The closer ξ gets to 1, the larger the required current and size.

We can define the normalized bias current i_b, transistor width w and length ℓ according to

$$i_b \triangleq \frac{I_b}{I_{norm}} = \frac{g_{ms} \cdot IC}{g_{ms}^2 - \xi \cdot IC} = \frac{g_{ms}/IC}{(g_{ms}/IC)^2 - \xi/IC}, \tag{6.4}$$

$$w \triangleq \frac{W}{W_{norm}} = \frac{IC}{g_{ms}^2 - \xi \cdot IC}, \tag{6.5}$$

$$\ell \triangleq \frac{L}{L_{norm}} = \frac{IC}{g_{ms}}, \tag{6.6}$$

where

$$I_{norm} \triangleq n\,U_T \cdot C_{L0} \cdot \omega_u, \tag{6.7}$$

$$W_{norm} \triangleq \frac{C_{L0} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} \cdot A_{dc} \cdot \omega_u, \tag{6.8}$$

$$L_{norm} \triangleq \frac{nU_T}{\lambda} \cdot A_{dc}. \tag{6.9}$$

The minimum normalized current is then given by

$$i_{b,opt} \triangleq i_b(IC_{opt}) = \frac{1}{\left(1-\sqrt{\xi}\right)^2} = \frac{1+2IC_{opt}+\sqrt{4IC_{opt}+1}}{2}. \tag{6.10}$$

The optimum normalized width, length and transconductance are given by

$$w_{opt} \triangleq w(IC_{opt}) = \frac{1}{\sqrt{\xi}\ \left(1-\sqrt{\xi}\right)} = \frac{1+3IC_{opt}+(1+IC_{opt})\sqrt{4IC_{opt}+1}}{2IC_{opt}}, \tag{6.11}$$

$$\ell_{opt} \triangleq \ell(IC_{opt}) = \frac{1}{1-\sqrt{\xi}} = \frac{1+\sqrt{4IC_{opt}+1}}{2}, \tag{6.12}$$

$$g_{m,opt} \triangleq g_m(IC_{opt}) = \frac{1}{1-\sqrt{\xi}} = \frac{1+\sqrt{4IC_{opt}+1}}{2}. \tag{6.13}$$

Note that the optimum current, width, length and transconductance only depend on ξ.

6.1 Specifications

The specifications for Problem 5 are given in Table 6.1.

Table 6.1: Specifications for problem 6.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	50	dB
Gain-bandwidth product	GBW	25	MHz
Load capacitance	C_{L0}	20	fF

6.2 Design

We can start by checking that the specifications in Table 6.1 are feasible for the given 180nm technology. For this we can check that

$$\xi \triangleq A_{dc} \cdot \omega_u \cdot \frac{C_{DW} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} < 1.$$

For the specifications in Table 6.1 and the chosen 180nm technology we have $\xi = 0.006$ which is smaller than 1.

Table 6.2: Parameters or problem 6.

Parameter	Value	Unit
C_{DW}	1.167	$fF/\mu m$
C_{D0}	0.16	fF
C_{L0}	20	fF
C_L	20.16	fF
ξ	0.006	-
IC_{opt}	0.09	-
$i_{b,opt}$	1.172	-
w_{opt}	14.161	-
ℓ_{opt}	1.083	-
$g_{m,opt}$	1.083	-

Table 6.2: Parameters or problem 6.

Parameter	Value	Unit
$I_{b,opt}$	122	nA
$(W/L)_{opt}$	1.58	-
I_{norm}	104	nA
W_{norm}	101	nm
L_{norm}	694	nm
$G_{m,norm}$	3.167	$\mu A/V$
$I_{b,opt}$	122.138	nA
W_{opt}	1.43	μm
L_{opt}	750.94	nm
$G_{m,opt}$	3.429	$\mu A/V$
$C_{D,opt}$	1.669	fF
AD	0.57	μm^2
PD	3.662	μm
C_{DBJ}	1.305	fF
C_F	0.524	fF
C_{out}	21.829	fF
GBW (check)	25	MHz
f_z	1.028	GHz
A_{dc}	50	dB

6.3 Simulations

We can now check whether we get the correct GBW and DC gain using ngspice simulations with the schematic shown in Figure 1.2. The simulations will be performed with the following parameters:

```
.param VDD=1.8 Ib=122n
.param CL=20.00f W=1.43u L=0.75u AD=5.72e-13 PD=3.66e-06
```

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 6.3.

Table 6.3: Operating point information.

Node	Voltage
vdd	1.8
in	0.4076
out	0.4076
1	0.4076
2	0.4076

The operating information for each transistor can be extracted and are given in Table 6.4 and Table 6.5.

Table 6.4: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[\mu A]$	I_{spec} $[\mu A]$	IC	n	V_{Dsat} $[mV]$
M1	0.122	1.597	0.076	1.27	118
M2	0.122	1.597	0.076	1.27	118

Table 6.5: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[\mu A/V]$
M1	1.27	4.390	3.400	0.980	0.010
M2	1.27	4.390	3.400	0.980	0.010

We see that the simulated transconductance of M_1 $G_m = 3.400\ \mu A/V$ is close to the theoretical estimation $G_m = 3.429\ \mu A/V$.

The transfer function magnitude and phase are plotted in Figure 6.1, which shows an almost perfect fit between the simulation and the theoretical estimation. The DC gain and gain-bandwidth product are right on target. Even the high frequency behavior is well captured because of the good estimation of the total gate-to-drain capacitance including the contribution of the gate transcapacitance.

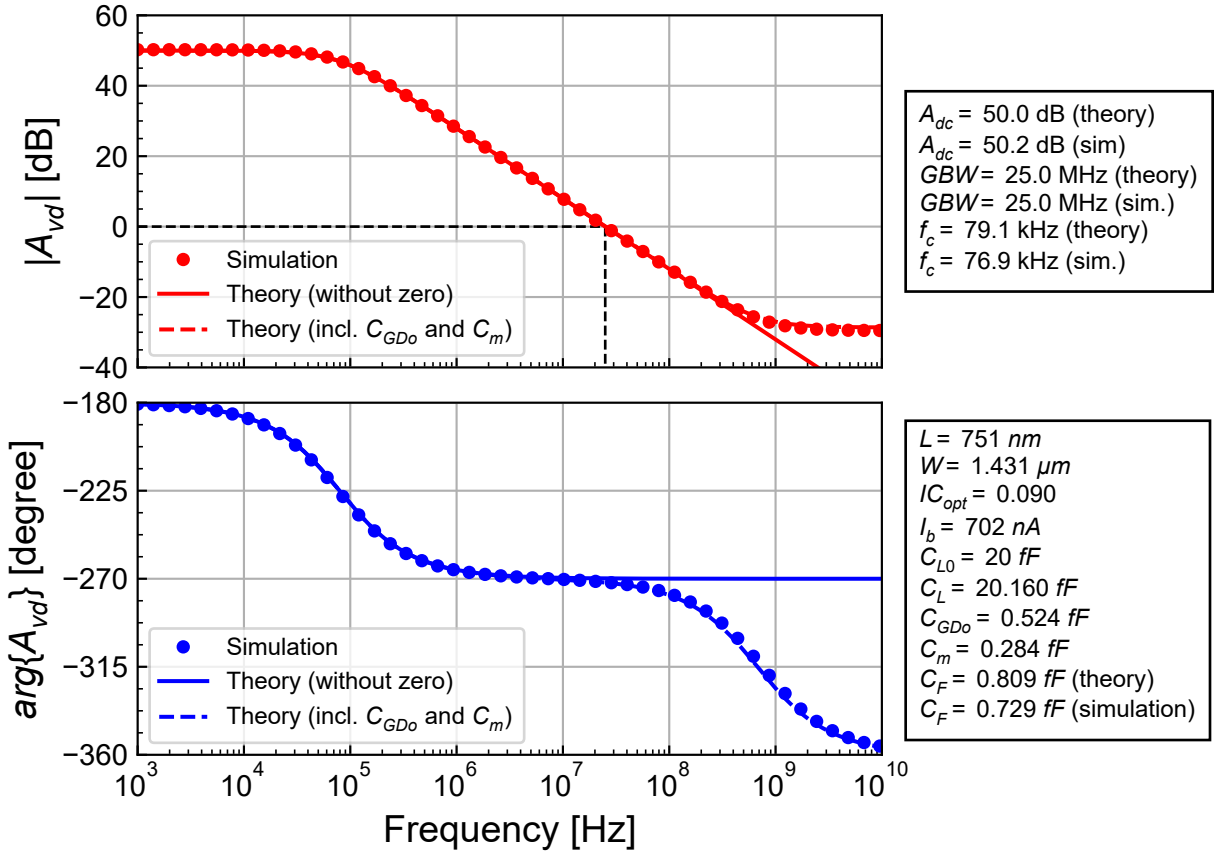

Figure 6.1: Simulated gain response compared to theoretical estimation for the long-channel case.

7 Conclusion

This exercise has shown various ways to design a single transistor setting its bias current and choosing its width and length for reaching different specifications. It has also illustrated the role of parasitic capacitances and how to estimate them. All the designs have been succesfully checked with simulations using ngspice and the EKV 2.6 compact model.

References

[1] C. Enz, "Common-source Open-loop Optimization." https://github.com/chrisenz/Analog-Circuit-Design/blob/main/Amplifiers/Basic/CS%20OL%20Optimization/CS_OL_optimization.pdf, 2025.

[2] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design*, 1st ed. John Wiley, 2006.