Fundamentals of Analog VLSI Design
Exercise 3 - Problem

Design and Optimization of the Common-source Gain Stage

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01.10.2025

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Introduction

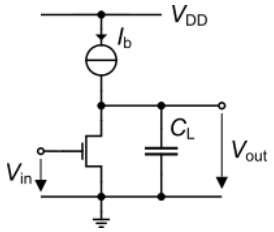

Figure 1: Common-source gain stage.

In this exercise we want to apply the G_m/I_D design methodology using the inversion coefficient IC to the simple common source amplifier shown in Figure 1 for various specifications. Most of these specifications are related to the transistor transconductance G_m. The exercise will show how to use the EKV functions related to the transconductance, in particular the normalized source transconductance which, for a long-channel transistor, only depends on the inversion coefficient according to

$$gms(IC) \triangleq \frac{G_{ms}}{G_{spec}} = \frac{G_m\, nU_T}{I_{spec}} = \frac{\sqrt{4IC+1}-1}{2}, \tag{0.1}$$

where $G_{spec} = I_{spec}/U_T$ is the specific conductance and $I_{spec} = I_D/IC$ is the specific current also given by $I_{spec} = I_{spec\square}\, W/L$.

In the case the drain current and inversion coefficient are imposed, you can get the transconductance from the normalized G_m/I_D function

$$gmid(IC) = \frac{G_m\, nU_T}{I_D} = \frac{G_{ms}\, U_T}{I_D} = \frac{gms(IC)}{IC} = \frac{\sqrt{4IC+1}-1}{2IC} \tag{0.2}$$

as

$$G_m = gmid(IC) \cdot \frac{I_D}{nU_T} \tag{0.3}$$

In the case the normalized transconductance is imposed, you can get the inversion coefficient by inverting (0.1) resulting in

$$IC = g_{ms} \cdot (g_{ms}+1). \tag{0.4}$$

In the case the transconductance and the current are given you can get the inversion coefficient from

$$IC = \frac{1-gmsid}{gmsid^2} \tag{0.5}$$

where

$$gmsid = \frac{G_m\, nU_T}{I_D} = \frac{G_{ms}\, U_T}{I_D} \tag{0.6}$$

For short-channel transistors we need to account for velocity saturation (VS). The normalized source transconductance and normalized G_m/I_D functions then become

$$gms(IC,\lambda_c) \triangleq \frac{G_{ms}}{G_{spec}} = \frac{G_m\, nU_T}{I_{spec}} = \frac{\sqrt{4IC+1+(\lambda_c\, IC)^2}-1}{2+\lambda_c^2\, IC}, \tag{0.7}$$

$$gmid(IC,\lambda_c) = \frac{G_m\, nU_T}{I_D} = \frac{G_{ms}\, U_T}{I_D} = \frac{gms(IC)}{IC} = \frac{\sqrt{4IC+1+(\lambda_c\, IC)^2}-1}{IC\,(2+\lambda_c^2\, IC)}, \tag{0.8}$$

where $\lambda_c = L_{sat}/L_{eff}$ is the VS parameter.

All the above EKV functions, and actually many more, are coded in python in the ekv_functions.py file.

For the design we assume a generic 180nm bulk CMOS process. The physical parameters are given in Table 1, the global process parameters in Table 2 and finally the MOSFET parameters in Table 3.

Table 1: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 2: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
H_{dif}	200	nm
W_{min}	200	nm
L_{min}	180	nm

Table 3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm

Table 3: Transistor process parameters

Parameter	NMOS	PMOS	Unit
ΔL	-76	-72	nm

Note that the effective channel width and length are defined as follows

$$W_{eff} \triangleq W + \Delta W, \tag{0.9}$$

$$L_{eff} \triangleq L + \Delta L, \tag{0.10}$$

where W and L are drawn width and length.

1 Problem 1: Imposing the gain bandwidth product (unity gain frequency)

Design the CS amplifier shown in Figure 1, for the specifications given in Table 1.1 at room temperature.

Table 1.1: Specifications for problem 1.

Specification	Symbol	Value	Unit
Gain-bandwidth product	GBW	10	MHz
Inversion coefficient	IC	1	-
Load capacitance	C_L	1	pF

Carry out the design procedure both for long- and short-channel devices in saturation, using the drawn lengths $L_{long} = 1\,\mu m$ and $L_{short} = 0.18\,\mu m$, respectively. Note that velocity saturation (VS) has to be accounted for in the short-channel case. We assume that the self-loading capacitance at the drain can be neglected (i.e. assume a constant load capacitance equal to C_L).

Carry out the design procedure following these steps:

- Draw the equivalent small-signal schematic ignoring the transistor parasitic capacitances.
- Derive the transfer function $A_v(s) \triangleq \Delta V_{out}/\Delta V_{in}$ and extract the expressions of the dc gain, cut-off frequency and gain-bandwidth product (unity gain frequency) f_u.
- Find the transistor transconductance value G_m.
- Find the normalized source transconductance $g_{ms}(IC) \triangleq G_{ms}/G_{spec} = n\,G_m/G_{spec} = nU_T\,G_m/I_{spec}$ from the imposed inversion coefficient IC. Then, deduce the specific current I_{spec} and the bias current I_b.
- Find the W_{eff}/L_{eff} ratio and the effective width W_{eff} for both the long and short channel case using the given drawn length L. Derive the drawn width W.
- Deduce the output conductance value G_{ds} and then calculate the dc gain value assuming the bias current source is ideal.
- Simulate the circuit using the ngspice simulator and compare the theoretical results with the simulations.

2 Problem 2: Imposing the power consumption

Design the CS amplifier shown in Figure 1, for the specifications given in Table 2.1 at room temperature.

Table 2.1: Specifications for problem 2.

Specification	Symbol	Value	Unit
Power consumption	P	20	μW
Inversion coefficient	IC	1	-
Load capacitance	C_L	1	pF

Carry out the design procedure both for long- and short-channel devices in saturation, using the drawn lengths $L_{long} = 1\,\mu m$ and $L_{short} = 0.18\,\mu m$, respectively. Note that velocity saturation (VS) has to be accounted for in the short-channel case. We assume that the self-loading capacitance at the drain can be neglected (i.e. assume a constant load capacitance C_L).

Carry out the design procedure following these steps:

- Find the bias current I_b for the specified maximum power consumption.
- Find the transconductance value of the transistor for the given inversion coefficient IC by means of the current efficiency.
- Find the gain-bandwidth product (unity gain frequency) using the specific current I_{spec}.
- Find the W_{eff}/L_{eff} ratio and the effective width W_{eff} for both the long and short channel case using the given drawn length L. Derive the drawn width W.
- Deduce the output conductance value G_{ds} and then calculate the dc gain value assuming the bias current source is ideal.
- Simulate the circuit using the ngspice simulator and compare the theoretical results with the simulations.

3 Problem 3: Imposing the gain bandwidth product and the current budget

Design the same CS amplifier shown in Figure 1 imposing both the gain-bandwidth product and the current budget with the specifications given in Table 3.1 at room temperature.

Table 3.1: Specifications for problem 3.

Specification	Symbol	Value	Unit
Gain-bandwidth product	GBW	1	MHz
Bias current	I_b	400	nA
Load capacitance	C_L	1	pF
Transistor length	L	1	μm

Carry out the design procedure only for the long-channel case with $L = L_{long} = 1\,\mu m$ following these steps:

- Find the transistor transconductance value.
- Find the inversion coefficient IC by means of the current efficiency and then the specific current I_{spec}.
- Find the W_{eff}/L_{eff} ratio and the effective width W_{eff} for the long channel case only using the given drawn length L. Derive the drawn width W.
- Deduce the output conductance value G_{ds} and then calculate the dc gain value assuming the bias current source is ideal.
- Simulate the circuit using the ngspice simulator and compare the theoretical results with the simulations.

4 Problem 4: Imposing the input-referred noise

In this problem we want to design the CS amplifier shown in Figure 1 imposing the input-referred noise including both the thermal and flicker noise. The specifications at room temperature are given in Table 4.1.

Table 4.1: Specifications for problem 4.

Specification	Symbol	Value	Unit
Corner frequency	f_k	100	kHz
Input referred white PSD	$\sqrt{S_{n,th}}$	30	$\frac{nV}{\sqrt{Hz}}$
	$10\ \log(S_{n,th})$	-150.46	$\frac{dBv}{\sqrt{Hz}}$
Inversion coefficient	IC	1	-
Load capacitance	C_L	1	pF

Carry out the design procedure following these steps:

- Using S_{nth} determine the transconductance G_m.
- Find the normalized transconductance $g_{ms}(IC)$.
- Determine the specific current I_{spec}, the bias current I_b and the W_{eff}/L_{eff} ratio.
- Using the noise corner frequency f_k, determine the effective gate area $W_{eff} \cdot L_{eff}$.
- Finally, calculate the effective and drawn dimensions of the transistor.
- Simulate the circuit using the ngspice simulator and compare the theoretical results with the simulations.

5 Problem 5: Minimum current for a given gain-bandwidth product with self-loading

In this problem we want to account for the self-loading effect which is particularly important when the transistor is getting wide as it typically happens in weak inversion. The specifications at room temperature are given in Table 5.1.

Table 5.1: Specifications for problem 5.

Specification	Symbol	Value	Unit
Gain-bandwidth product	GBW	25	MHz
Load capacitance	C_{L0}	20	fF
Transistor length	L	1	μm

Follow the procedure illustrated in the lecture notes.

Simulate your design and check whether it meets the specifications.

6 Problem 6: Minimum current for a given DC gain and gain-bandwidth product with self-loading

In this problem we want to account for the self-loading effect but use the additional degree of freedom, namely the transistor gate length, to set the dc gain. The specifications at room temperature are given in Table 6.1.

Table 6.1: Specifications for problem 6.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	50	dB
Gain-bandwidth product	GBW	25	MHz
Load capacitance	C_{L0}	20	fF

Follow the procedure illustrated in the lecture notes.

Simulate your design and check whether it meets the specifications.