

Fundamentals of Analog VLSI Design

Exercise 2 - Solution

Differential pair - Inverter - Velocity saturation

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1 Problem 1: The differential pair

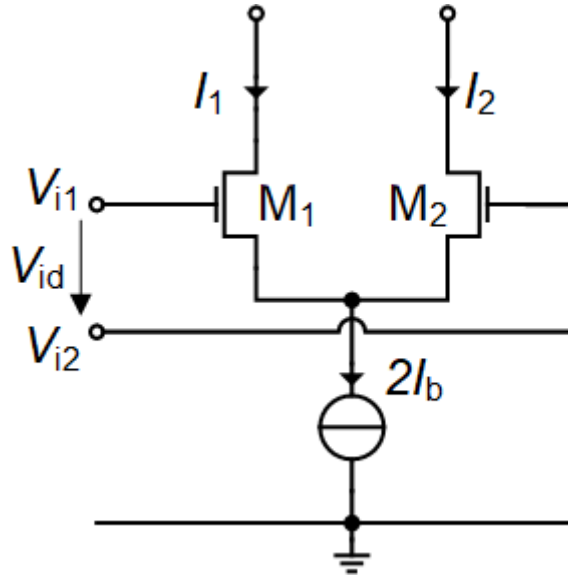


Figure 1.1: Differential pair schematic.

1.1 Both transistors in weak inversion

1.1.1 Large-signal characteristic

In the following analysis, we will assume that M_1 and M_2 are perfectly matched, leading to

$$V_{T01} = V_{T02} = V_{T0}, \quad (1.1)$$

$$I_{D01} = I_{D02} = I_{D0}, \quad (1.2)$$

$$n_1 = n_2 = n. \quad (1.3)$$

In the case both transistors are biased in weak inversion and saturation and since the bulks of M_1 and M_2 are connected to the ground, the drain currents are then given by

$$I_1 = I_{D0} \cdot e^{\frac{V_{i1} - nV_S}{nU_T}}, \quad (1.4)$$

$$I_2 = I_{D0} \cdot e^{\frac{V_{i2} - nV_S}{nU_T}}. \quad (1.5)$$

The differential output current is then given by

$$I_{od} \triangleq I_1 - I_2 = I_{D0} \cdot e^{-\frac{V_S}{U_T}} \cdot \left[e^{\frac{V_{i1}}{nU_T}} - e^{\frac{V_{i2}}{nU_T}} \right]. \quad (1.6)$$

Now, the sum of I_1 and I_2 is set by the bottom current source

$$I_1 + I_2 = 2I_b, \quad (1.7)$$

leading to

$$2I_b = I_{D0} \cdot e^{-\frac{V_S}{U_T}} \cdot \left[e^{\frac{V_{i1}}{nU_T}} + e^{\frac{V_{i2}}{nU_T}} \right] \quad (1.8)$$

from which we get

$$I_{D0} \cdot e^{-\frac{V_S}{U_T}} = \frac{2I_b}{e^{\frac{V_{i1}}{nU_T}} + e^{\frac{V_{i2}}{nU_T}}} \quad (1.9)$$

Replacing (1.9) in (1.6) results in

$$I_{od} = 2I_b \cdot \frac{e^{\frac{V_{i1}}{nU_T}} - e^{\frac{V_{i2}}{nU_T}}}{e^{\frac{V_{i1}}{nU_T}} + e^{\frac{V_{i2}}{nU_T}}}. \quad (1.10)$$

The input voltages can be written in terms of the differential and common mode voltages according to

$$V_{i1} = V_{ic} + \frac{V_{id}}{2}, \quad (1.11)$$

$$V_{i2} = V_{ic} - \frac{V_{id}}{2}. \quad (1.12)$$

Replacing in (1.10) results in

$$I_{od} = 2I_b \cdot \frac{e^{\frac{V_{id}}{2nU_T}} - e^{-\frac{V_{id}}{2nU_T}}}{e^{\frac{V_{id}}{2nU_T}} + e^{-\frac{V_{id}}{2nU_T}}} = 2I_b \cdot \tanh\left(\frac{V_{id}}{2nU_T}\right). \quad (1.13)$$

The differential output current I_{od} normalized to $2I_b$ can then be written as

$$i_{od} \triangleq \frac{I_{od}}{2I_b} = \tanh(v_{id}), \quad (1.14)$$

where $v_{id} \triangleq V_{id}/(2nU_T)$.

1.1.2 Small-signal characteristic

The small-signal transconductance is defined by

$$G_m \triangleq \frac{dI_{od}}{dV_{id}} = G_{m0} \cdot \left[1 - \tanh^2\left(\frac{V_{id}}{2nU_T}\right) \right] \quad (1.15)$$

where G_{m0} is the transconductance for $V_{id} = 0$

$$G_{m0} = \frac{I_b}{nU_T}. \quad (1.16)$$

The maximum transconductance G_{m0} of the differential pair therefore corresponds to the transconductance of a single transistor for $V_{id} = 0$ (i.e. when $I_1 = I_2 = I_b$).

The small-signal transconductance normalized to G_{m0} is then given by

$$g_m \triangleq \frac{G_m}{G_{m0}} = 1 - \tanh^2(v_{id}). \quad (1.17)$$

The normalized differential output current i_{od} and normalized transconductance g_m are plotted below versus the normalized differential input voltage v_{id}

From Figure 1.2, we see that the large-signal nonlinear characteristic can be approximated by a piecewise linear characteristic where the middle part has the slope of the nonlinear characteristic at $v_{id} = 0$. The linear range can then be defined as the input voltage covered by the middle linear characteristic. In weak inversion the linear range is about $4nU_T$ which is about 135 mV at room temperature for $n = 1.3$. This is rather small.

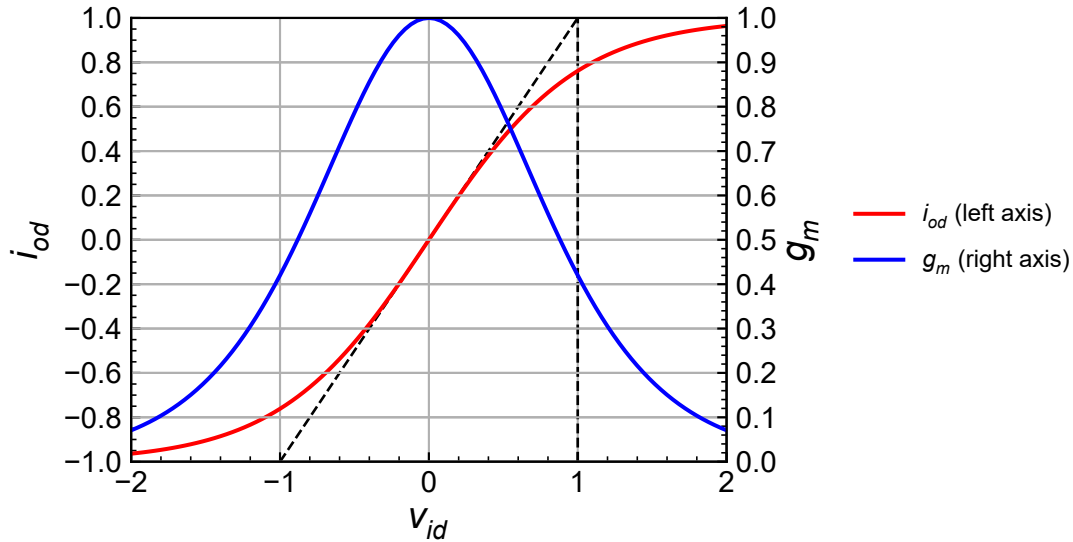


Figure 1.2: Differential current i_{od} and transconductance g_m versus differential input voltage v_{id} for both transistors M_1 and M_2 biased in weak inversion and saturation.

1.2 Both transistors in strong inversion

1.2.1 Large-signal characteristic

We again will assume that the two transistors are perfectly matched, which means that

$$V_{T01} = V_{T02} = V_{T0}, \quad (1.18)$$

$$\beta_1 = \beta_2 = \beta, \quad (1.19)$$

$$n_1 = n_2 = n. \quad (1.20)$$

In the case both transistors are biased in strong inversion and saturation and since the bulks of M_1 and M_2 are connected to the ground, the drain currents are given by

$$I_1 = \frac{\beta}{2n} \cdot (V_{i1} - V_{T0} - n V_S)^2, \quad (1.21)$$

$$I_2 = \frac{\beta}{2n} \cdot (V_{i2} - V_{T0} - n V_S)^2, \quad (1.22)$$

where V_S is the voltage of the common source node. Solving the above equations together with

$$I_{od} = I_1 - I_2, \quad (1.23)$$

$$I_1 + I_2 = 2I_b, \quad (1.24)$$

$$V_{i1} = V_{ic} + \frac{V_{id}}{2}, \quad (1.25)$$

$$V_{i2} = V_{ic} - \frac{V_{id}}{2}, \quad (1.26)$$

$$V_{id} = V_{i1} - V_{i2}, \quad (1.27)$$

leads to

$$I_{od} = V_{id} \cdot \sqrt{\frac{\beta}{2nI_b}} \cdot \sqrt{1 - \frac{\beta}{2nI_b} \cdot \left(\frac{V_{id}}{2}\right)^2} \quad (1.28)$$

valid for

$$|V_{id}| < 2\sqrt{\frac{2nI_b}{\beta}} = 2(V_{ic} - V_{T0} - V_S). \quad (1.29)$$

The differential output current I_{od} can be normalized to the maximum output current $2I_b$

$$i_{od} \triangleq \frac{I_{od}}{2I_b} = v_{id} \cdot \sqrt{1 - \left(\frac{v_{id}}{2}\right)^2}, \quad (1.30)$$

valid for

$$|v_{id}| < \sqrt{2}, \quad (1.31)$$

where

$$v_{id} \triangleq \frac{V_{id}}{\sqrt{2nI_b/\beta}} = \frac{V_{id}}{V_G - V_{T0} - nV_S}. \quad (1.32)$$

1.2.2 Small-signal transconductance

The small-signal transconductance is defined as

$$G_m \triangleq \frac{dI_{od}}{dV_{id}}, \quad (1.33)$$

which is given by

$$G_m = G_{m0} \cdot \frac{2 - v_{id}^2}{\sqrt{4 - v_{id}^2}}, \quad (1.34)$$

where

$$G_{m0} = \sqrt{\frac{2\beta I_b}{n}} \quad (1.35)$$

is the transconductance for $V_{id} = 0$ which also corresponds to the transconductance of M_1 or M_2 for $V_{id} = 0$.

The large-signal normalized differential output current and the normalized transconductance are plotted versus v_{id} in Figure 1.3.

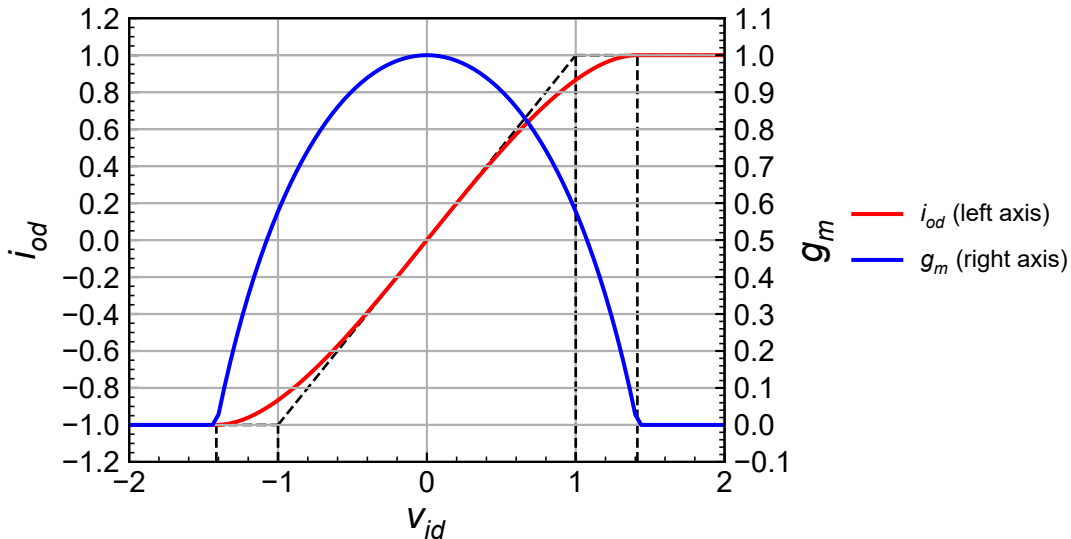


Figure 1.3: Differential current i_{od} and transconductance g_m versus differential input voltage v_{id} for both transistors M_1 and M_2 biased in strong inversion and saturation.

Similarly to what has been done in weak inversion we can approximate the nonlinear characteristic by a piecewise linear model as shown in Figure 1.3. The linear range is now proportional to the overdrive voltage according to $2(V_G - V_{T0} - nV_S)$, which is much larger than what we get in weak inversion. We can therefore make the differential pair more linear by increasing the overdrive voltage. However, this comes at the cost of a reduced current efficiency G_m/I_b .

1.3 Optional: Both transistors in any modes of operation (saturation)

1.3.1 Large-signal characteristic

We can use the EKV charge-based model to express the gate voltages of M_1 and M_2 in terms of q_{s1} and q_{s2} according to

$$\frac{V_{i1} - V_{T0} - n V_S}{n U_T} = 2q_{s1} + \ln(q_{s1}), \quad (1.36)$$

$$\frac{V_{i2} - V_{T0} - n V_S}{n U_T} = 2q_{s2} + \ln(q_{s2}). \quad (1.37)$$

If we want to be consistent with the analysis of the differential pair in weak inversion we need to use the same normalization. This means that the voltages need to be normalized to $2nU_T$, leading to

$$v_{i1} - v_{t0n} - v_s = q_{s1} + \frac{1}{2} \ln(q_{s1}), \quad (1.38)$$

$$v_{i2} - v_{t0n} - v_s = q_{s2} + \frac{1}{2} \ln(q_{s2}), \quad (1.39)$$

where

$$v_{i1} \triangleq \frac{V_{i1}}{2nU_T}, \quad (1.40)$$

$$v_{i2} \triangleq \frac{V_{i2}}{2nU_T}, \quad (1.41)$$

$$v_s \triangleq \frac{V_S}{2nU_T}. \quad (1.42)$$

The normalized differential input voltage v_{id} is then given by subtracting (1.39) to (1.38) resulting in

$$v_{id} \triangleq \frac{V_{id}}{2nU_T} = v_{i1} - v_{i2} = q_{s1} - q_{s2} + \frac{1}{2} \ln\left(\frac{q_{s1}}{q_{s2}}\right) \quad (1.43)$$

We need to be careful with the normalization of the currents. In order to have the output differential current $I_{od} = I_1 - I_2$ normalized to the maximum output current $2I_b$, like it was done for the analysis in weak and strong inversion, we need to define the normalized currents i_1 , i_2 and i_{od} as

$$i_1 \triangleq \frac{I_1}{2I_b}, \quad (1.44)$$

$$i_2 \triangleq \frac{I_2}{2I_b}, \quad (1.45)$$

$$i_{od} \triangleq \frac{I_{od}}{2I_b} = \frac{I_1 - I_2}{2I_b} = i_1 - i_2. \quad (1.46)$$

The normalized source charges q_{s1} and q_{s2} are related to the normalized drain currents i_{d1} and i_{d2} according to

$$i_{d1} \triangleq \frac{I_1}{I_{spec}} = q_{s1} \cdot (q_{s1} + 1), \quad (1.47)$$

$$i_{d2} \triangleq \frac{I_2}{I_{spec}} = q_{s2} \cdot (q_{s2} + 1). \quad (1.48)$$

Notice that i_1 and i_2 are different than i_{d1} and i_{d2} since the former are normalized to $2I_b$, whereas the latter are normalized to I_{spec} . They are related according to

$$i_1 = \frac{i_{d1}}{2IC_q}, \quad (1.49)$$

$$i_2 = \frac{i_{d2}}{2IC_q}, \quad (1.50)$$

where

$$IC_q \triangleq \frac{I_b}{I_{spec}} \quad (1.51)$$

corresponds to the inversion coefficient of M_1 and M_2 at the quiescent operating point, i.e. for $V_{id} = 0$.

Solving the above set of equations for q_{s1} and q_{s2} results in

$$q_{s1} = \frac{\sqrt{4IC_q(1+i_{od})+1}-1}{2}, \quad (1.52)$$

$$q_{s2} = \frac{\sqrt{4IC_q(1-i_{od})+1}-1}{2}. \quad (1.53)$$

We can now sweep the normalized differential output current for a given IC_q and then calculate q_{s1} and q_{s2} according to (1.52) and (1.53) and use them to calculate v_{id} according to (1.43). The result is plotted in Figure 1.4 for different IC_q .

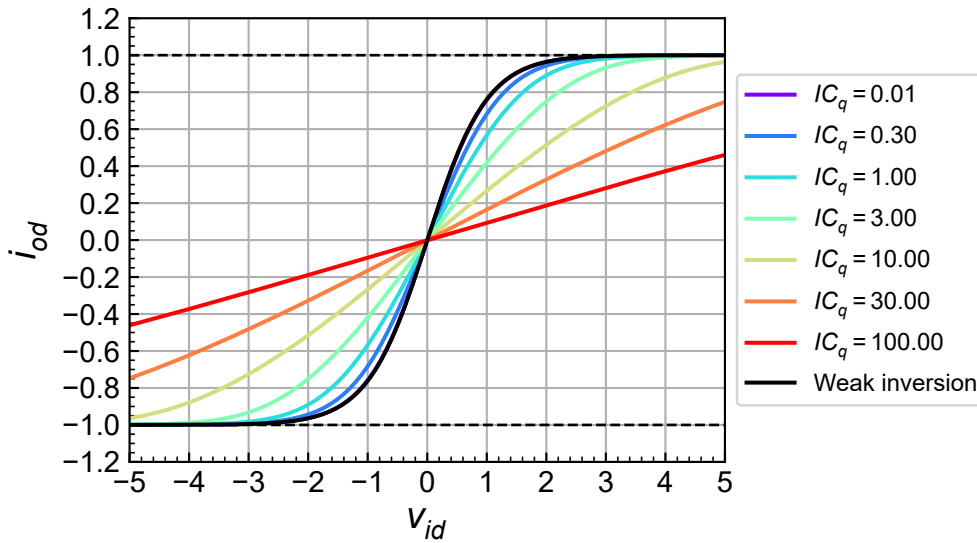


Figure 1.4: Differential current i_{od} versus differential input voltage v_{id} valid in all regions of operation (assuming M_1 and M_2 in saturation).

We clearly see that increasing the inversion coefficient IC_q from weak inversion to strong inversion extends the linear range from $4nU_T$ to $2(V_{ic} - V_{T0} - nV_S)$, where $V_{ic} \triangleq (V_{i1} + V_{i2})/2$ is the input common-mode voltage. However this comes at the cost of a reduced transconductance efficiency G_{m0}/I_b .

1.3.2 Small-signal transconductance

In the previous section we have derived an expression of V_{id} in terms of q_{s1} and q_{s2} which depend on I_{od} . We can derive the transconductance by differentiating V_{id} wrt I_{od}

$$\frac{dV_{id}}{dI_{od}} = \frac{1}{G_m} \quad (1.54)$$

or in normalized form

$$\frac{dv_{id}}{di_{od}} \cdot \frac{2nU_T}{2I_b} = \frac{1}{G_m}. \quad (1.55)$$

The transconductance can then be written as

$$G_m \cdot \frac{nU_T}{I_b} = \left(\frac{dv_{id}}{di_{od}}\right)^{-1} = \frac{di_{od}}{dv_{id}} = g_m. \quad (1.56)$$

so that

$$g_m \triangleq \frac{di_{od}}{dv_{id}} = \frac{G_m}{I_b/(nU_T)}. \quad (1.57)$$

It can be shown that

$$g_m = \frac{4}{IC_q} \cdot \frac{q_{s1} \cdot q_{s2}}{q_{s1} + q_{s2}} \quad (1.58)$$

with q_{s1} and q_{s2} given by (1.52) and (1.53).

Now, we want to plot g_m normalized to its value at $v_{id} = 0$

$$g_{m0} \triangleq g_m(v_{id} = 0). \quad (1.59)$$

For $v_{id} = 0$, we have $i_{od} = 0$ and from (1.52) and (1.53), we get

$$q_s \triangleq q_{s1}|_{v_{id}=0} = q_{s2}|_{v_{id}=0} = \frac{\sqrt{4IC_q + 1} - 1}{2}. \quad (1.60)$$

g_{m0} can therefore be written as

$$g_{m0} = \frac{q_s}{IC_q} = \frac{\sqrt{4IC_q + 1} - 1}{2IC_q}. \quad (1.61)$$

The transconductance normalized to the value it takes at $v_{id} = 0$ is therefore given by

$$\frac{G_m}{G_{m0}} = \frac{g_m}{g_{m0}} = \frac{2}{q_s} \cdot \frac{q_{s1} \cdot q_{s2}}{q_{s1} + q_{s2}} \quad (1.62)$$

with q_s , q_{s1} and q_{s2} given by (1.60), (1.52) and (1.53), respectively.

The normalized transconductance g_m is plotted versus the normalized differential input voltage v_{id} in Figure 1.5 for different values of the inversion coefficient IC_q .

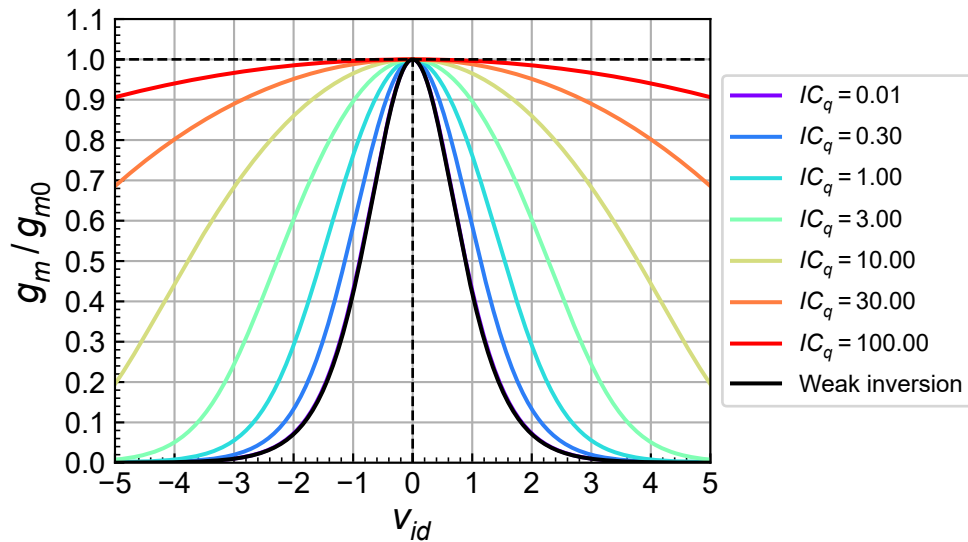


Figure 1.5: Transconductance normalized to its value at $v_{id} = 0$ versus differential input voltage v_{id} valid in all regions of operation (assuming M_1 and M_2 in saturation).

2 Problem 2: The inverter as a transconductance amplifier

2.1 Analysis

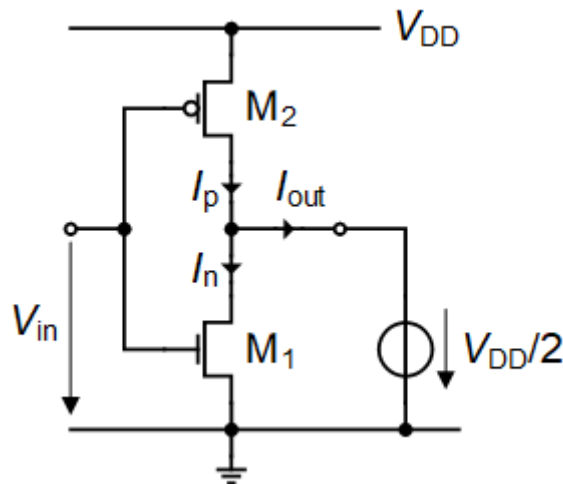


Figure 2.1: The CMOS inverter.

Assuming that both transistors are biased in weak inversion and saturation, the drain currents are then given by

$$I_n = I_{D0n} \cdot e^{\frac{V_{in}}{n_n U_T}}, \quad (2.1)$$

$$I_p = I_{D0p} \cdot e^{\frac{V_{DD} - V_{in}}{n_p U_T}}, \quad (2.2)$$

where

$$I_{D0n} = I_{specn} \cdot e^{\frac{-V_{T0n}}{n_n U_T}}, \quad (2.3)$$

$$I_{D0p} = I_{specp} \cdot e^{\frac{-V_{T0p}}{n_p U_T}}, \quad (2.4)$$

with

$$I_{specn} = I_{specn\Box} \cdot \frac{W_n}{L_n}, \quad (2.5)$$

$$I_{specp} = I_{specp\Box} \cdot \frac{W_p}{L_p}. \quad (2.6)$$

Defining V_b as the quiescent input voltage such that the output current is zero and hence $I_p = I_n = I_b$ we can write

$$I_b = I_{D0n} \cdot e^{\frac{V_b}{n_n U_T}} = I_{D0p} \cdot e^{\frac{V_{DD} - V_b}{n_p U_T}}. \quad (2.7)$$

We can then express I_{D0n} and I_{D0p} as

$$I_{D0n} = I_b \cdot e^{\frac{-V_b}{n_n U_T}}, \quad (2.8)$$

$$I_{D0p} = I_b \cdot e^{\frac{V_b - V_{DD}}{n_p U_T}}. \quad (2.9)$$

Replacing (2.8) and (2.9) in (2.1) and (2.2) results in

$$I_n = I_b \cdot e^{\frac{V_{in} - V_b}{n_n U_T}}, \quad (2.10)$$

$$I_p = I_b \cdot e^{-\frac{V_{in} - V_b}{n_p U_T}}, \quad (2.11)$$

The output current can then be written as

$$I_{out} = I_p - I_n = I_b \cdot \left[e^{-\frac{V_{in} - V_b}{n_n U_T}} - e^{\frac{V_{in} - V_b}{n_n U_T}} \right]. \quad (2.12)$$

Assuming that $n_n = n_p = n$, the normalized output current can be written as

$$i_{out} \triangleq \frac{I_{out}}{I_b} = -2 \sinh(v_{in} - v_b) \quad (2.13)$$

where $v_{in} \triangleq V_{in}/(nU_T)$ and $v_b \triangleq V_b/(nU_T)$.

The normalized output current is plotted in Figure 2.2 together with the currents of the nMOS and pMOS transistors. We see that the current is ideally not limited hence the inverter can operate as a class AB transconductance amplifier. Contrary to the differential pair where the output current is limited by the bias current $2I_b$, the output current of the inverter can be much larger than the bias current I_b flowing in M_1 and M_2 for $V_{in} = V_b$. The current will actually be limited by the supply voltage and the supply series resistances.

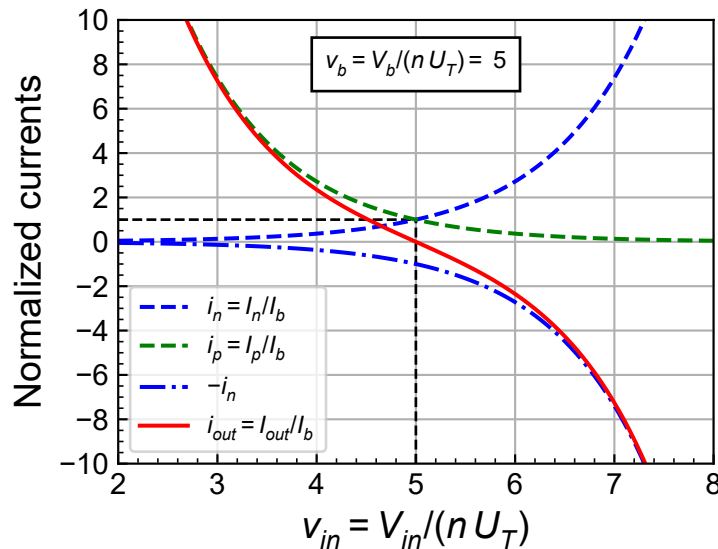


Figure 2.2: The inverter large-signal transfer characteristic in weak inversion.

2.2 Design

We want to design a CMOS inverter to be used as a transconductance amplifier. For this we use the schematic of Figure 2.3. In addition to the CMOS inverter made of M_1 and M_2 , this circuit includes

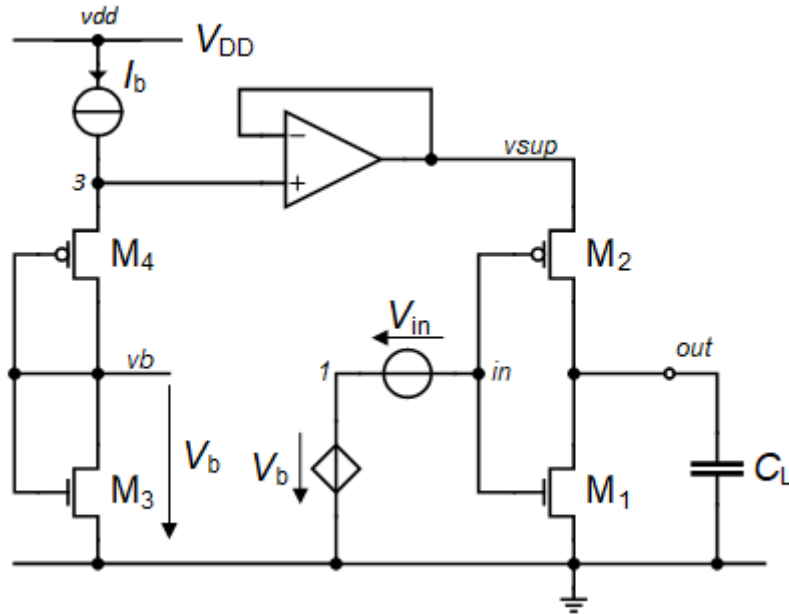


Figure 2.3: Schematic of the CMOS inverter used for simulation.

a bias circuit made of M_3 , M_4 , the current source setting the bias current I_b and the OPAMP. The bias circuit is used to properly set the operating point of circuit in quiescent state, i.e. when $V_{in} = 0$. This is needed to control the current and therefore the inverter small-signal transconductance. The bias current imposes the current to the diode-connected transistors M_3 and M_4 which are made identical to M_1 and M_2 , respectively. This generates the required bias voltage V_b to apply at the gates of M_1 and M_2 for their quiescent current to be equal to I_b provided the supply voltage applied to the CMOS inverter is equal to the voltage at the source of M_4 (node 3). This is realized with the OPAMP which sets the supply voltage V_{sup} to be equal to the voltage at node 3 and ensures that the bias current flowing in M_1 and M_2 is equal to I_b .

The specifications for the CMOS inverter are given in Table 2.1. We will design it for a generic 180nm bulk CMOS process. The physical parameters are given in Table 2.2, the global process parameters in Table 2.3 and finally the MOSFET parameters in Table 2.4.

Table 2.1: Specifications for the CMOS inverter.

Specification	Symbol	Value	Unit
Gain-bandwidth product	GBW	2	MHz
Load capacitance	C_L	1	pF
Length of M_1	L_1	0.5	μm
Length of M_2	L_2	0.5	μm

Table 2.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 2.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 2.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\Box}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	mV · μm
A_β	1	1	% · μm
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

To bias M_1 and M_2 in weak inversion, we choose an inversion coefficient of $IC_1 = IC_2 = 0.1$. The gain-bandwidth product GBW is set by the inverter transconductance G_{meq} and the load capacitance C_L according to

$$GBW = \frac{G_{meq}}{2\pi C_L}, \quad (2.14)$$

where the inverter transconductance G_{meq} is simply the sum of the nMOS and pMOS transconductances

$$G_{meq} = G_{m1} + G_{m2} \quad (2.15)$$

In weak inversion, the two transconductances are given by

$$G_{m1} = \frac{I_b}{n_1 U_T}, \quad (2.16)$$

$$G_{m2} = \frac{I_b}{n_2 U_T}. \quad (2.17)$$

and hence

$$G_{meq} = \frac{I_b}{U_T} \left(\frac{1}{n_1} + \frac{1}{n_2} \right). \quad (2.18)$$

If the slope factors can be considered as equal $n_1 = n_2 = n$, then $G_{m1} = G_{m2}$. Accounting for the fact that M_1 and M_2 are not biased in deep weak inversion we have

$$G_{meq} = \frac{I_b}{U_T} \left(\frac{gmsid(IC_1)}{n_1} + \frac{gmsid(IC_2)}{n_2} \right), \quad (2.19)$$

where

$$gmsid = \frac{G_m n U_T}{I_D} \quad (2.20)$$

is the normalized G_m/I_D function. In our case $IC_1 = IC_2 = IC$ and hence

$$G_{meq} = \frac{I_b gmsid(IC)}{U_T} \left(\frac{1}{n_1} + \frac{1}{n_2} \right), \quad (2.21)$$

We can then deduce the bias current as

$$I_b = \frac{G_{meq} U_T}{gmsid(IC) (1/n_1 + 1/n_2)} \quad (2.22)$$

The bias current is set to $I_b = 229 \text{ nA}$. We can now get the specific currents as $I_{spec1} = I_b/IC_1 = 2.287 \text{ } \mu\text{A}$ and $I_{spec2} = I_b/IC_2 = 2.287 \text{ } \mu\text{A}$ from which we deduce the aspect ratios $W_1/L_1 = 3.198$ and $W_2/L_2 = 13.207$. Knowing the length we get the width $W_1 = 1.60 \text{ } \mu\text{m}$ and $W_2 = 6.60 \text{ } \mu\text{m}$.

2.3 Simulation

2.3.1 DC transfer characteristic

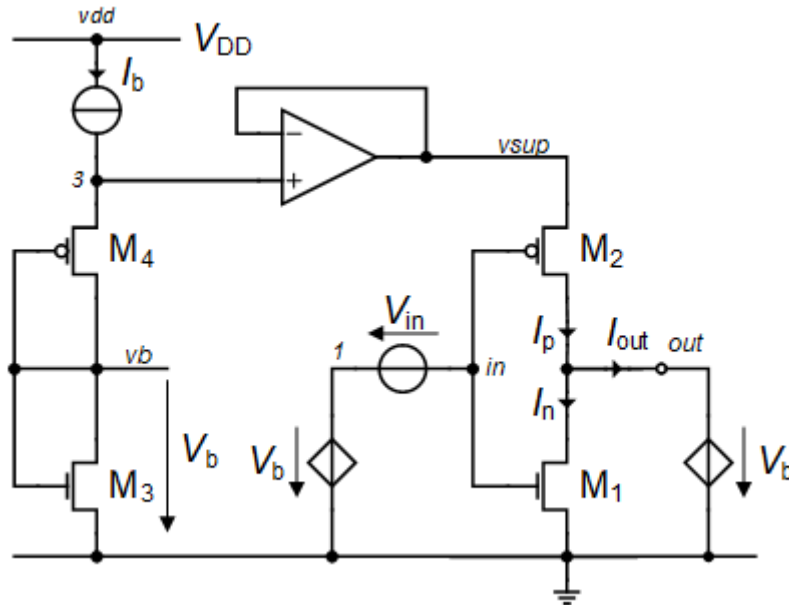


Figure 2.4: Schematic of the CMOS inverter used for the of the DC transfer characteristic.

To simulate the DC transfer characteristic I_{out} versus V_{in} , we will use the schematic shown in Figure 2.4. We first check the operating point looking at the quiescent voltages which are presented in Table 2.5.

Table 2.5: Operating point information.

Node	Voltage
vdd	1.8
vsup	0.826433
vb	0.418316
out	0.418316
1	0.418316
2	0.418316
3	0.826434
d1	0.418316
d2	0.418316

The large-signal transfer characteristic is shown in Figure 2.5.

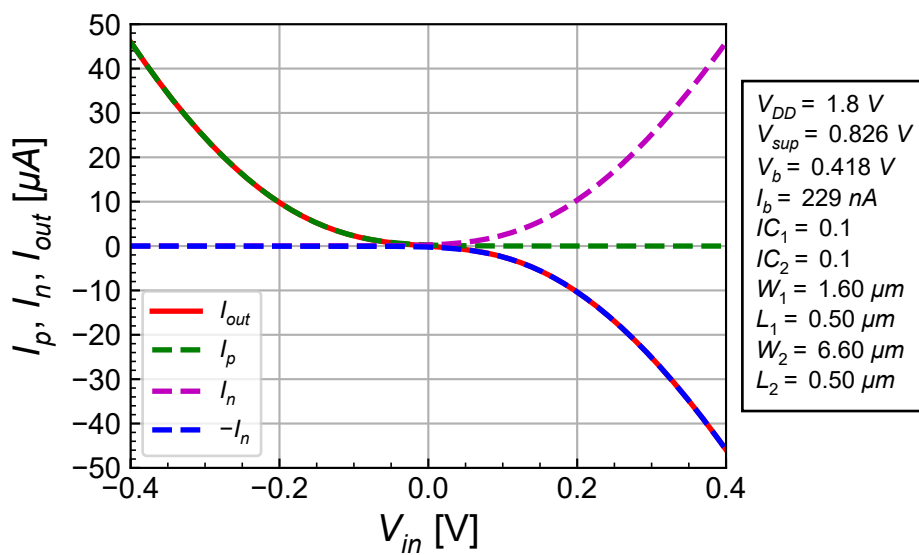


Figure 2.5: Simulated large-signal input-output characteristic.

Figure 2.5 clearly illustrates the class AB operation of the CMOS inverter and its ability to deliver an output current that is much larger than the bias current. We can zoom into the region close to the operating as shown in Figure 2.6.

2.3.2 Open-loop transfer function

We can also simulate the open-loop transfer function which is plotted in Figure 2.7 and compared to the theoretical estimation. We see that the gain-bandwidth product perfectly matches the simulation and is right on target. The simulated DC gain is slightly larger than the theoretical estimation. This simply comes from the simple output conductance model which is not very accurate.

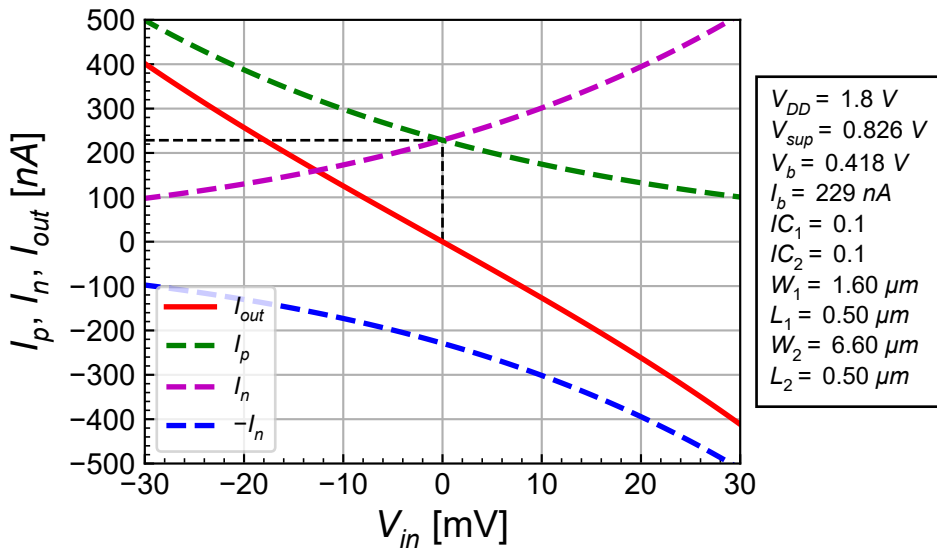


Figure 2.6: Simulated large-signal input-output characteristic.

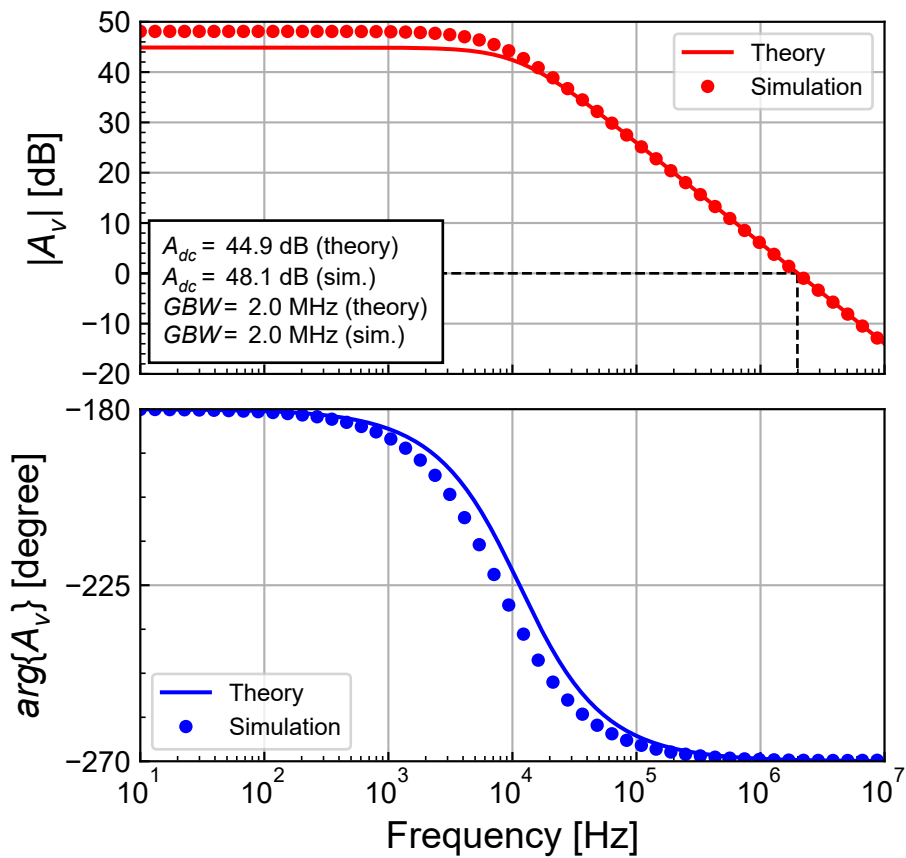


Figure 2.7: Simulated gain response compared to theoretical estimation.

3 Problem 3: Effect of velocity saturation on the gate transconductance

3.1 Strong inversion

For the strong inversion case we assume a bias current $I_b = 20 \mu A$, an inversion coefficient $IC = 30$ and load capacitance $C_L = 1 pF$.

3.1.1 Long-channel case

For the long-channel case the normalized source transconductance is given by

$$g_{ms} = \frac{\sqrt{4IC + 1} - 1}{2}, \quad (3.1)$$

which for the given inversion coefficient $IC = 30$ gives $g_{ms} \triangleq G_m/G_{spec} = 5$. Knowing the bias current $I_b = 20 \mu A$ and the inversion coefficient $IC = 30$, we can deduce the specific current as $I_{spec} = I_b/IC = 667 nA$. The gate transconductance is then given by

$$G_m = G_{spec} \cdot \frac{g_{ms}}{n} = \frac{I_{spec}}{n \cdot U_T} \cdot g_{ms}, \quad (3.2)$$

which is equal to $G_m = 128.2 \mu A/V$. The corresponding bandwidth is then given by $BW = G_m/(2\pi C_L) = 20.4 MHz$.

3.1.2 Short-channel case

For the short-channel case, the normalized source transconductance now also depends on the velocity saturation parameter λ_c according to

$$g_{ms} = \frac{\sqrt{4IC + 1 + (\lambda_c IC)^2} - 1}{2 + \lambda_c^2 IC}. \quad (3.3)$$

For $\lambda_c = 0.333$ and $IC = 30$, we get $g_{ms} = 2.600$. Keeping the same current $I_b = 20 \mu A$ and inversion coefficient $IC = 30$ and assuming that I_{spec} remains the same, we get $G_m = I_{spec}/(nU_T) \cdot g_{ms} = 66.664 \mu A/V$, which is 1.923 times smaller than what we get for the long-channel case. The corresponding bandwidth is now reduced accordingly to $BW = G_m/(2\pi C_L) = 10.6 MHz$.

3.2 Weak inversion

In the case of weak inversion we assume an inversion coefficient $IC = 0.1$, a bias current $I_b = 100 nA$ and a load capacitance $C_L = 0.1 pF$.

3.2.1 Long-channel case

For the long-channel case the normalized source transconductance is given by $g_{ms} \triangleq G_m/G_{spec} = 0.092$. Knowing the bias current $I_b = 100 \mu A$ and the inversion coefficient $IC = 0.1$, we can deduce the specific current as $I_{spec} = I_b/IC = 1 \mu A$. The gate transconductance is then given by $G_m = 3.523 \mu A/V$ and the corresponding bandwidth is equal to $BW = G_m/(2\pi C_L) = 5.6 MHz$.

3.2.2 Short-channel case

For the short-channel case, the normalized source transconductance is given by $g_{ms} = 0.091$ which is almost equal to what we got for the long-channel case in weak inversion. This is expected since velocity saturation has no effect in weak inversion.

Keeping the same current $I_b = 100 nA$ and inversion coefficient $IC = 0.1$ and assuming that I_{spec} remains the same, we get $G_m = I_{spec}/(nU_T) \cdot g_{ms} = 3.513 \mu A/V$, which is about equal to what we got for the long-channel case. The corresponding bandwidth is also unchanged $BW = G_m/(2\pi C_L) = 5.6 MHz$.

This example shows that velocity saturation reduces the transconductance that we get for a given current and inversion coefficient. For best current efficiency, we should move to moderate or even weak inversion to avoid the effect of velocity saturation. Now, moving the operating point to weak inversion results in a much lower transconductance and therefore bandwidth for a given capacitance. It also leads to large transistors and large parasitics.