# Fundamentals of Analog VLSI Design
# Exercise 6 - Problem

**The Fully Differential $G_m$-R Gain Stage**

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# 1 Introduction

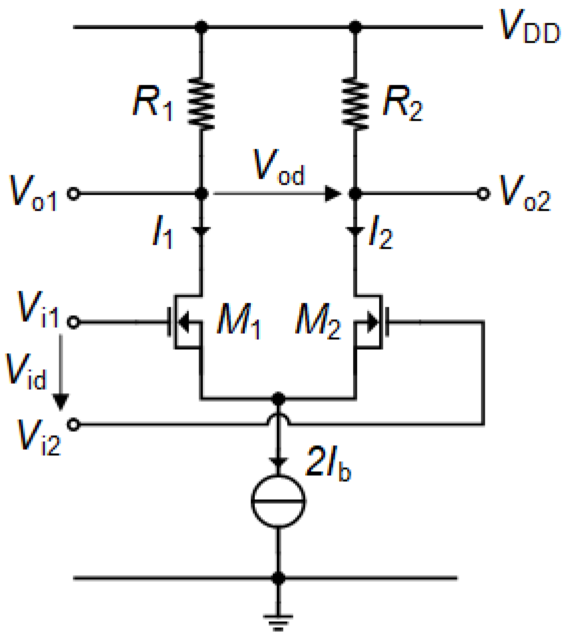


Figure 1.1: Schematic of the differential pair with resistive load.

Figure 1.1 shows a differential pair composed of two NMOS transistors $M_1$ and $M_2$, loaded with resistors $R_1$ and $R_2$, respectively. Since there are two input terminals, the output current or voltage depends on both the input voltages $V_{i1}$ and $V_{i2}$. It is usually more interesting to express the output current or voltage in terms of the differential and common mode input voltages $V_{id}$ and $V_{ic}$ defined as

$$V_{id} \triangleq V_{i1} - V_{i2}$$
$$V_{ic} \triangleq \frac{V_{i1} + V_{i2}}{2}.$$

The differential mode and common mode operations are defined for $V_{ic} = const.$ and for $V_{id} = 0$, respectively. The input terminals are set to an appropriate common mode voltage $V_{ic}$, to which a differential voltage $V_{id}$ is superimposed according to

$$V_{i1} = V_{ic} + \frac{V_{id}}{2}$$
$$V_{i2} = V_{ic} - \frac{V_{id}}{2}.$$

# 2 Small-signal analysis

- Draw the small-signal equivalent schematic of the circuit assuming the transistors are biased in saturation.
- Calculate the small-signal differential voltage gain $A_{vd} \triangleq V_{od}/V_{id}$.
- Calculate the small-signal common-mode input voltage to differential output voltage gain $A_{vc} \triangleq V_{od}/V_{ic}$.

# 3 Noise analysis

- Draw the small-signal equivalent schematic of the circuit assuming the transistors are biased in saturation and including all the noise sources.
- Calculate the output noise power spectral density (PSD) or output noise resistance assuming that the transistors and resistors are perfectly matched.
- Calculate the input-referred thermal noise PSD and the equivalent thermal noise resistance $R_{nin,th}$.
- Calculate the input-referred flicker noise PSD and the equivalent flicker noise resistance $R_{nin,fl}$.
- Calculate the total output thermal noise power assuming that there is an output capacitance $C$ in parallel with each of the load resistance $R_1$ and $R_2$ (assume that transistors, resistors and capacitors are perfectly matched).

# 4 Offset analysis

Mismatch between the two transistors of the differential pair $M_1$-$M_2$ and of the resistors $R_1$-$R_2$ cause some non-zero differential output voltage even for a zero differential input voltage $V_{id} = 0$.

- Calculate the differential mode output mismatch voltage in terms of drain current mismatch $\Delta I_D$ and resistance mismatch $\Delta R$. Hint: use the above noise analysis where the noise currents are replaced by current mismatch.
- Calculate the input-referred offset voltage in terms of resistor mismatch $\Delta R$ and MOS transistor mismatch ($\beta$- and $V_{T0}$-mismatch).
- Determine the variance of the input referred offset voltage. How can it be minimized?

# 5 Common-mode input range analysis (CMIR) and differential-mode output range analysis (DMOR)

- Calculate the minimum and maximum common-mode input voltages $V_{ic,min}$ and $V_{ic,max}$. For this analysis, $V_{id}$ is set to 0 and the ideal current source is replaced by a transistor ($M_2$).
- Calculate the minimum and maximum output voltages $V_{o,min}$ and $V_{o,max}$; deduce the differential output voltage swing $\Delta V_{od,max}$.

# 6 Example

## 6.1 Design

- Design the amplifier, i.e. size the transistors, determine the values of the resistors and the bias current, to meet the specifications given in Table 6.1. For the design we will use a generic 180nm bulk CMOS process. The physical parameters are given in Table 6.2, the global process parameters in Table 6.3 and finally the MOSFET parameters in Table 6.4.

Table 6.1: Specifications for the differential pair with resistive loads.

| Specification | Symbol | Value | Unit |
|---|---|---|---|
| Input common mode voltage | $V_{ic}$ | 0.8 | $V$ |
| DC gain | $A_{dc}$ | 25 | $dB$ |
| DC gain | $A_{dc}$ | 18 | - |
| Bandwidth | $B$ | 1 | $MHz$ |
| Input-referred thermal noise resistance | $R_{nin,th}$ | 10 | $k\Omega$ |
| Maximum input-referred offset voltage | $V_{os}$ | 2 | $mV$ |

Table 6.2: Physical parameters

| Parameter | Value | Unit |
|---|---|---|
| $T$ | 300 | $K$ |
| $U_T$ | 25.875 | $mV$ |

Table 6.3: Global process parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DD}$ | 1.8 | $V$ |
| $C_{ox}$ | 8.443 | $\frac{fF}{\mu m^2}$ |
| $W_{min}$ | 200 | $nm$ |
| $L_{min}$ | 180 | $nm$ |

Table 6.4: Transistor process parameters

| Parameter | NMOS | PMOS | Unit |
|---|---|---|---|
| sEKV parameters | | | |
| $n$ | 1.27 | 1.31 | - |
| $I_{spec\square}$ | 715 | 173 | $nA$ |
| $V_{T0}$ | 0.455 | 0.445 | $V$ |
| $L_{sat}$ | 26 | 36 | $nm$ |
| $\lambda$ | 15 | 20 | $\frac{V}{\mu m}$ |

Table 6.4: Transistor process parameters

| Parameter | NMOS | PMOS | Unit |
|---|---|---|---|
| Overlap capacitances parameters | | | |
| $C_{GDo}$ | 0.366 | 0.329 | $\frac{fF}{\mu m}$ |
| $C_{GSo}$ | 0.366 | 0.329 | $\frac{fF}{\mu m}$ |
| $C_{GBo}$ | 0 | 0 | $\frac{fF}{\mu m}$ |
| Junction capacitances parameters | | | |
| $C_J$ | 1 | 1.121 | $\frac{fF}{\mu m^2}$ |
| $C_{JSW}$ | 0.2 | 0.248 | $\frac{fF}{\mu m}$ |
| Flicker noise parameters | | | |
| $K_F$ | 8.1e-24 | 6.8e-23 | $J$ |
| $AF$ | 1 | 1 | - |
| $\rho$ | 0.05794 | 0.4828 | $\frac{V \cdot m^2}{A \cdot s}$ |
| Matching parameters | | | |
| $A_{VT}$ | 5 | 5 | $mV \cdot \mu m$ |
| $A_\beta$ | 1 | 1 | $\% \cdot \mu m$ |
| Source and drain sheet resistance parameter | | | |
| $R_{sh}$ | 600 | 2386 | $\frac{\Omega}{\mu m}$ |
| Width and length parameters | | | |
| $\Delta W$ | 39 | 54 | $nm$ |
| $\Delta L$ | -76 | -72 | $nm$ |

## 6.2 Simulation

- Simulate your design using the available qucs-s schematic.

## 6.3 Reducing the supply voltage

- What happens if $V_{DD} = 1\,V$? Can you use the same design as before and fulfill all the specifications? Using the same $V_{ic}$, get the new $\Delta V_{od,max}$ and propose an alternative design relaxing one of the specifications.