Fundamentals of Analog VLSI Design
Exercise 5 - Problem

The Cascode Gain Stage

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1 Cascode stage

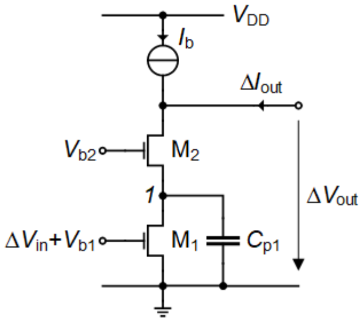

Figure 1.1: Schematic of the cascode gain stage.

Figure 1.1 shows the schematic of the basic cascode gain stage, where both transistors M_1 and M_2 are biased in saturation. The cascode gain stage is used to increase the output resistance (reduce the output conductance) and therefore increase the DC gain without spending more current (current reuse). We will show that this increase of the output resistance and gain is done without significant increase of noise.

We will first carry a small-signal analyze to demonstrate the above features. Then we will show that the noise of the cascode transistor M_2 can actually be neglected at low frequency.

1.1 Analysis

1.1.1 Small-signal analysis

- Draw the equivalent small-signal schematic of the cascode gain stage of Figure 1.1 assuming that the transistors M_1 and M_2 are biased in saturation.
- Calculate the DC equivalent transconductance $G_{meq} \triangleq \Delta I_{out}/\Delta V_{in}|_{\Delta V_{out}=0}$ assuming that $G_{ms2} \gg G_{ds1}, G_{ds2}$.
- Calculate the output conductance $G_{out} = \Delta I_{out}/\Delta V_{out}$ neglecting the parasitic capacitance C_{p1}. How does it compare to the output conductance G_{ds1} of M_1 alone?
- Calculate the output admittance $Y_{out} = \Delta I_{out}/\Delta V_{out}$ including the parasitic capacitance C_{p1}. What is the effect of the parasitic capacitance C_{p1} on the output admittance Y_{out}?

1.1.2 Noise analysis

- Calculate the output noise conductance G_{nout} and input-referred noise resistance R_{nin} neglecting the parasitic capacitance C_{p1}. Separate the input-referred noise resistance in its thermal and 1/f noise contributions $R_{nin}(f) = R_{nt} + R_{nf}(f)$.
- Calculate the cascode noise excess factor $\gamma_{cas} = G_{meq} \cdot R_{nt}$. How does it compare to the noise coming from M_1 only?
- What is the effect of the parasitic capacitance C_{p1} at node 1 on the input-referred noise?

1.2 Design

Design the circuit of Figure 1.1 to achieve the specifications given in Table 1.1 for a generic 180nm bulk CMOS process. Find the minimum current and size the transistor to achieve these specifications. The physical parameters are given in Table 1.2, the global process parameters in Table 1.3 and finally the MOSFET parameters for this 180nm bulk CMOS process are given in Table 1.4.

Table 1.1: Specifications for the cascode gain stage.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	80	dB
Gain-bandwidth product	GBW	10	MHz
Load capacitance	C_L	1	pF

Table 1.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 1.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 1.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	13	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	6.8e-23	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$

Table 1.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

1.3 Simulation

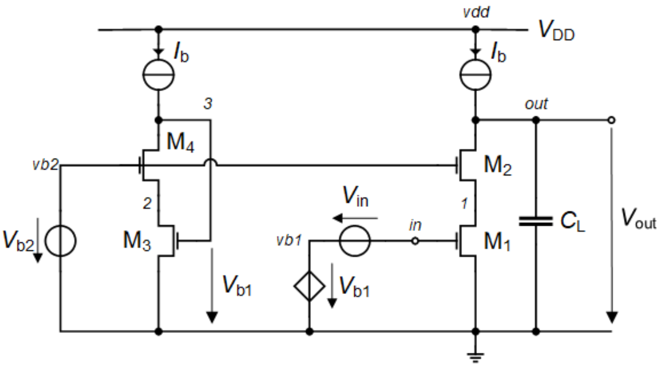

Figure 1.2: Schematic used for the simulation of the transfer function.

You can check your design by simulating the transfer function $A_v = \Delta V_{out}/\Delta V_{in}$ using the schematic shown in Figure 1.2. Note that transistors M_3 and M_4 have been added to correctly set the DC gate voltage of M_1 such that its current is equal to the bias current I_b. Of course M_3 is identical to M_1 and M_4 is identical to M_2.

To save you some time and allow you to run the simulation using ngspice without writing the Jupyter or Quarto notebook, you can use the qucs-s schematic that is provided.

Note

Note that the default design in the qucs-s schematic does not satisfy the specs. You need to update the parameters in the size_bias.par file with those obtained from your design.

Warning

You could also run a noise simulation using the same schematic. However, in qucs-s it is not possible to turn off the noise coming from the bias transistors M_3 and M_4. This means that you will get twice the noise of M_1 and M_2. In the Quarto notebook we read the raw file which gives all the individual noise contributions and from which we can extract only the noise coming from M_1 and M_2.

2 Regulated cascode

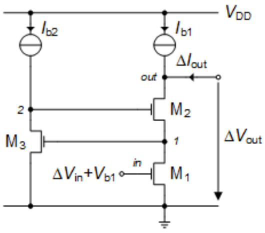

Figure 2.1: Schematic of the regulated cascode.

The schematic of Figure 2.1 corresponds to the regulated cascode, where an additional CS gain stage M_3 is added to maintain the voltage at node 1 constant and therefore to further increase the output resistance and DC gain [1].

2.1 Small-signal analysis

- Draw the small-signal equivalent schematic of the circuit assuming that all the transistors are biased in saturation.
- Calculate the DC equivalent transconductance $G_{meq} \triangleq \Delta I_{out}/\Delta V_{in}|_{\Delta V_{out}=0}$ assuming that all the transconductances are much larger than the output conductances.
- Calculate the output conductance $G_{out} = \Delta I_{out}/\Delta V_{out}$. How does it compare to the output conductance of the cascode of Section 1 ?
- Calculate the voltage gain $A_v \triangleq \Delta V_{out}/\Delta V_{in}$. How does it compare to the cascode of Section 1?

2.2 Noise analysis

- Calculate the output noise conductance G_{nout} and input-referred noise R_{nin}. Separate the input-referred noise resistance in its thermal and 1/f noise contributions $R_{nin}(f) = R_{nt} + R_{nf}(f)$.
- Calculate the cascode noise excess factor $\gamma_{cas} = G_{meq} \cdot R_{nt}$. How does it compare to the noise of the cascode of Section 1?

References

[1] E. Sackinger and W. Guggenbuhl, “A high-swing, high-impedance MOS cascode circuit,” *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 289–298, 1990, doi: 10.1109/4.50316.