Fundamentals of Analog VLSI Design
Exercise 4 - Problem

Basic Common-source Gain Stages

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1 Problem 1

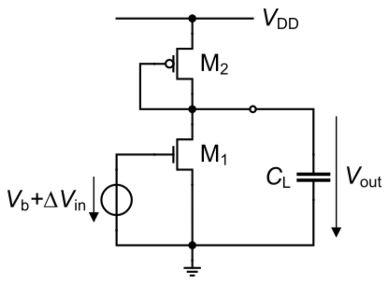

Figure 1.1: Schematic of an elementary gain stage with diode connected load.

Figure 1.1 shows the schematic of a simple common-source (CS) gain-stage with a diode-connected pMOS load. We first will analyze the small-signal operation of this circuit and then will design it for the specifications given in Table 1.1 for a generic 180nm bulk CMOS process. Finally we want to validate the design with circuit simulation.

1.1 Analysis

- Draw the small-signal schematic of the CS gain stage of Figure 1.1 including all the noise sources.
- Derive the small-signal transfer function $A_v(s) \triangleq \Delta V_{out}/\Delta V_{in}$. Give the expressions of the DC gain A_{dc} and cut-off frequency f_c.
- How should M_1 and M_2 be biased to maximize the DC voltage gain?
- What is the maximum achievable voltage gain?
- Calculate the input-referred noise resistance R_{nin} and split it in terms of the input-referred thermal noise resistance R_{nt} and flicker noise resistance R_{nf}.
- Calculate the input-referred thermal noise excess factor $\gamma_{neq} \triangleq G_{m1} \cdot R_{nt}$.
- How should M_1 and M_2 be biased to minimize the input-referred thermal noise excess factor?

1.2 Design

- Design the amplifier for the specifications given in Table 1.1 and for a generic 180nm bulk CMOS process. The physical parameters are given in Table 1.2, the global process parameters in Table 1.3 and finally the MOSFET parameters in Table 1.4.

Table 1.1: Specifications for problem 1.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	-10	-
DC gain in dB	$A_{dc,dB} = 20\,\log(\lvert A_{dc}\rvert)$	20	dB
Cut-off frequency	f_c	1	MHz

Table 1.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 1.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 1.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	6.8e-23	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

Note that the effective channel width and length are defined as follows

$$W_{eff} \triangleq W + \Delta W, \tag{1.1}$$
$$L_{eff} \triangleq L + \Delta L, \tag{1.2}$$

where W and L are drawn width and length.

1.3 Simulation

- Simulate the designed circuit with ngspice or qucs-s.

2 Problem 2

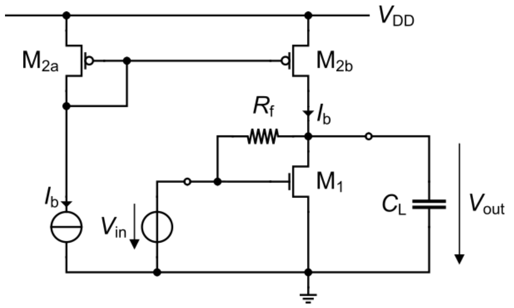

Figure 2.1: Schematic of an elementary gain stage with resistive feedback.

Figure 2.1 shows the schematic of another simple common-source (CS) gain-stage with a feedback resistance R_F. We first will analyze the small-signal operation of this circuit and then will design it for the specifications given in Table 2.1 for a generic 180nm bulk CMOS process. Finally we want to validate the design with circuit simulation.

2.1 Analysis

- Draw the small-signal schematic of the circuit of Figure 2.1 including all the noise sources.
- Derive the small-signal transfer function $A_v(s) \triangleq \Delta V_{out}/\Delta V_{in}$. Give the DC gain A_{dc} and cut-off frequency f_c assuming that $G_{m1} \cdot R_f \gg 1$.
- Calculate the input-referred noise resistance R_{nin} and split it in terms of the input-referred thermal noise resistance R_{nt} and flicker noise resistance R_{nf}.
- Calculate the input-referred thermal noise excess factor $\gamma_{neq} \triangleq G_{m1} \cdot R_{nt}$.
- How should M_1, M_{2a} and M_{2b} be biased to minimize the input-referred thermal noise excess factor?

2.2 Design

- Design the amplifier for the specifications given in Table 2.1 and for the same generic 180nm bulk CMOS process as for Problem 1. The physical parameters are given in Table 1.2, the global process parameters in Table 1.3 and finally the MOSFET parameters in Table 1.4.

Table 2.1: Specifications for problem 2.

Specification	Symbol	Value	Unit
DC gain	A_{dc}	-10	-
DC gain in dB	$A_{dc,dB} = 20\,\log(\lvert A_{dc}\rvert)$	20	dB
Cut-off frequency	f_c	1	MHz

2.3 Simulations

- Simulate the designed circuit with ngspice or qucs-s.