Fundamentals of Analog VLSI Design
Exercise 2 - Problem

Differential pair - Inverter - Velocity saturation

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24.09.2025

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1 Problem 1: The differential pair

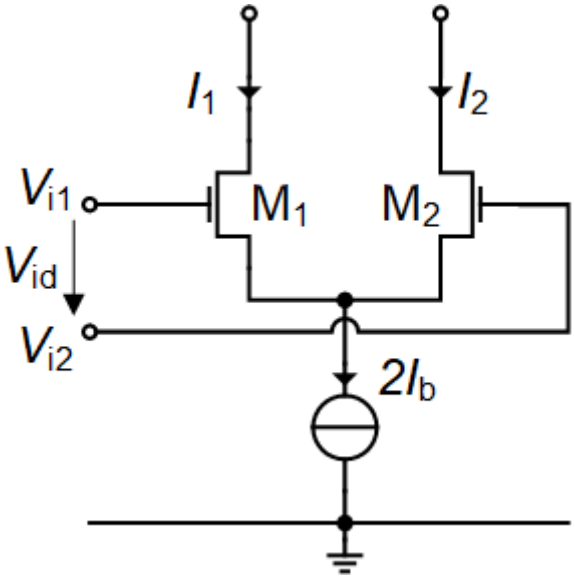

Figure 1.1: Differential pair schematic.

Figure 1.1 shows the schematic of the basic differential pair. The differential input voltage is defined as $V_{id} \triangleq V_{i1} - V_{i2}$, whereas the differential output current is defined as $I_{od} \triangleq I_1 - I_2$.

> **Note**
>
> We assume that M_1 and M_2 are perfectly matched. also assume that M_1 and M_2 are long-channel transistors so we can ignore short-channel effects such as velocity saturation.

1.1 Both transistors in weak inversion

1.1.1 Large-signal characteristic

Derive the large-signal expression of the differential output current I_{od} as a function of the differential input voltage V_{id} assuming that both transistors are biased in weak inversion and saturation.

1.1.2 Small-signal characteristic

Derive the small-signal transconductance from the large-signal transfer function obtained above and its particular value G_{m0} at $V_{id} = 0$. What is the approximate linear range if the differential pair is modeled by a piece-wise linear characteristic having a slope G_{m0} equal to that of the differential pair at $V_{id} = 0$?

1.2 Both transistors in strong inversion

1.2.1 Large-signal characteristic

Derive the large-signal expression of the differential output current I_{od} as a function of the differential input voltage V_{id} assuming that both transistors are biased in strong inversion and saturation.

1.2.2 Small-signal transconductance

Derive the small-signal transconductance from the large-signal transfer function obtained above and its particular value G_{m0} at $V_{id} = 0$. What is the approximate linear range if the differential pair is modeled by a piece-wise linear characteristic having a slope G_{m0} equal to that of the differential pair at $V_{id} = 0$?

1.3 Optional: Both transistors in any modes of operation (saturation)

We can use the EKV charge-based model to derive an expression of the differential input voltage as a function of the differential output current valid in any modes of operation (in saturation). In order to do this, first express the input voltages V_{i1} and V_{i2} normalized to $2nU_T$ as a function of the normalized source charges q_{s1} and q_{s2}. Then find an expression of i_1 and i_2 defined as

$$i_1 \triangleq \frac{I_1}{2I_b} = \frac{i_{d1}}{2IC_q}, \tag{1.1}$$

$$i_2 \triangleq \frac{I_2}{2I_b} = \frac{i_{d2}}{2IC_q}, \tag{1.2}$$

with $i_{d1} \triangleq I_1/I_{spec}$, $i_{d2} \triangleq I_2/I_{spec}$ and $IC_q \triangleq I_b/I_{spec}$ and where I_{spec} is the specific current of M_1 and M_2 and IC_q is the inversion coefficient of M_1 and M_2 at the quiescent point, i.e. for $V_{id} = 0$. You can then invert i_1 and i_2 to obtain expressions of q_{s1} and q_{s2} in terms of $i_{od} \triangleq i_1 - i_2$ and parameter IC_q. Sweeping the normalized output current i_{od} for a given IC_q, you get the corresponding differential input voltage v_{id}.

2 Problem 2: The inverter as a transconductance amplifier

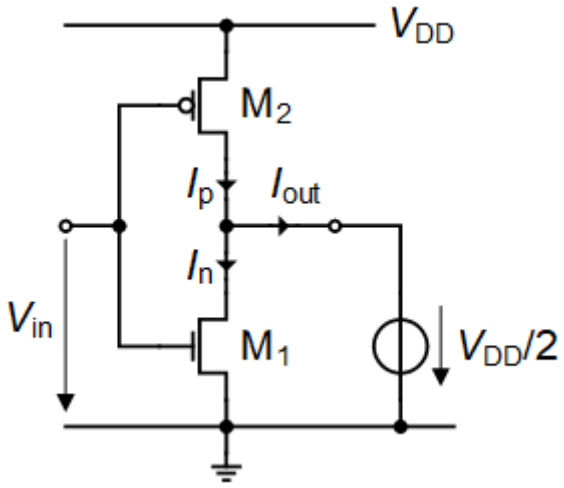

Figure 2.1: The CMOS inverter.

As shown in Figure 2.1, the inverter can be used as a class AB transconductance amplifier. Derive the large-signal output current $I_{out} = I_p - I_n$ versus the input voltage V_{in} assuming that both transistors are biased in weak inversion and saturation and have the same slope factor $n_n = n_p = n$. Note that the output voltage is maintained constant at $V_{DD}/2$ to calculate the output current I_{out}. What is limiting the output current?

3 Problem 3: Effect of velocity saturation on the gate transconductance

In this problem we want to investigate the effect of velocity saturation on the gate transconductance of an nMOS transistor. We will compare the long-channel case to the short-channel first in strong inversion and then in weak inversion.

3.1 Strong inversion

For strong inversion we assume a bias current $I_b = 20\,\mu A$ and an inversion coefficient $IC = 30$ to drive a large load capacitance $C_L = 5\,pF$. Calculate its gate transconductance G_m and bandwidth assuming its slope factor is $n = 1.3$ and $U_T = 26\,mV$ in the following cases.

3.1.1 Long-channel case

Assume the channel is long enough to ignore the effect of velocity saturation.

3.1.2 Short-channel case

Assume the transistor length is short resulting in a velocity saturation parameter $\lambda_c = 1/3$. How much smaller is the gate transconductance and bandwidth with velocity saturation compared to the long-channel case?

3.2 Weak inversion

In the case of weak inversion we assume an inversion coefficient $IC = 0.1$, a bias current $I_b = 100\,nA$ and a load capacitance $C_L = 0.1\,pF$.

3.2.1 Long-channel case

Assume again that the channel is long enough to ignore the effect of velocity saturation.

3.2.2 Short-channel case

Assume the transistor length is short resulting in a velocity saturation parameter $\lambda_c = 1/3$. How much smaller is the gate transconductance and bandwidth with velocity saturation compared to the long-channel case?

What can we conclude from this simple example?