# Fundamentals of Analog VLSI Design
# Exercise 11 - Solution

**Linearized Transconductor**

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# 1 Problem 1: MOS in linear Region

## 1.1 Introduction

Very linear transconductors can be built using the MOS transistor biased in the linear region. Indeed, the drain current $I_D$ of a long-channel MOS transistor biased in strong inversion and in the linear region assuming $V_S = 0$ is given by

$$I_D = n\,\beta \left(V_P - \frac{V_D}{2}\right) V_D = \beta \left(V_G - V_{T0} - \frac{n}{2}\,V_D\right) V_D \quad \text{for } V_D < V_P = \frac{V_G - V_{T0}}{n}, \tag{1.1}$$

where we have neglected the effect of mobility reduction due to the vertical field. The forward current $I_F$, reverse current $I_R$ and drain current $I_D = I_F - I_R$ are sketched in Figure 1.1. For $V_G > V_{T0} + n\,V_D$, the drain current depends linearly on $V_G$. The range of the input voltage $V_{in} = V_G$ in which the transconductor behaves linearly can be defined as $V_{Gmin} < V_{in} < V_{Gmax}$ where $V_{Gmin} = V_{T0} + n\,V_D$ and $V_{Gmax}$ depends on the deviation from the linear behavior due to mobility reduction due to the vertical field.

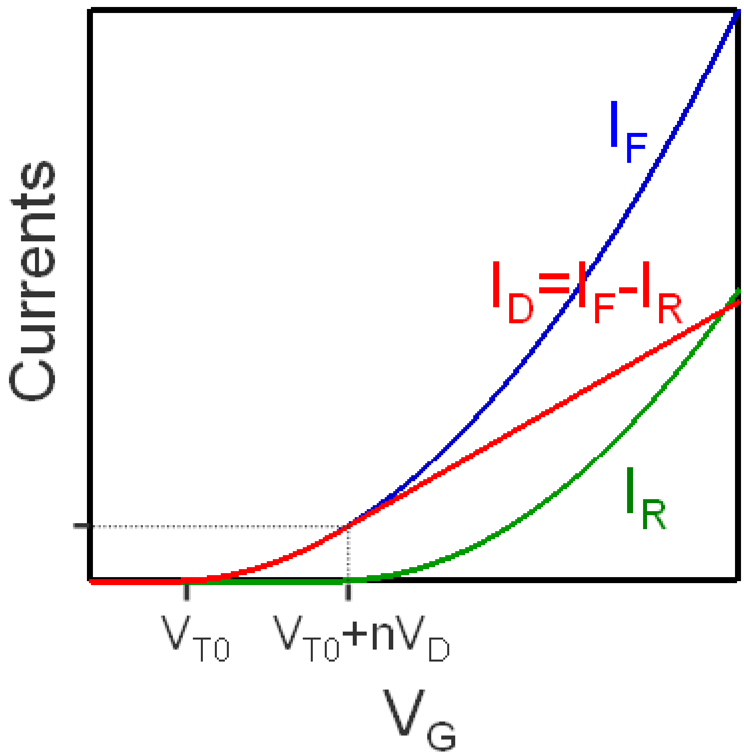


Figure 1.1: Forward, reverse and drain current of a transistor biased in strong inversion and in the linear region.

To bias transistor $M_1$ in the linear region, we can use the circuit of Figure 1.2, which is similar to a cascode stage except that in this case the transistor $M_1$ is biased in the linear region and in strong inversion. For a given gate bias voltage $V_G$, the bias voltage $V_b$ applied at the gate of $M_2$ is set such that the drain voltage of $M_1$ is smaller than its saturation voltage $V_D < V_P \cong (V_G - V_{T0})/n$. Now, the

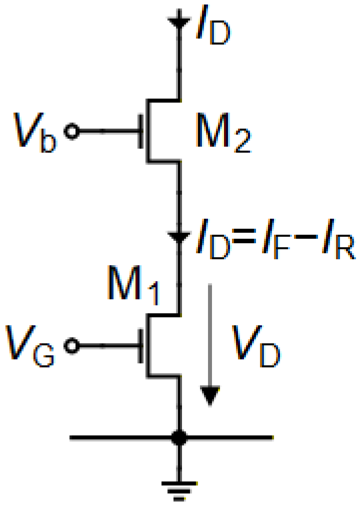


Figure 1.2: MOS transistor biased in the linear region

impedance at the drain node of $M_1$ is not zero and has an effect of the equivalent transconductance. We will study this in Problem 1.

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- From Figure 1.1, estimate the input linear range assuming that it is limited by the supply voltage on the positive side.

From Figure 1.1, we can easily deduce that the maximum input amplitude as

$$V_{in,max} = \frac{V_{DD} - V_{T0} - n_1 V_{D1}}{2}. \tag{1.2}$$

The linear input range is maximized by minimizing $V_{D1}$. On the other hand, as discussed below, the maximum equivalent transconductance is

$$G_{meq,max} = \beta_1 \cdot V_{D1}. \tag{1.3}$$

We can therefore observe that there is a trade-off between linear range and transconductance (or gain-bandwidth product for a given load capacitance).

Note that the corresponding maximum gate bias voltage is then simply

$$V_{G1,max} = \frac{V_{DD} + V_{T0} + n_1 V_{D1}}{2}. \tag{1.4}$$

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- Derive the small-signal transconductance of the circuit shown in Figure 1.2. Assume that the output voltage is grounded and that $M_1$ is biased in the linear region and $M_2$ in the saturation region.

The small-signal equivalent circuit of the circuit of Figure 1.2 is shown in Figure 1.3. Notice the drain transconductance $G_{md1}$ due to the fact that $M_1$ is biased in the linear region. We have also assumed that $G_{ds1} \ll G_{md1}$. To derive the equivalent transconductance we assume that the small-signal output voltage is grounded. This results in

$$G_{meq} = \frac{\Delta I_{out}}{\Delta V_{in}} = \frac{G_{m1}\,(G_{ms2} + G_{ds2})}{G_{ms2} + G_{md1} + G_{ds1} + G_{ds2}} \cong \frac{G_{m1}\,G_{ms2}}{G_{ms2} + G_{md1}} = G_{m1}\,\frac{G_{ms2}/G_{md1}}{G_{ms2}/G_{md1} + 1}, \tag{1.5}$$

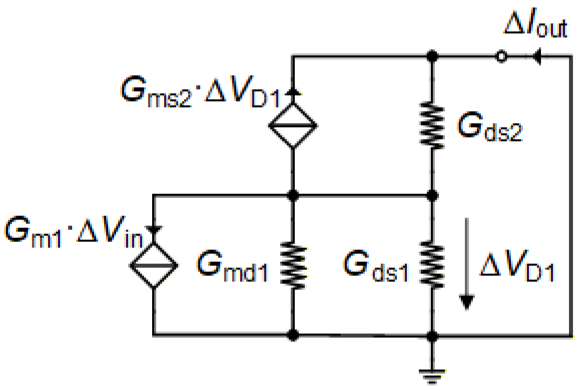


Figure 1.3: Small-signal schematic of the circuit of Figure 1.2

where we have assumed that $G_{ds1}, G_{ds2} \ll G_{ms2}$. If additionally we assume that $G_{ms2} \gg G_{md1}$, then $G_{meq} \cong G_{m1}$. However, the assumption $G_{ms2} \gg G_{md1}$ is not always valid. We will investigate this below.

The transconductances $G_{m1}$ and $G_{md1}$ are given by

$$G_{m1} = \frac{G_{ms1} - G_{md1}}{n_1} = \frac{G_{spec1}}{n_1}\,(q_{s1} - q_{d1}), \tag{1.6}$$

$$G_{ms1} = G_{spec1}\, q_{s1}, \tag{1.7}$$

$$G_{md1} = G_{spec1}\, q_{d1}. \tag{1.8}$$

Note that the above equations are valid in all regions of operation. If we assume that $M_1$ is biased in strong inversion and in the linear region $q_s$ and $q_d$ are related to the voltages according to with

$$q_{s1} = \frac{V_{P1}}{2\,U_T} = \frac{v_{p1}}{2}, \tag{1.9}$$

$$q_{d1} = \frac{V_{P1} - V_{D1}}{2\,U_T} = \frac{v_{p1} - v_{d1}}{2}, \tag{1.10}$$

where $v_{p1} \triangleq V_{P1}/U_T$ and $v_{d1} \triangleq V_{D1}/U_T$ are the normalized pinch-off and drain voltages of $M_1$. The transconductance $G_{m1}$ then writes

$$G_{m1} = \frac{G_{spec1}}{n_1}\,\frac{V_{D1}}{2\,U_T} = \beta_1\, V_{D1}. \tag{1.11}$$

If we further assume that $M_2$ is bias biased in weak inversion to maximize $G_{ms2}$ for the given current $I_D$, then

$$G_{ms2} = \frac{I_D}{U_T}. \tag{1.12}$$

The drain current $I_D$ can be written as

$$I_D = I_{spec1}\,[q_{s1}\,(q_{s1} + 1) - q_{d1}\,(q_{d1} + 1)]. \tag{1.13}$$

If we assume that $M_1$ is biased in strong inversion (i.e. $q_{s1} \gg 1$ and $q_{d1} \gg 1$) then the current simplifies to

$$I_D = I_{spec1}\,(q_{s1}^2 - q_{d1}^2) = I_{spec1}\,(q_{s1} - q_{d1})(q_{s1} + q_{d1}), \tag{1.14}$$

We can then write

$$q_{s1} - q_{d1} = \frac{V_{D1}}{2\,U_T} = \frac{v_{d1}}{2}, \tag{1.15}$$

$$q_{s1} + q_{d1} = \frac{2\,V_{P1} - V_{D1}}{2\,U_T} = \frac{2\,v_{p1} - v_{d1}}{2}. \tag{1.16}$$

Replacing in the expression of the drain current we get

$$I_D = I_{spec1} \frac{(2\,V_{P1} - V_{D1})\,V_{D1}}{(2\,U_T)^2} = n_1\,\beta_1 \left(V_{P1} - \frac{n_1}{2}\,V_{D1}\right) V_{D1}, \tag{1.17}$$

which is identical to (1.1).

Transconductance $G_{ms2}$ can therefore be written as

$$G_{ms2} = G_{spec1}\,(q_{s1}^2 - q_{d1}^2) \tag{1.18}$$

and $G_{ms2}/G_{md1}$ as

$$\frac{G_{ms2}}{G_{md1}} = \frac{q_{s1}^2 - q_{d1}^2}{q_{d1}} = q_{d1}\left[\left(\frac{q_{s1}}{q_{d1}}\right)^2 - 1\right]. \tag{1.19}$$

The $q_{s1}/q_{d1}$ ratio can be written in terms of voltages as

$$\frac{q_{s1}}{q_{d1}} = \frac{V_{P1}}{V_{P1} - V_{D1}} = \frac{v_{p1}}{v_{p1} - v_{d1}}. \tag{1.20}$$

The $G_{ms2}/G_{md1}$ ratio is plotted in Figure 1.4 versus $v_{p1}$ sweeping also $v_{d1}$ maintaining a constant $v_{d1}/v_{p1} = \alpha$ ratio.

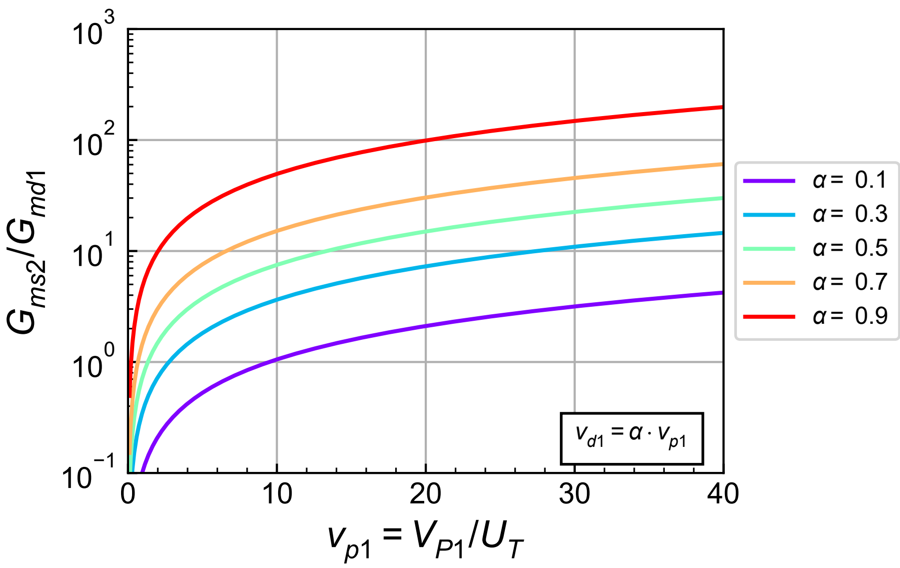


Figure 1.4: $G_{ms2}/G_{md1}$ ratio versus $v_{p1}$.

From Figure 1.4 we see that when $v_{d1}$ is small compared to $v_{p1}$ (i.e. small $\alpha$), $G_{ms2}$ can no more be considered much larger than $G_{md1}$, particularly at low $v_{p1}$.

We can evaluate the effect of the cascode transistor on the equivalent transconductance by looking at the $G_{meq}/G_{m1}$ given by

$$\frac{G_{meq}}{G_{m1}} = \frac{G_{ms2}/G_{md1}}{G_{ms2}/G_{md1} + 1}, \tag{1.21}$$

which depends only on the $V_{P1}$ and $V_{D1}$ voltages. The $G_{meq}/G_{m1}$ ratio is plotted in Figure 1.5 versus $v_{p1}$ sweeping also $v_{d1}$ maintaining a constant $v_{d1}/v_{p1} = \alpha$ ratio.

From Figure 1.5, we see that the finite conductance at the drain node of $M_1$ due to $G_{md1}$ and $G_{ms2}$ slightly reduces the equivalent transconductance $G_{meq}$ compared to $G_{m1}$ particularly at low $\alpha = v_{d1}/v_{p1}$.

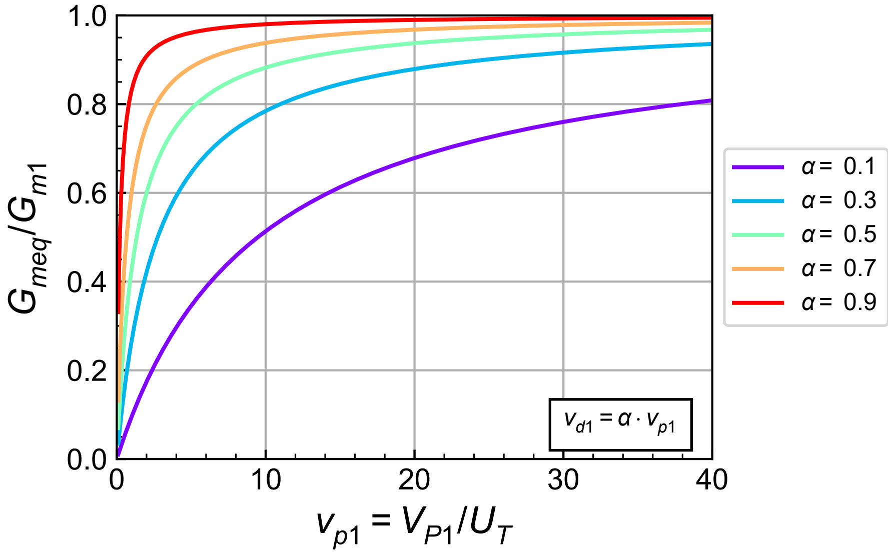


Figure 1.5: $G_{meq}/G_{m1}$ ratio versus $V_{P1}$.

Finally, we can plot the $G_{meq}/G_{spec1}$ ratio given by

$$\frac{G_{meq}}{G_{spec1}} = \frac{G_{m1}}{G_{spec1}} \frac{G_{ms2}/G_{md1}}{G_{ms2}/G_{md1} + 1}, \tag{1.22}$$

where

$$\frac{G_{m1}}{G_{spec1}} = \frac{V_{D1}}{2n_1 U_T} = \frac{v_{d1}}{2n_1}. \tag{1.23}$$

The $G_{meq}/G_{spec1}$ ratio is plotted in Figure 1.6 versus $v_{d1}$ sweeping also $v_{p1}$ maintaining a constant $v_{p1}/v_{d1} = 1/\alpha$ ratio.

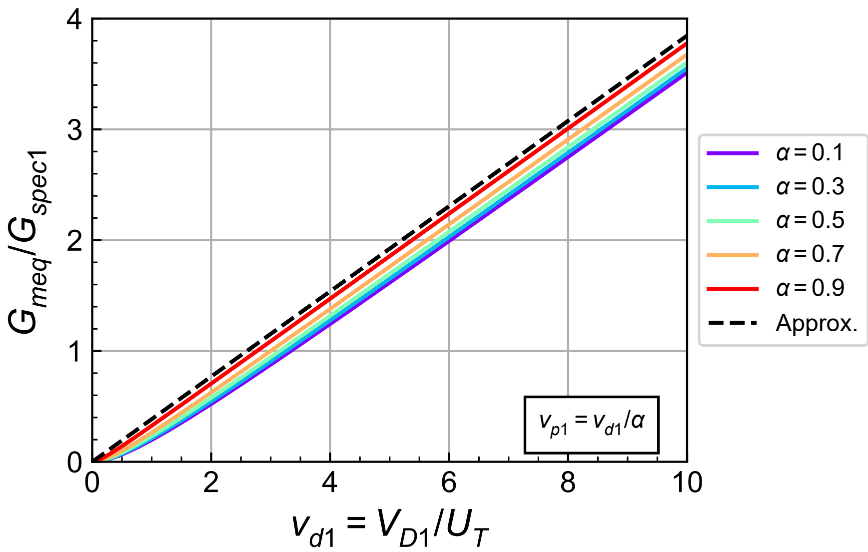


Figure 1.6: $G_{meq}/G_{spec1}$ ratio versus $v_{d1}$.

From Figure 1.6, we see that the effect of $G_{ms2}$ and $G_{md1}$ on $G_{meq}$ remain small so that the approximation

$$G_{meq} \cong \beta_1 \cdot V_{D1} \tag{1.24}$$

can be used.

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- Calculate the input-referred noise of the circuit of Figure 1.2.

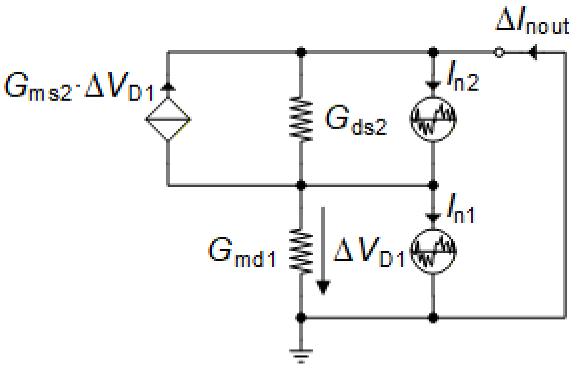


Figure 1.7: Small-signal circuit of Figure 1.2 for noise calaculation.

The small-signal circuit of Figure 1.2 for the noise calculation is shown in Figure 1.7. The output noise conductance is given by

$$G_{nout} = \left(\frac{G_{ms2}}{G_{md1} + G_{ms2}}\right)^2 \cdot G_{n1} + \left(\frac{G_{md1}}{G_{md1} + G_{ms2}}\right)^2 \cdot G_{n2}. \tag{1.25}$$

The input-referred noise resistance is then given by

$$R_{nin} \triangleq \frac{G_{nout}}{G_{meq}^2} = \frac{G_{n1}}{G_{m1}^2} + \left(\frac{G_{md1}}{G_{m1}\,G_{ms2}}\right) G_{n2}. \tag{1.26}$$

We can rewrite $R_{nin}$ as

$$R_{nin} = \frac{G_{n1}}{G_{m1}^2}\,(1+\eta) \tag{1.27}$$

with

$$\eta = \left(\frac{G_{md1}}{G_{ms2}}\right)^2 \frac{G_{n2}}{G_{n1}}. \tag{1.28}$$

For thermal noise, we have to remember that the thermal noise excess factor $\gamma_n$ is mostly used for transistors biased in saturation. It is defined as

$$\gamma_n = \frac{G_n}{G_m} = \frac{g_n}{g_m}, \tag{1.29}$$

where

$$g_n \triangleq \frac{G_n}{G_{spec}} = \frac{1}{6}\,\frac{4q_s^2 + 3q_s + 4q_s q_d + 3q_d + 4q_d^2}{q_s + q_d + 1} \tag{1.30}$$

and

$$g_m \triangleq \frac{G_m}{G_{spec}} = \frac{q_s - q_d}{n}. \tag{1.31}$$

We see that $\gamma_n \to \infty$ for $q_d \to q_s$ (or $v_d \to v_s$).

We also have introduced the thermal noise parameter $\delta_n$ defined as

$$\delta_n \triangleq \frac{G_n}{G_{ms}} = \frac{g_n}{g_{ms}} = \frac{g_n}{q_s}, \tag{1.32}$$

which tends to 1 as $q_d \to q_s$ (or $v_d \to v_s$).

$\gamma_n$ is related to $\delta_n$ accoding to

$$\gamma_n = \frac{g_n}{q_s}\,\frac{q_s}{g_m} = \frac{n\,\delta_n}{1 - q_d/q_s}, \tag{1.33}$$

which in saturation (i.e. for $q_d = 0$) reduces to

$$\gamma_{n,sat} = n\,\delta_{n,sat}, \tag{1.34}$$

with

$$\delta_{n,sat} = \delta_n(q_d = 0) = \frac{2}{3}\,\frac{q_s + 3/4}{q_s + 1} = \begin{cases} \frac{1}{2} & \text{WI and sat. } (q_s \ll 1) \\ \frac{2}{3} & \text{SI and sat. } (q_s \gg 1). \end{cases} \tag{1.35}$$

$\delta_n$ and $\gamma_n$ in strong inversion ($v_p = 40$) are plotted versus $v_d$ in Figure 1.8.

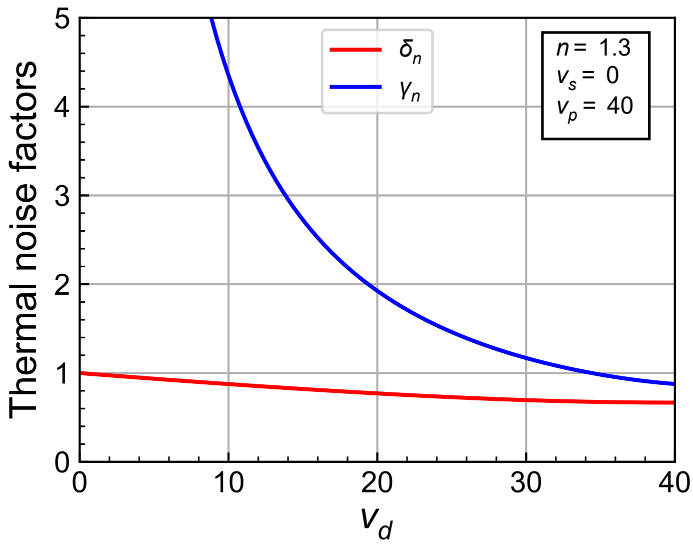


Figure 1.8: Noise parameters $\delta_n$ and $\gamma_n$ versus $v_d$ in strong inversion.

We see that $\gamma_n$ increases significantly as $v_d$ decreases and tends to infinity when $v_d$ tends to 0. This is simply due to the fact that when $v_d$ tends to $v_s$, $G_m$ tends to 0.

The equivalent thermal noise excess factor of the transconductor of Figure 1.2 is given by

$$\gamma_{neq} = G_{m1}\,R_{nin} = \frac{G_{n1}}{G_{m1}}\,(1 + \eta_{th}) = \gamma_{n1}\,(1 + \eta_{th}), \tag{1.36}$$

where

$$\gamma_{n1} = \frac{g_{n1}}{g_{m1}}. \tag{1.37}$$

For $M_1$ biased in strong inversion (i.e. $q_{s1} \gg 1$ and $q_{d1} \gg 1$), $g_{n1}$ simplifies to

$$g_{n1} \cong \frac{2}{3}\,\frac{q_{s1}^2 + q_{s1}q_{d1} + q_{d1}^2}{q_{s1} + q_{d1}} = q_{s1} \cdot \frac{1 + q_{d1}/q_{s1} + (q_{d1}/q_{s1})^2}{1 + q_{d1}/q_{s1}} \tag{1.38}$$

and $g_{m1}$ to

$$g_{m1} = \frac{q_{s1} - q_{d1}}{n_1} = \frac{q_{s1}}{n_1}\left(1 - \frac{q_{d1}}{q_{s1}}\right) \tag{1.39}$$

with

$$\frac{q_{d1}}{q_{s1}} = 1 - \frac{v_{d1}}{v_{p1}}. \tag{1.40}$$

We can then write

$$\gamma_{n1} = n_1\,\frac{1 + q_{d1}/q_{s1} + (q_{d1}/q_{s1})^2}{1 - (q_{d1}/q_{s1})^2}. \tag{1.41}$$

The $\eta_{th}$ parameter which represents the contribution of $M_2$ to the input-referred thermal noise resistance relative to that of $M_1$ is given by

$$\eta_{th} = \left(\frac{G_{md1}}{G_{ms2}}\right)^2\,\frac{\delta_{n2}\,G_{ms2}}{\delta_{n1}\,G_{ms1}} = \frac{\delta_{n2}}{\delta_{n1}}\,\frac{G_{md1}}{G_{ms2}}\,\frac{G_{md1}}{G_{ms1}}. \tag{1.42}$$

The thermal noise parameter $\delta_{n1}$ is defined as

$$\delta_{n1} \triangleq \frac{g_{n1}}{g_{ms1}} = \frac{g_{n1}}{q_{s1}}. \tag{1.43}$$

For $M_1$ biased in strong inversion (i.e. $q_{s1} \gg 1$ and $q_{d1} \gg 1$), $g_{n1}$ simplifies to

$$g_{n1} \cong \frac{2}{3} \frac{q_{s1}^2 + q_{s1}q_{d1} + q_{d1}^2}{q_{s1} + q_{d1}} = q_{s1} \cdot \frac{1 + q_{d1}/q_{s1} + (q_{d1}/q_{s1})^2}{1 + q_{d1}/q_{s1}} \tag{1.44}$$

and

$$\delta_{n1} = \frac{1 + q_{d1}/q_{s1} + (q_{d1}/q_{s1})^2}{1 + q_{d1}/q_{s1}} \tag{1.45}$$

with

$$\frac{q_{d1}}{q_{s1}} = 1 - \frac{v_{d1}}{v_{p1}}. \tag{1.46}$$

Since we have assumed that $M_2$ is biased in weak inversion and saturation, $\delta_{n2} = 1/2$ so that

$$\frac{\delta_{n2}}{\delta_{n1}} = \frac{1}{2} \frac{1 + q_{d1}/q_{s1}}{1 + q_{d1}/q_{s1} + (q_{d1}/q_{s1})^2}. \tag{1.47}$$

The $G_{md1}/G_{ms2}$ ratio in strong inversion is given

$$\frac{G_{md1}}{G_{ms2}} = \frac{q_{d1}}{q_{s1}^2 - q_{d1}^2} = \frac{1}{q_{s1}} \frac{q_{d1}/q_{s1}}{1 - (q_{d1}/q_{s1})^2} \tag{1.48}$$

The $G_{md1}/G_{ms1}$ ratio in strong inversion is given

$$\frac{G_{md1}}{G_{ms1}} = \frac{q_{d1}}{q_{s1}} = 1 - \frac{v_{d1}}{v_{p1}} \tag{1.49}$$

Parameter $\eta_{th}$ is plotted versus $v_{d1}$ in Figure 1.9 together with the different factors in (1.42)

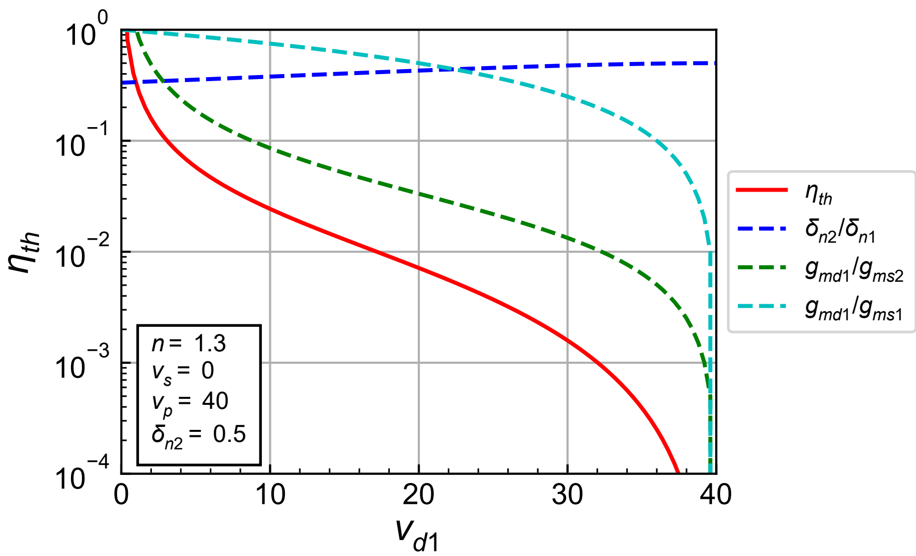


Figure 1.9: $\eta_{th}$ versus $v_d$ in strong inversion.

From Figure 1.9, we see that for $V_{D1}$ larger than a few $U_T$, $\eta_{th}$ is totally negligible and the thermal noise excess factor can simply be approximated by $\gamma_{n1}$, which is plotted versus $v_{d1}$ for $v_{p1} = 40$ in Figure 1.10.

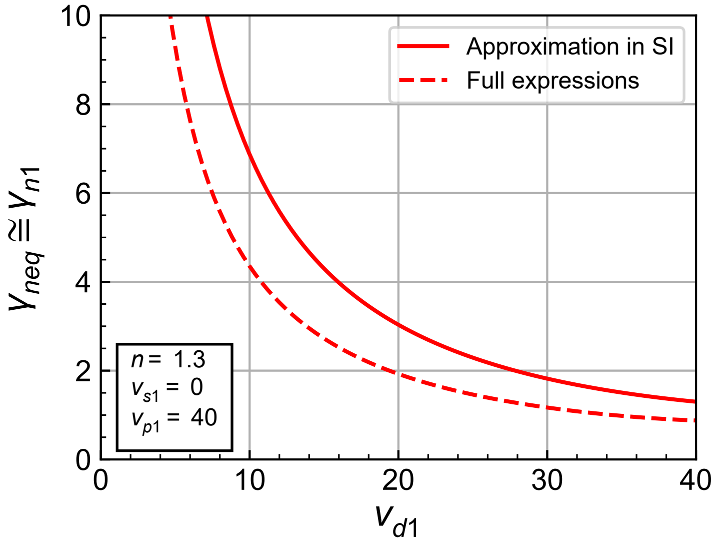


Figure 1.10: Thermal noise excess factor $\gamma_{n1}$ versus $v_{d1}$.

Figure 1.10 shows that the thermal noise excess factor of the linearized transconductor of Figure 1.2 degrades as $v_{d1}$ decreases. This clearly illustrates the trade-off between linear range, demanding for a small $V_{D1}$ and thermal noise, demanding for $V_{D1}$ close to $V_{P1}$.

The expression of $\gamma_{n1}$ valid in strong inversion is compared to that obtained with the full expressions of $g_{n1}$ and $g_{m1}$. We see that the strong inversion simplification slightly overestimates the actual value obtained from the full expressions.

# 2 Problem 2: Low-voltage Linearized Transconductor

## 2.1 Introduction

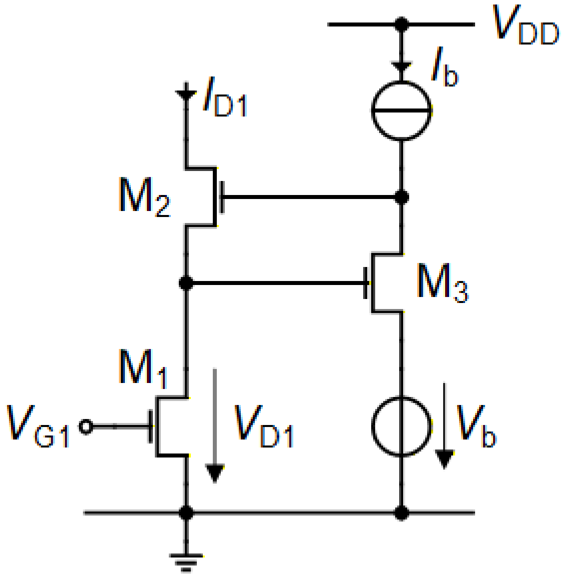


Figure 2.1: Linearized transconductor with regulated cascode.

Similarly to the cascode stage, we can reduce the impedance seen by the driver transistor $M_1$ at its drain by using a regulated cascode as shown in Figure 2.1. However, to bias $M_1$ in the linear region requires a negative bias voltage $V_b$.

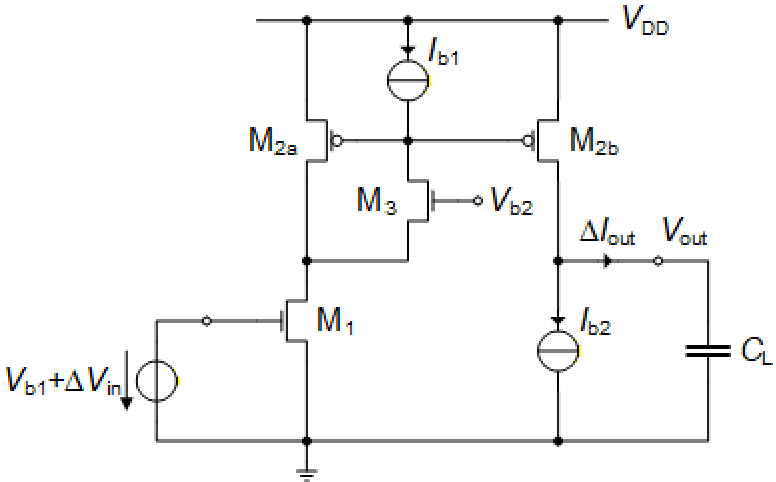


Figure 2.2: Low-voltage linearized transconductor [1].

This problem can be circumvented by using the low-voltage linearized transconductor shown in Figure 2.2 [1]. It is made of a driver transistor $M_1$ biased in the linear region by means of transistor

$M_3$ and the bias voltage $V_{b2}$. Transistors $M_{2a}$ and $M_{2b}$ form a current mirror (they have the same gate voltage), mirroring the current variation from $M_1$ to the output. The role of transistor $M_3$ is to maintain the $V_{DS1}$ voltage as constant as possible to avoid any distortion. This is obtained by the feedback loop introduced by $M_3$ and $M_{2a}$.

## 2.2 Small-signal analysis

- Draw the small-signal schematic of the circuit given in Figure 2.2, assuming that all the transistors are biased in saturation except for $M_1$ which is biased in the linear region.

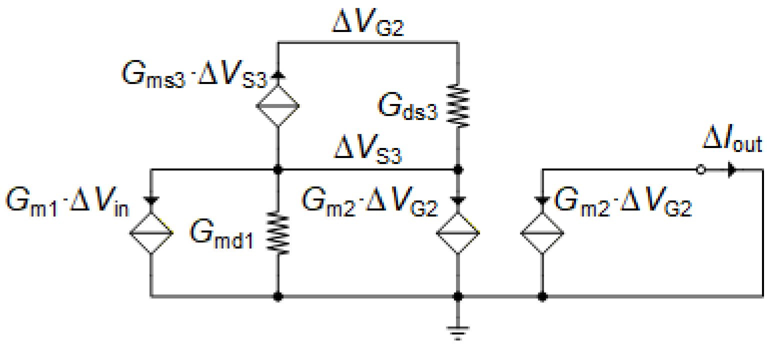


Figure 2.3: Small-signal schematic of Figure 2.2 for the derivation of the equivalent transconductance.

The small-signal of the low-voltage linearized transconductor of Figure 2.2 is shown in Figure 2.3 including the drain transconductance $G_{md1}$ of $M_1$.

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- Derive the expression of the equivalent small-signal transconductance $G_{meq} = \Delta I_{out}/\Delta V_{in}$ for $\Delta V_{out} = 0$ where $\Delta V_{in}$ is the small-signal input voltage. Consider only the output conductance $G_{ds}$ of $M_3$ and that $M_{2a}$-$M_{2b}$ are perfectly matched and.

The equivalent transconductance $G_{meq}$ can be derived from the schematic shown in Figure 2.3 resulting in

$$G_{meq} \triangleq \frac{\Delta I_{out}}{\Delta V_{in}} = G_{m1} \frac{G_{m2}\,(G_{ms3} + G_{ds3})}{G_{m2}\,G_{ms3} + G_{m2}\,G_{ds3} + G_{md1}\,G_{ds3}}, \tag{2.1}$$

which for $G_{ds3} \ll G_{ms3}$, $G_{meq}$ reduces to

$$G_{meq} \cong G_{m1} \frac{G_{m2}\,G_{ms3}}{G_{m2}\,G_{ms3} + G_{md1}\,G_{ds3}} = \frac{G_{m1}}{1 + \frac{G_{md1}\,G_{ds3}}{G_{m2}\,G_{ms3}}}. \tag{2.2}$$

We see that even if $G_{md1}$ is of the same order of magintude than $G_{m2}$, since $G_{ms3} \gg G_{ds3}$, $G_{meq}$ reduces to

$$G_{meq} \cong G_{m1}. \tag{2.3}$$

## 2.3 Noise analysis

- Draw the small-signal circuit inclduding all the noise sources.

The small-signal schematic including all the noise sources is shown in Figure 2.4.

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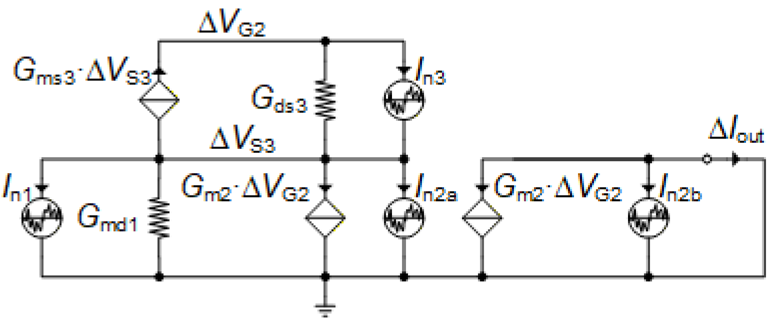


Figure 2.4: Small-signal schematic of Figure 2.2 for the noise calculation.

- Derive an expression of the output noise conductance $G_{nout}$ assuming that $G_{ms3} \gg G_{ds3}$.

The output noise conductance can be calculated with the help of Figure 2.4. Assuming that $G_{ms3} \gg G_{ds3}$ results in

$$G_{nout} = G_{n1} + 2\,G_{n2} + \left(\frac{G_{md1}}{G_{ms3}}\right)^2 G_{n3}. \tag{2.4}$$

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- Calculate the input-referred noise resistance $R_{nin}$, the input-referred thermal noise resistance $R_{nt}$ and the equivalent thermal noise excess factor $\gamma_{neq} \triangleq G_{meq} \cdot R_{nt}$.

The input-referred noise resistance is given by

$$R_{nin} \triangleq \frac{G_{nout}}{G_{meq}^2} \cong \frac{G_{n1}}{G_{m1}^2} + \frac{2\,G_{n2}}{G_{m1}^2} + \left(\frac{G_{md1}}{G_{m1}\,G_{ms3}}\right)^2 G_{n3}. \tag{2.5}$$

which can be written as

$$R_{nin} = \frac{G_{n1}}{G_{m1}^2}\,(1+\eta) \tag{2.6}$$

with

$$\eta = 2\,\frac{G_{n2}}{G_{n1}} + \left(\frac{G_{md1}}{G_{ms3}}\right)^2 \frac{G_{n3}}{G_{n1}}. \tag{2.7}$$

The equivalent thermal noise excess factor $\gamma_{neq}$ is then given by

$$\gamma_{neq} \triangleq G_{meq} \cdot R_{nt} = \frac{G_{n1}}{G_{m1}}\,(1+\eta_{th}) = \gamma_{n1}\,(1+\eta_{th}). \tag{2.8}$$

Assuming $M_1$ is biased in strong inversion (i.e. $q_{s1} \gg 1$ and $q_{d1} \gg 1$), we can reuse the results of Problem 1, leading to

$$\gamma_{n1} = n_1\,\frac{1 + q_{d1}/q_{s1} + (q_{d1}/q_{s1})^2}{1-(q_{d1}/q_{s1})^2}. \tag{2.9}$$

with

$$\frac{q_{d1}}{q_{s1}} = 1 - \frac{v_{d1}}{v_{p1}}. \tag{2.10}$$

For thermal noise $G_{n2}$ and $G_{n3}$ are given by

$$G_{n1} = \delta_{n1}\,G_{ms1}, \tag{2.11}$$
$$G_{n2} = \gamma_{n2}\,G_{m2}, \tag{2.12}$$
$$G_{n3} = \delta_{n3}\,G_{ms3}. \tag{2.13}$$

The $\eta_{th}$ factor can then be written as

$$\eta_{th} = 2\frac{\gamma_{n2}}{\delta_{n1}}\frac{G_{m2}}{G_{ms1}} + \frac{\delta_{n3}}{\delta_{n1}}\frac{G_{md1}}{G_{ms1}}\frac{G_{md1}}{G_{ms3}}. \tag{2.14}$$

Similarly to Problem 1, the last term in (2.14) can be neglected. Assuming that $M_{2a}$-$M_{2b}$ are biased in strong inversion, we have

$$G_{m2} = \beta_2 V_{P2}, \tag{2.15}$$
$$G_{ms1} = \beta_1 V_{P1}. \tag{2.16}$$

Assuming we can choose $\beta_1 \gg \beta_2$ and $V_{P1} \gg V_{P2}$, we can then neglect also the first term in $\eta_{th}$ so that

$$\gamma_{neq} \cong \gamma_{n1}. \tag{2.17}$$

The thermal noise excess factor is therefore also quite large (in the order of 5 to 6) and follows the same trade-off in terms of linear range and thermal noise excess factor.

[1] U. Yodprasit and C. C. Enz, “A 1.5-v 75-dB dynamic range third-order $G_m$-$C$ filter integrated in a 0.18-$\mu$m standard digital CMOS process,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1189–1197, 2003, doi: 10.1109/JSSC.2003.813293.