Fundamentals of Analog VLSI Design
Exercise 11 - Problem

Linearized Transconductor

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1 Problem 1: MOS in the linear region

1.1 Introduction

Very linear transconductors can be built using the MOS transistor biased in the linear region. Indeed, the drain current I_D of a long-channel MOS transistor biased in strong inversion and in the linear region assuming $V_S = 0$ is given by

$$I_D = n\,\beta\left(V_P - \frac{V_D}{2}\right)V_D = \beta\left(V_G - V_{T0} - \frac{n}{2}\,V_D\right)V_D \quad \text{for } V_D < V_P = \frac{V_G - V_{T0}}{n}, \tag{1.1}$$

where we have neglected the effect of mobility reduction due to the vertical field. The forward current I_F, reverse current I_R and drain current $I_D = I_F - I_R$ are sketched in Figure 1.1. For $V_G > V_{T0} + n\,V_D$, the drain current depends linearly on V_G. The range of the input voltage $V_{in} = V_G$ in which the transconductor behaves linearly can be defined as $V_{Gmin} < V_{in} < V_{Gmax}$ where $V_{Gmin} = V_{T0} + n\,V_D$ and V_{Gmax} depends on the deviation from the linear behavior due to mobility reduction due to the vertical field.

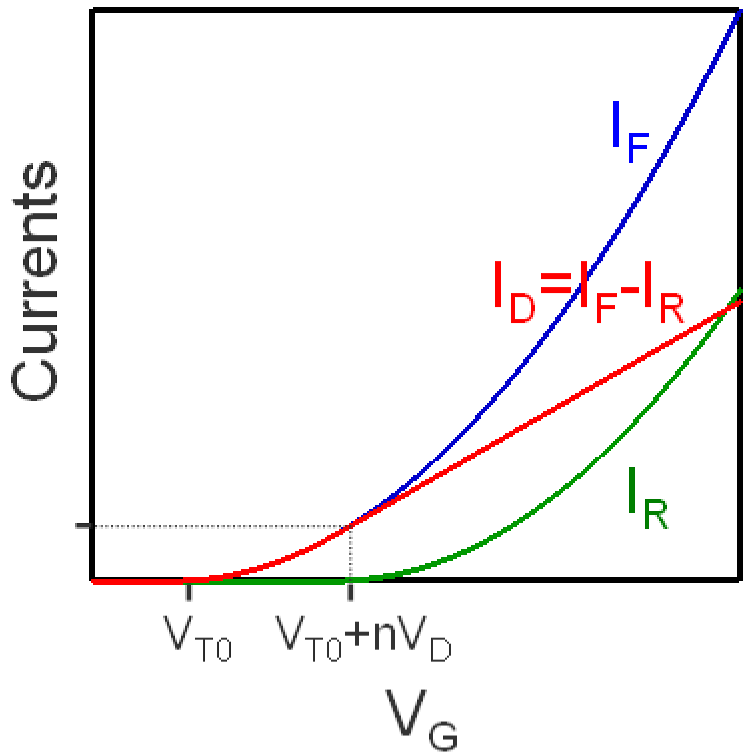

Figure 1.1: Forward, reverse and drain current of a transistor biased in strong inversion and in the linear region.

To bias transistor M_1 in the linear region, we can use the circuit of Figure 1.2, which is similar to a cascode stage except that in this case the transistor M_1 is biased in the linear region and in strong inversion. For a given gate bias voltage V_G, the bias voltage V_b applied at the gate of M_2 is set such that the drain voltage of M_1 is smaller than its saturation voltage $V_D < V_P \cong (V_G - V_{T0})/n$. Now, the

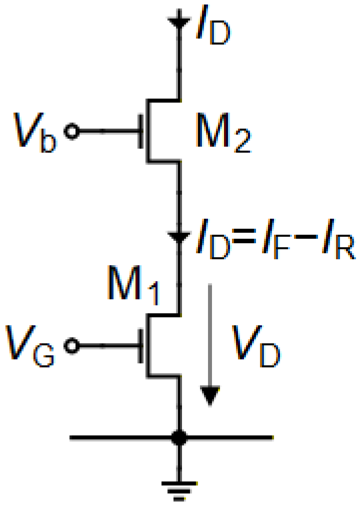

Figure 1.2: MOS transistor biased in the linear region

impedance at the drain node of M_1 is not zero and has an effect of the equivalent transconductance. We will study this in Problem 1.

- From Figure 1.1, estimate the input linear range assuming that it is limited by the supply voltage on the positive side.
- Derive the small-signal transconductance of the circuit shown in Figure 1.2. Assume that the output voltage is grounded and that M_1 is biased in the linear region and M_2 in the saturation region.
- Calculate the input-referred noise resistance R_{nin}, the input-referred thermal noise resistance R_{nt} and the equivalent thermal noise excess factor $\gamma_{neq} \triangleq G_{meq} \cdot R_{nt}$.

2 Problem 2: Low-voltage linearized transconductor

2.1 Introduction

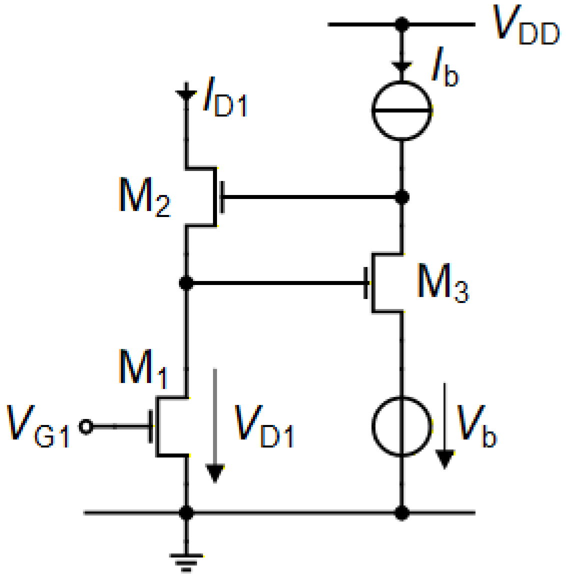

Figure 2.1: Linearized transconductor with regulated cascode.

Similarly to the cascode stage, we can reduce the impedance seen by the driver transistor M_1 at its drain by using a regulated cascode as shown in Figure 2.1. However, to bias M_1 in the linear region requires a negative bias voltage V_b.

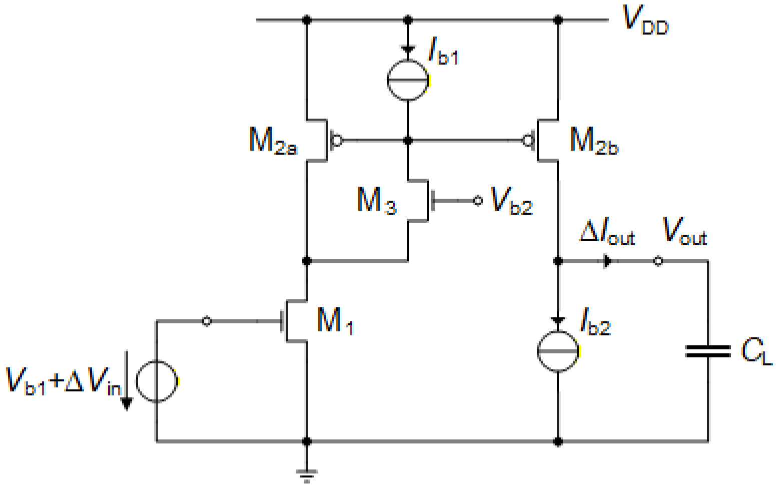

Figure 2.2: Low-voltage linearized transconductor [1].

This problem can be circumvented by using the low-voltage linearized transconductor shown in Figure 2.2 [1]. It is made of a driver transistor M_1 biased in the linear region by means of transistor

M_3 and the bias voltage V_{b2}. Transistors M_2 and M_4 form a current mirror (they have the same gate voltage), mirroring the current variation from M_1 to the output. The role of transistor M_3 is to maintain the V_{DS1} voltage as constant as possible to avoid any distortion. This is obtained by the feedback loop introduced by M_3 and M_2.

2.2 Small-signal analysis

- Draw the small-signal schematic of the circuit given in Figure 2.2, assuming that all the transistors are biased in saturation except for M_1 which is biased in the linear region.
- Derive the expression of the equivalent small-signal transconductance $G_{meq} = \Delta I_{out}/\Delta V_{in}$ for $\Delta V_{out} = 0$ where ΔV_{in} is the small-signal input voltage. Consider only the output conductance G_{ds} of M_3 and that M_{2a}-M_{2b} are perfectly matched and.

2.3 Noise analysis

- Draw the small-signal circuit inclduding all the noise sources.
- Derive an expression of the output noise conductance G_{nout} assuming that $G_{ms3} \gg G_{ds3}$.
- Calculate the input-referred noise resistance R_{nin}, the input-referred thermal noise resistance R_{nt} and the equivalent thermal noise excess factor $\gamma_{neq} \triangleq G_{meq} \cdot R_{nt}$.

References

[1] U. Yodprasit and C. C. Enz, "A 1.5-v 75-dB dynamic range third-order G_m-C filter integrated in a 0.18-μm standard digital CMOS process," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1189–1197, 2003, doi: 10.1109/JSSC.2003.813293.