Fundamentals of Analog VLSI Design
Exercise 10 - Problem

Mulitanh Linearized Differential Pair (Version 2)

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1 Introduction

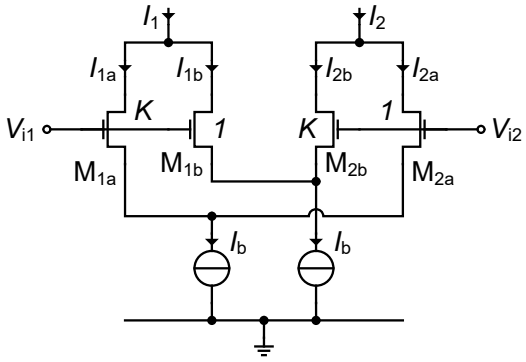

Figure 1.1: Linearized differential pair in weak inversion [1] [2].

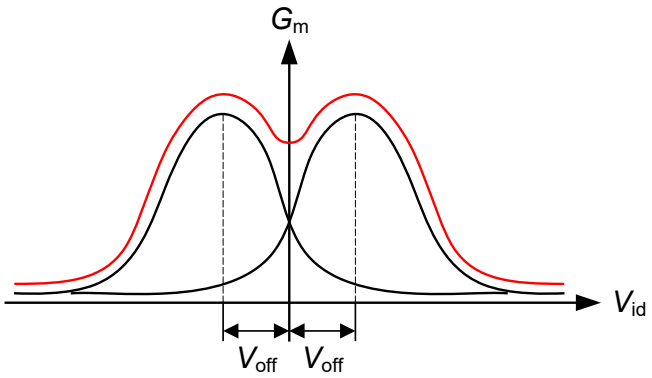

Figure 1.2: Principle of the linearized differential pair in weak inversion [1] [2].

Figure 1.1 shows a linearized differential pair operating in weak inversion [1] [2]. It is based on the principle illustrated in Figure 1.2. By making M_{2b} K-times larger than M_{1b} and M_{1a} K-times larger than M_{2a} results in introducing some offset voltage in the differential pairs M_{1a}-M_{2a} and M_{1b}-M_{2b} shifting their I-V characteristic as shown in Figure 1.2 by an offset voltage $V_{off} = n\,U_T \cdot \ln(K)$. The differential current $I_{od} \triangleq I_1 - I_2$ shows a more linear characteristics with an extended linear range [1].

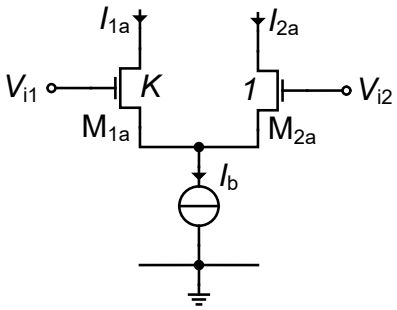

Figure 1.3: Half linearized differential pair a of Figure 1.1 in weak inversion with $\beta_{1a} = K \cdot \beta_{2a}$ [1].

The analysis of the linearized differential pair of Figure 1.1 can be done by separating the linearized differential pair into the differential pair a shown in Figure 1.3 and the differential pair b shown in Figure 1.4.

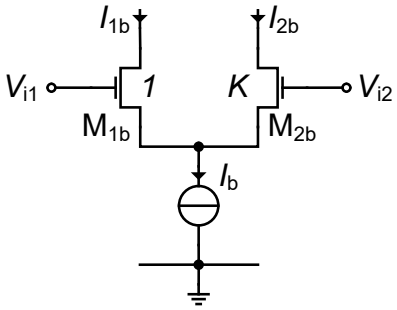

Figure 1.4: Half linearized differential pair b of Figure 1.1 in weak inversion with $\beta_{2b} = K \cdot \beta_{1b}$ [1].

2 Large-signal analysis

- Derive the expression of the differential current $I_{oda} \triangleq I_{1a} - I_{2a}$ of the half differential pair a shown in Figure 1.3 in differential mode i.e. with $V_{i1} = V_{ic} + V_{id}/2$ and $V_{i2} = V_{ic} - V_{id}/2$. Assume that both transistors are biased in weak inversion and in saturation with $\mathrm{M_{1a}}$ K-times larger than $\mathrm{M_{2a}}$ (i.e. $\beta_{1a} = K \cdot \beta_{2a}$). We can assume that $\mathrm{M_{1a}}$-$\mathrm{M_{2a}}$ have the same slope factors $n_{1a} = n_{2a} = n$, threshold voltages V_{T0n} and specific currents $I_{spec\square}$ (i.e. $I_{D01a} = K \cdot I_{D02a} = K \cdot I_{D0}$). Hint: use the offset voltage $V_{off} \triangleq n\,U_T \ln(K)$ or $K = e^{V_{off}/(n\,U_T)}$.
- Using the above result, deduce the large-signal differential current $I_{od} \triangleq I_1 - I_2$ of the linearized differential pair of Figure 1.1 in differential mode.

3 Small-signal analysis

- Draw the small-signal schematic of the half differential pair a shown in Figure 1.3, assuming that all the transistors are biased in weak inversion and in saturation. Derive the equivalent transconductance in differential mode $\Delta V_{i1} = -\Delta V_{i2} = \Delta V_{id}/2$

$$G_{meqa} \triangleq \frac{\Delta I_{oda}}{\Delta V_{id}} \tag{3.1}$$

  with $\Delta I_{oda} = \Delta I_{1a} - \Delta I_{2a}$ and $\Delta V_{id} = \Delta V_{i1} - \Delta V_{i2}$. Assume that the output conductances can be neglected.

- Derive the equivalent transconductance in differential mode for the other half differential pair b

$$G_{meqb} \triangleq \frac{\Delta I_{odb}}{\Delta V_{id}} \tag{3.2}$$

  with $\Delta I_{odb} = \Delta I_{1b} - \Delta I_{2b}$. Assume again that the output conductances can be neglected.

- Derive the equivalent small-signal transconductance $G_{meq} = \Delta I_{od}/\Delta V_{id}$ of the linearized differential pair of Figure 1.1, where $\Delta I_{od} \triangleq \Delta I_1 - \Delta I_2$ is the small-signal differential output current and $\Delta V_{id} = \Delta V_{i1} - \Delta V_{i2}$ is the small-signal input voltage. Reuse the expressions of the equivalent transconductances G_{meqa} and G_{meqb} of the half differential pairs a and b.

4 Noise analysis

- Derive the output noise conductance G_{nouta} and G_{noutb} of the half differential pairs a of Figure 1.3 and Figure 1.4, respectively, in terms of the transistor noise conductances including the noise coming from the bottom bias source.
- Derive the output noise conductance of the linearized differential pair of Figure 1.1 using the results obtained for the half differential pair.
- Calculate the input-referred noise resistance R_{nin} and the input-referred thermal noise resistance R_{nt}.
- Calculate the thermal noise excess factor $\gamma_{neq} \triangleq G_{meq} R_{nt}$ of the linearized differential pair.

References

[1] H. Tanimoto, M. Koyama, and Y. Yoshida, "Realization of a 1-v active filter using a linearization technique employing plurality of emitter-coupled pairs," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 7, pp. 937–945, 1991, doi: 10.1109/4.92013.

[2] J. Hauptmann, F. Dielacher, R. Steiner, C. C. Enz, and F. Krummenacher, "A low-noise amplifier with automatic gain control and anticlipping control in CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 7, pp. 974–981, 1992, doi: 10.1109/4.142591.