Fundamentals of Analog & Mixed Signal VLSI Design

Single-ended Differential Amplifiers
Part 3

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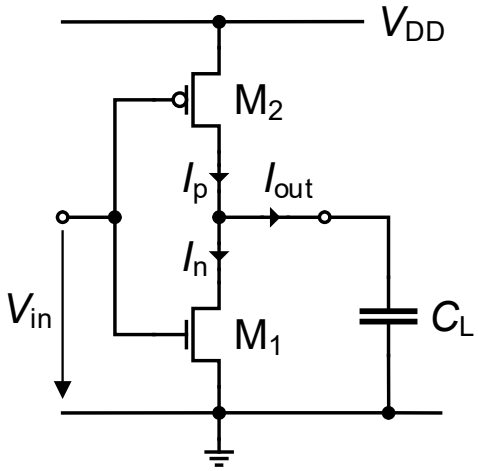
Outline

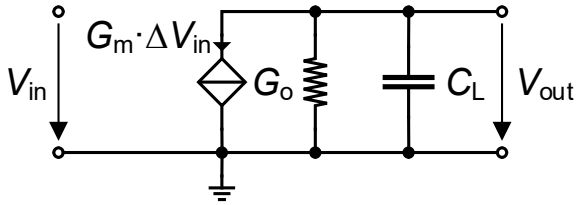
- **The CMOS inverter OTA**
- Improved slew-rate OTAs
- Appendices

The CMOS Inverter as an Amplifier



- The CMOS inverter can be used as a very efficient amplifier thanks to the current sharing between the nMOS and pMOS transistors
- The overall transconductance is the sum of the nMOS and pMOS transconductances
- In WI, the CMOS inverter can operate at very low-voltage thanks to the minimum saturation voltage achieved in WI

The CMOS Inverter – Small-signal and Noise Analysis



- The overall OTA G_m is the sum of the nMOS and pMOS G_m

$$G_m = G_{m1} + G_{m2} \cong 2G_{m1} = 2\frac{I_b}{nU_T}$$

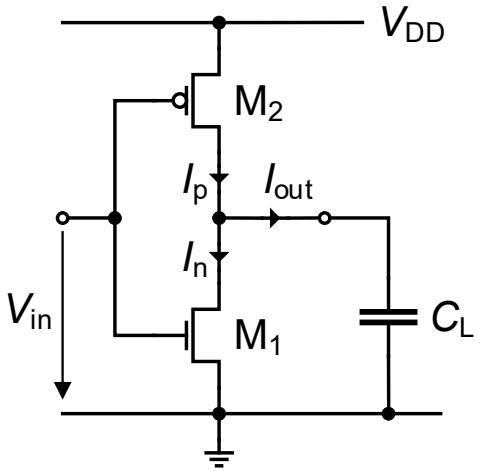
- which in WI is twice that of a single transistor since both transistors share the same bias current
- The DC gain is given by

$$A_{dc} = -\frac{G_m}{G_o} = -\frac{G_{m1} + G_{m2}}{G_{ds1} + G_{ds2}}$$

- and the noise is half that of a single transistor for the same bias current

$$R_n = \frac{G_{n1} + G_{n2}}{(G_{m1} + G_{m2})^2} = \frac{2\,\gamma_{n1} \cdot G_{m1}}{4\,G_{m1}^2} = \frac{\gamma_{n1}}{2G_{m1}} = \frac{R_{n1}}{2}$$

Large-signal Transfer Characteristic in WI



- Assuming that $n_1 = n_2 = n$ the output current $I_{out} = I_p - I_n$ is given by

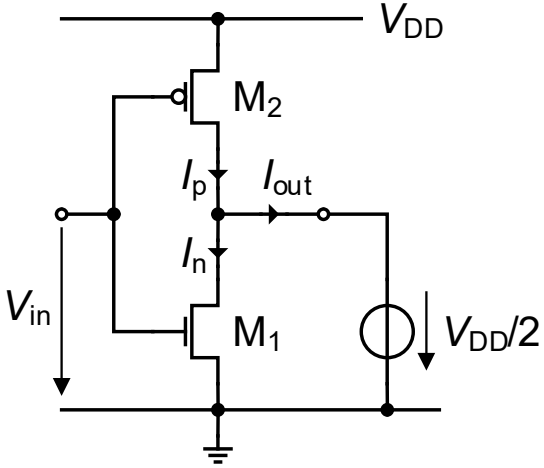
$$i_{out} \triangleq \frac{I_{out}}{I_b} = -2\sinh\left(\frac{V_{in} - V_b}{nU_T}\right)$$

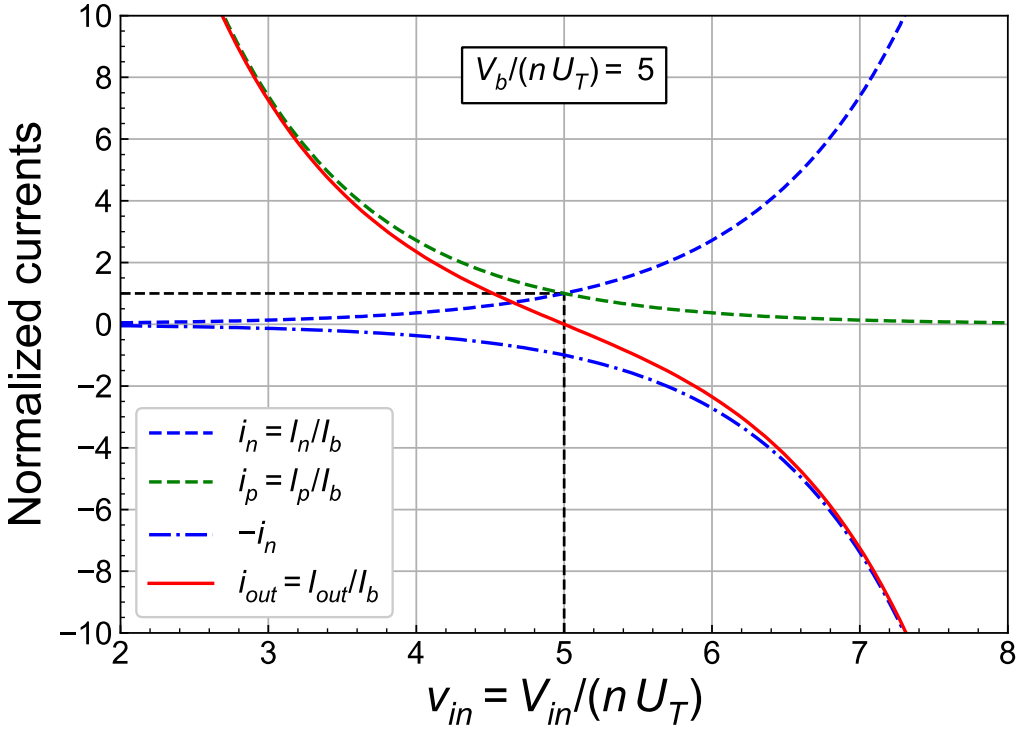
- V_b and I_b correspond to the quiescent gate and bias current for $I_{out} = 0$

$$I_b = I_{D01} \cdot e^{\frac{V_b}{nU_T}} = I_{D02} \cdot e^{\frac{V_{DD}-V_b}{nU_T}}$$

- where $I_{D01} = I_{spec1} \cdot e^{\frac{-V_{T0n}}{nU_T}}$ and $I_{D02} = I_{spec2} \cdot e^{\frac{-V_{T0p}}{nU_T}}$
- with $I_{spec1} = I_{specn\square} \cdot \frac{W_1}{L_1}$ and $I_{spec2} = I_{specp\square} \cdot \frac{W_2}{L_2}$

Class AB Transfer Characteristic

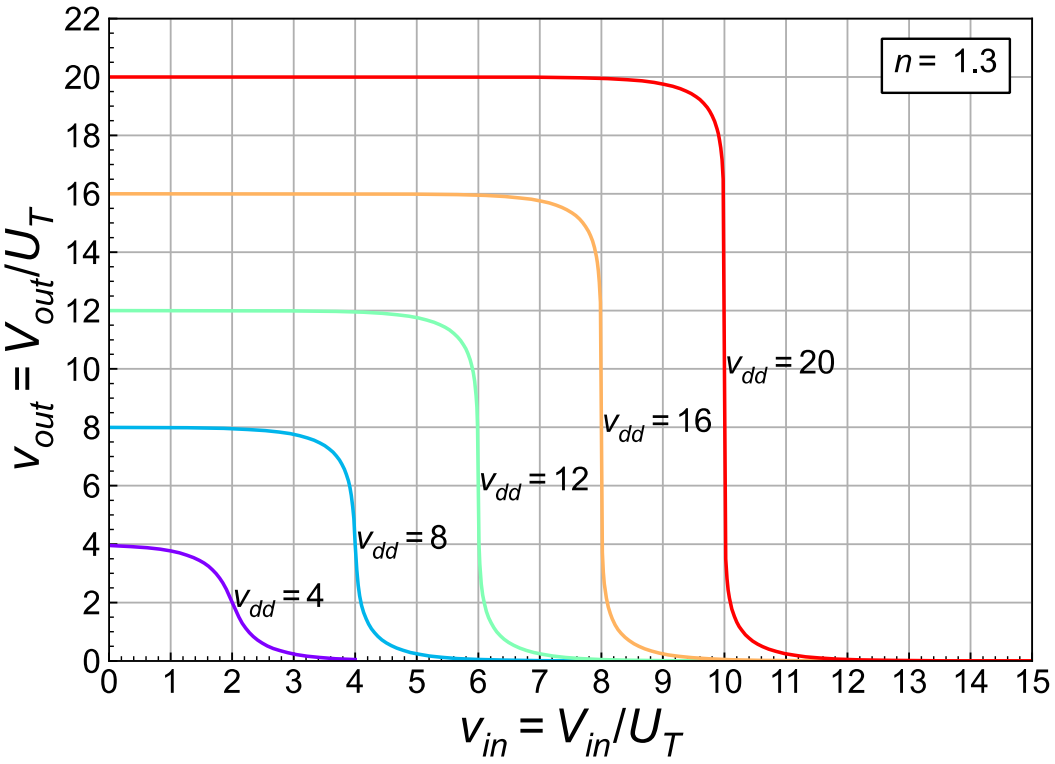




- The current is not limited by a bias current but by the supply voltage
- The class AB transfer characteristic is shown above for the case $V_b = V_{DD}/2$
- The use of inverters was proposed by Krummenacher already in 1981 for designing micropower SC filters

📖 F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.

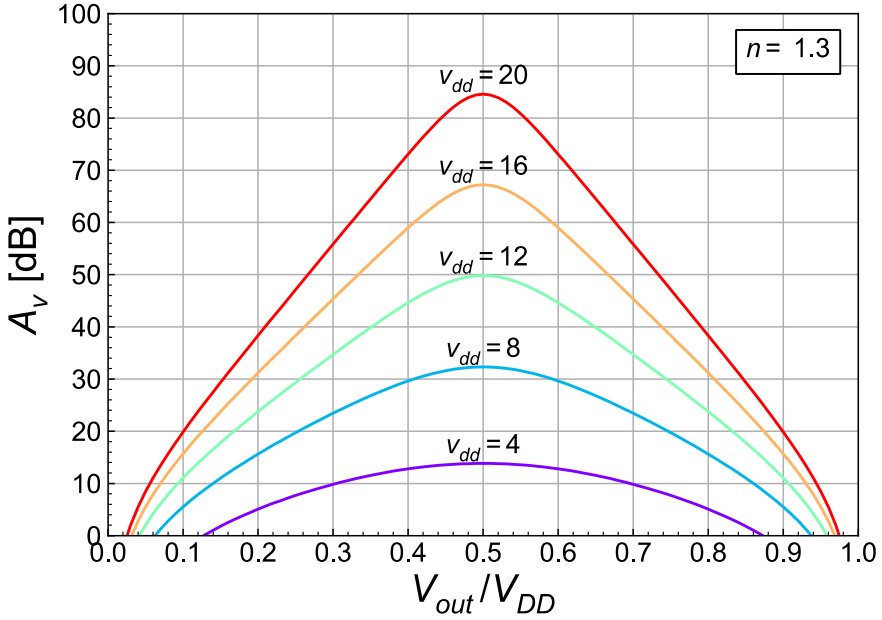
Large-signal Transfer Characteristic in WI

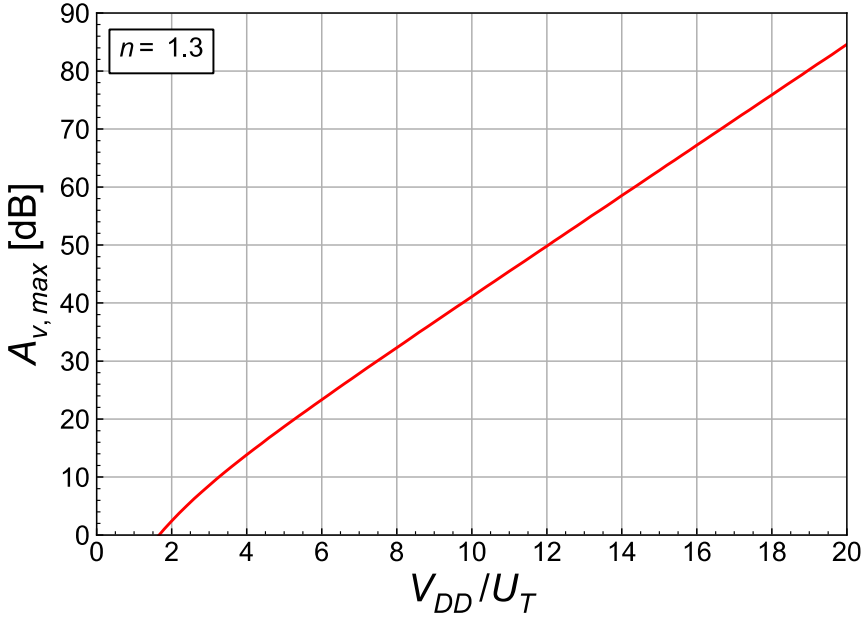


- Assuming $n_1 = n_2 = n$, $I_{D01} = I_{D02}$ and neglecting SCE (DIBL and CLM)
- Can operate at very low supply voltage still providing some voltage gain

E. Vittoz, "Analog Circuits in Weak Inversion" in *Sub-threshold Design for Ultra Low-Power Systems*, Springer 2006.
E. Vittoz, "Weak Inversion for Ultimate Low-Power Logic" in *Low-Power Electronics Design*, Ed. C. Piguet, CRC Press 2005.

Voltage Gain





- Large DC gain can be obtained at very low-voltage, provided
  - low, controlled threshold voltages are available
  - adequate bias scheme is implemented
- Of course the large voltage gain shown above can be significantly lower because of SCE such as DIBL

E. Vittoz, "Analog Circuits in Weak Inversion" in *Sub-threshold Design for Ultra Low-Power Systems*, Springer 2006.
E. Vittoz, "Weak Inversion for Ultimate Low-Power Logic" in *Low-Power Electronics Design*, Ed. C. Piguet, CRC Press 2005.

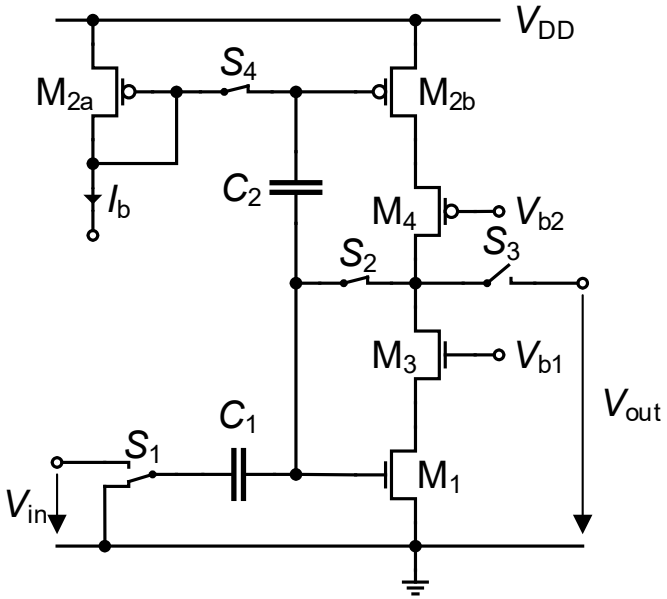
The CMOS Inverter in Weak Inversion

- The CMOS inverter has many great features particularly when it is biased in WI, including:
  - Maximum transconductance at given current I_b
    (global G_m is doubled for the same bias current since in WI $G_m \propto I_b$)
  - Maximum DC gain
  - Minimum input-referred white noise at given current I_b
  - Intrinsically class AB
  - Very low-voltage operation
- However it suffers from a major drawback, namely
  - Poor intrinsic PSRR (6 dB)!
- The later can be circumvented by adding a voltage regulator
- In SI and saturation, for long-channel transistors with for $\beta_1/n_1 = \beta_2/n_2$, the OTA operates as a linear transconductor

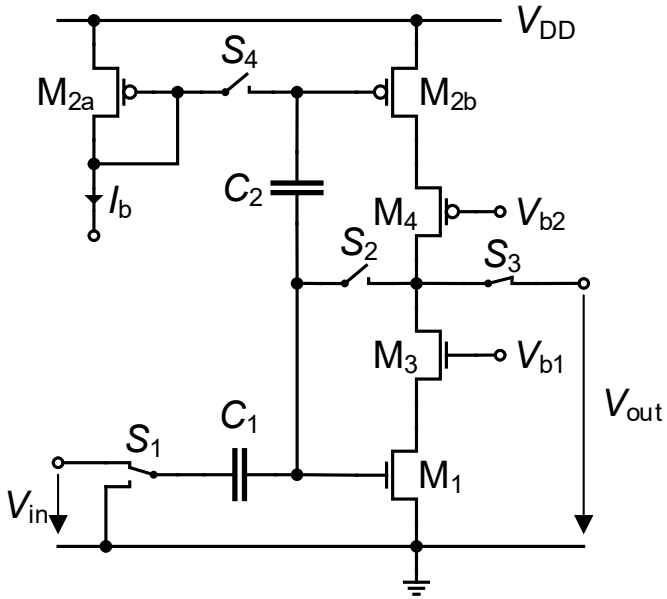
F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.
E. Vittoz, "Analog Circuits in Weak Inversion" in *Sub-threshold Design for Ultra Low-Power Systems*, Springer 2006.

Dynamically Biased Inverter Amplifier (1/2)

Phase Φ_1 (Autozero)



Phase Φ_2 (Amplification)

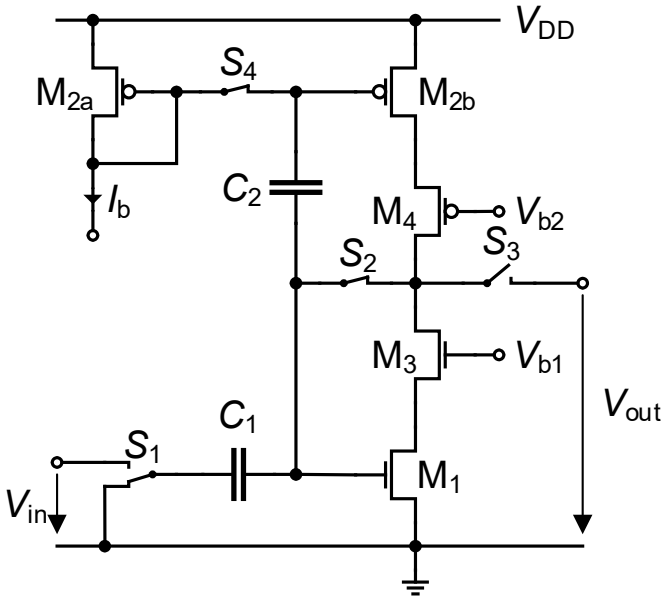


- Two non-overlapping phases operation
- During phase Φ_1, the amplifier is disconnected from the input and the bias current is imposed in the inverter
- At the end of phase Φ_1, the bias voltages are sampled on C_1 and C_2 ideally maintaining the bias current I_b in the inverter during the amplification phase Φ_2

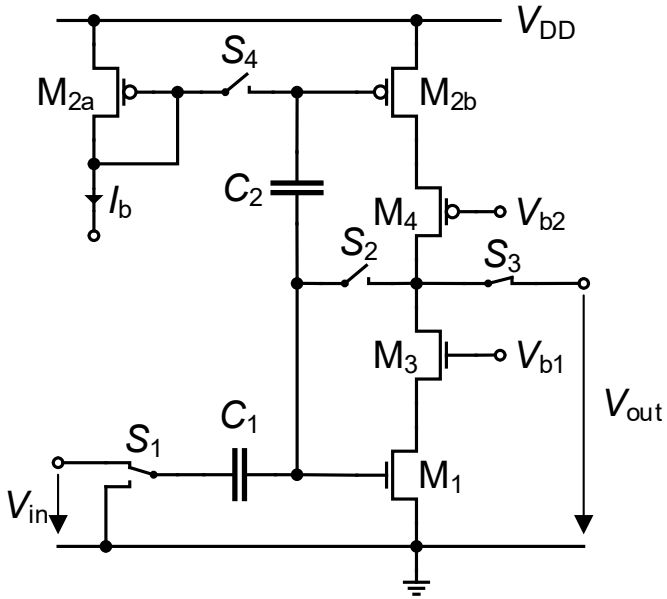
📖 F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.

Dynamically Biased Inverter Amplifier (2/2)

Phase Φ_1 (Autozero)



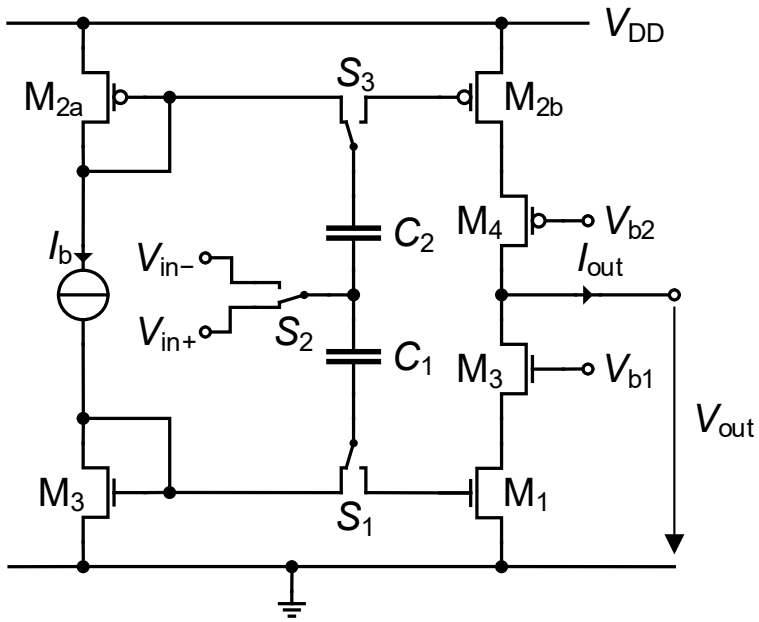
Phase Φ_2 (Amplification)



- Pros:
  - Good low-frequency PSRR
  - No offset
  - Reduction of 1/f noise by autozero
  - Flexible input common-mode
- Cons:
  - Two non-overlapping phases
  - Discontinuous operation
  - Systematic step at output
  - Charge injection

F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.

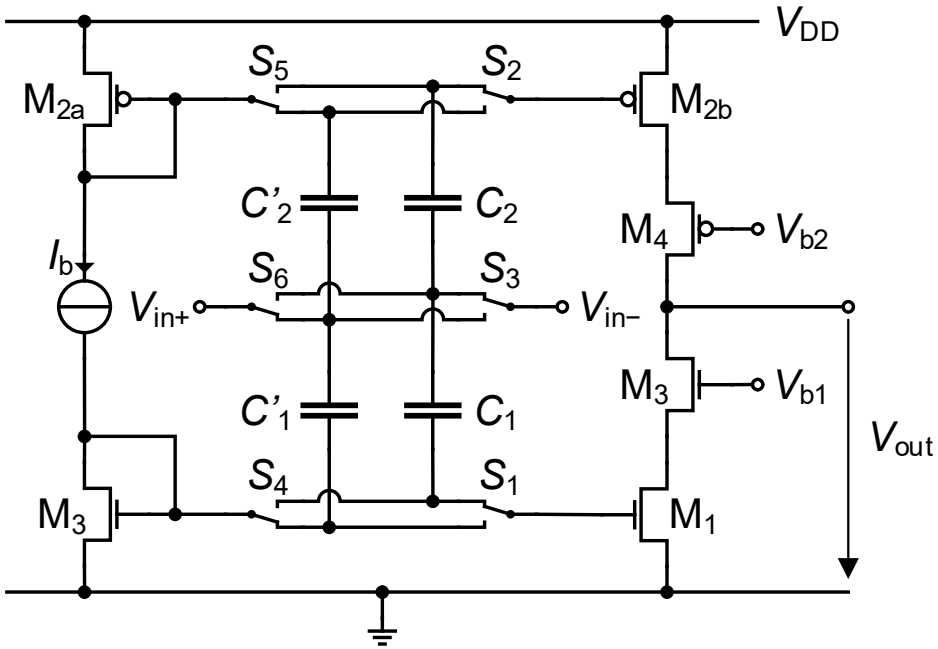
Differential Dynamically Biased Inverter Amplifier



- The above circuit provides a differential input
- In most SC circuits, the positive input is set to a certain commode-mode voltage
- The above circuit samples the bias voltage during phase Φ_1 referenced to the common-mode voltage imposed on the positive input
- The bias voltage sampled on C_1 and C_2 are then applied to M_1 and M_{2b} during the amplification phase Φ_2

S. Masuda, Y. Kitamura, S. Ohya, and M. Kikuchi, "CMOS Sampled Differential, Push Pull Cascode Operational Amplifier," ISCAS 1984.

Differential Dynamically Biased Inverter Amplifier



- The above circuit can operate during both phases Φ_1 and Φ_2
- Indeed, the amplifier inputs (gates of M_1 and M_{2b}) are always connected to the negative input, while the gates of M_{2a} and M_3 are always connected to the positive input
- This OTA can therefore directly replace the OTAs in SC filters

S. Masuda, Y. Kitamura, S. Ohya, and M. Kikuchi, "CMOS Sampled Differential, Push Pull Cascode Operational Amplifier," ISCAS 1984.

Outline

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- **Improved slew-rate OTAs**
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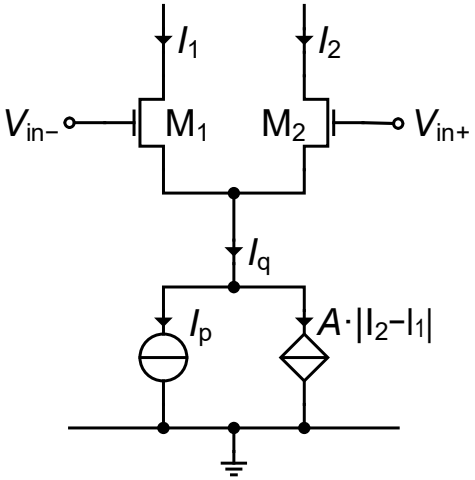
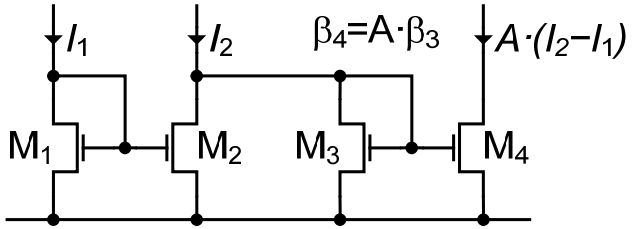
Differential Feedback Amplifier – Principle





- **Settling time** of simple OTAs having their input differential pair biased in WI is set by the **slew-rate**
- Limited slew rate due to small currents can be circumvented by using **adaptive biasing**
- Principle: increase the differential pair bias current for large differential input signals

$$I_q = I_p + A \cdot |I_2 - I_1| \text{ with } I_q = I_1 + I_2$$

📖 M. Degrauwe, *et al.*, JSSC, 1985

Differential Feedback Amplifier – Output Current

- It can be shown that currents I_1 and I_2 depend on $V_{in} \triangleq V_{in+} - V_{in-}$ according to

$$i_1 \triangleq \frac{I_1}{I_p} = \frac{1}{1+A+(1-A)e^{v_{in}}} \text{ and } i_2 \triangleq \frac{I_2}{I_p} = \frac{e^{v_{in}}}{1+A+(1-A)e^{v_{in}}} \text{ with } v_{in} \triangleq \frac{V_{in}}{nU_T}$$

- Resulting in the output current $I_{out} = I_2 - I_1$ given by

$$i_{out} \triangleq \frac{I_{out}}{I_p} = i_2 - i_1 = \frac{\tanh\left(\frac{v_{in}}{2}\right)}{1 - A\tanh\left(\frac{v_{in}}{2}\right)}$$

- In the particular case where there is no feedback ($A = 0$) we recover the differential pair transfer characteristic

$$i_{out} = \tanh\left(\frac{v_{in}}{2}\right)$$

- For $0 < A < 1$, the output current is limited to $I_p/(1-A)$
- For $A \geq 1$, the output current is no longer limited to the bias current I_p
- The output current tends to infinity for a critical value of the input voltage given by

$$V_{in,crit} = nU_T \cdot \ln\left(\frac{A+1}{A-1}\right)$$

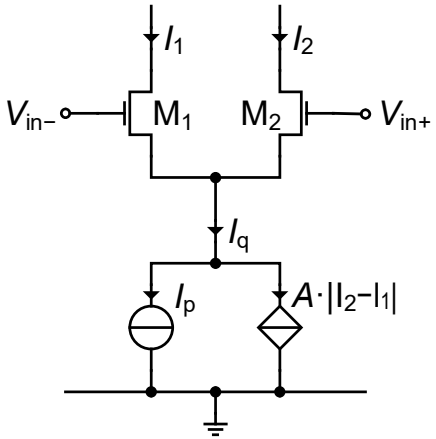
- For $A = 1$, one of the two branches remains at $I_p/2$ i.e. $min(I_1, I_2) = \frac{I_p}{2}$ and the output current becomes

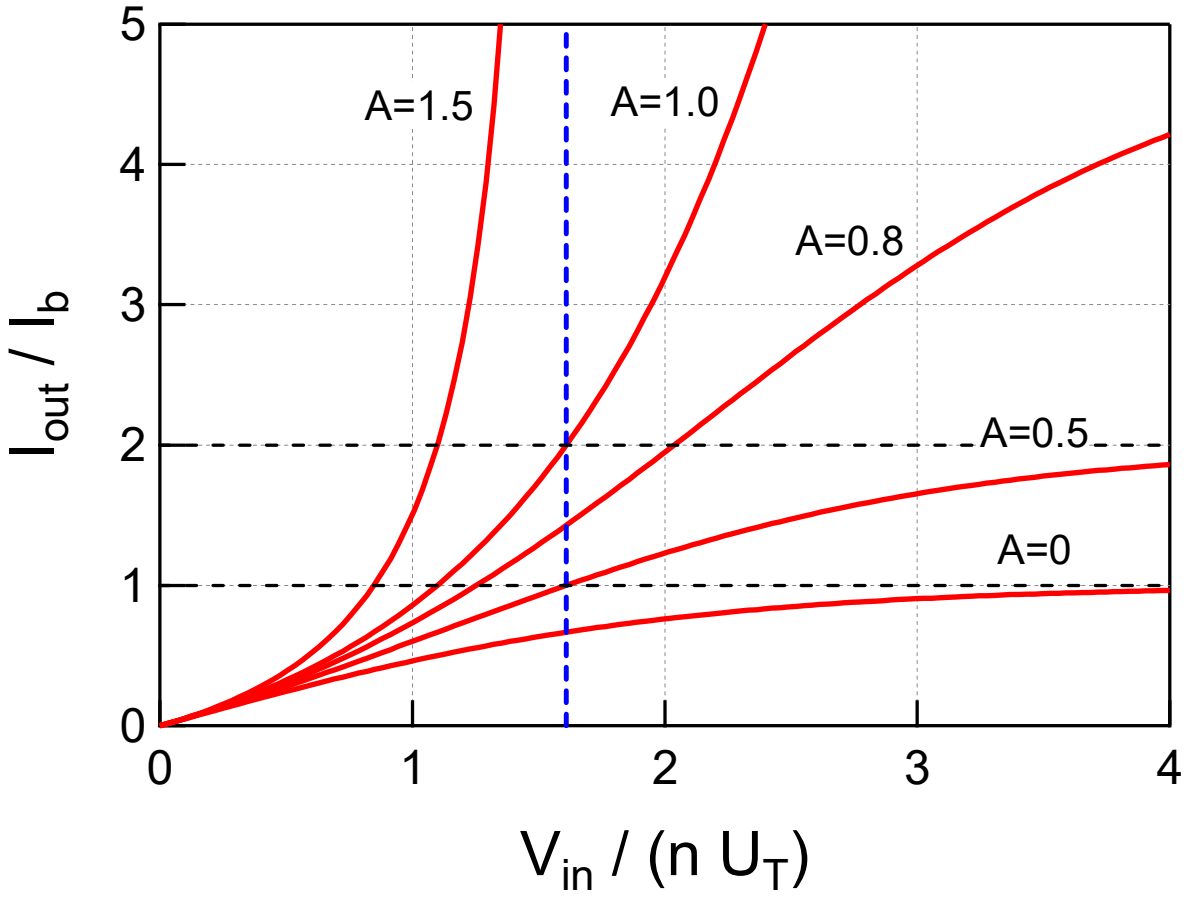
$$i_{out} = \tfrac{1}{2}(e^{v_{in}} - 1)$$

📖 M. Degrauwe, *et al.*, JSSC, 1985

Differential Feedback Amplifier – Output Current

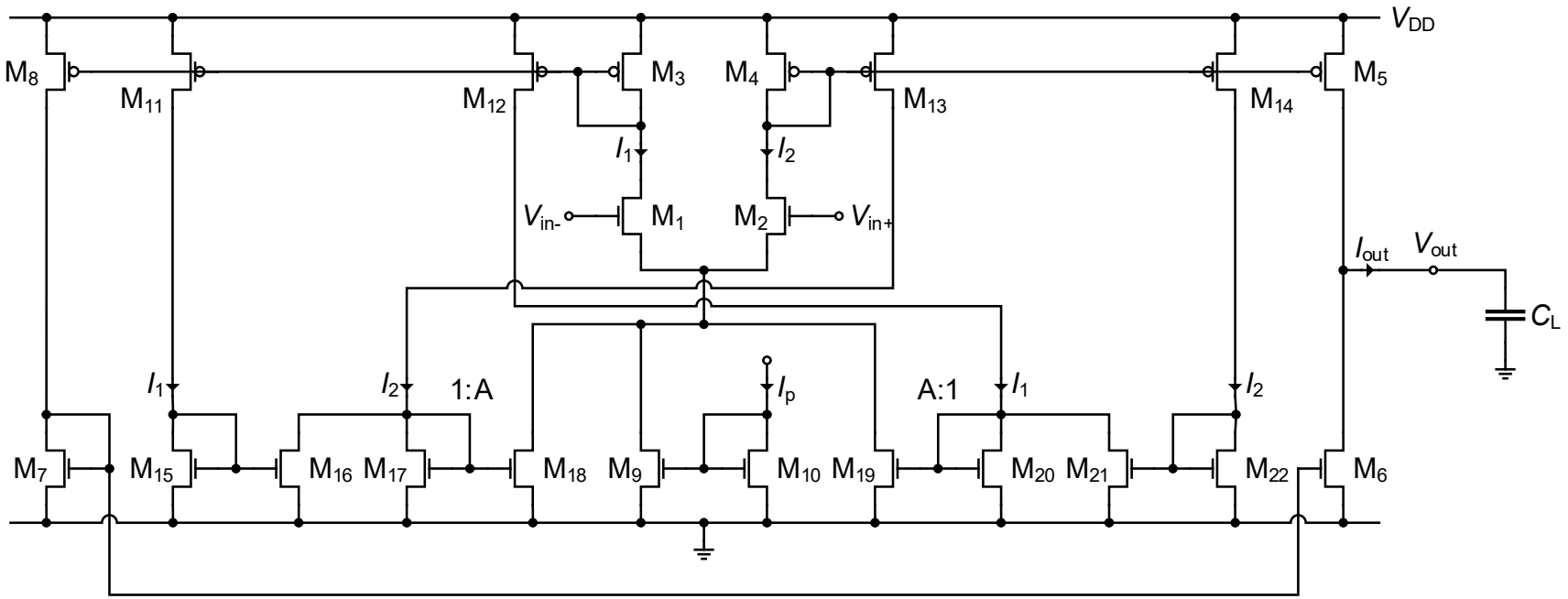
$$I_{out} = I_2 - I_1$$
$$V_{in} = V_{in+} - V_{in-}$$





M. Degrauwe, *et al.*, JSSC, 1985

Differential Feedback Amplifier – Differential OTA



- Transistors M_1 to M_{10} implement the symmetrical OTA, whereas transistors M_{11} to M_{22} implement the two feedback networks

📖 M. Degrauwe, *et al.*, JSSC, 1985

Differential Feedback Amplifier – Experimental Validation

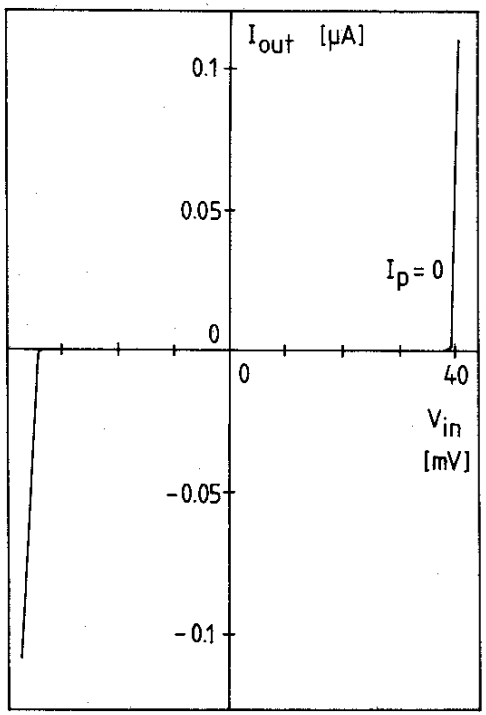


Fig. 8. Measured output current for $I_p = 0$.

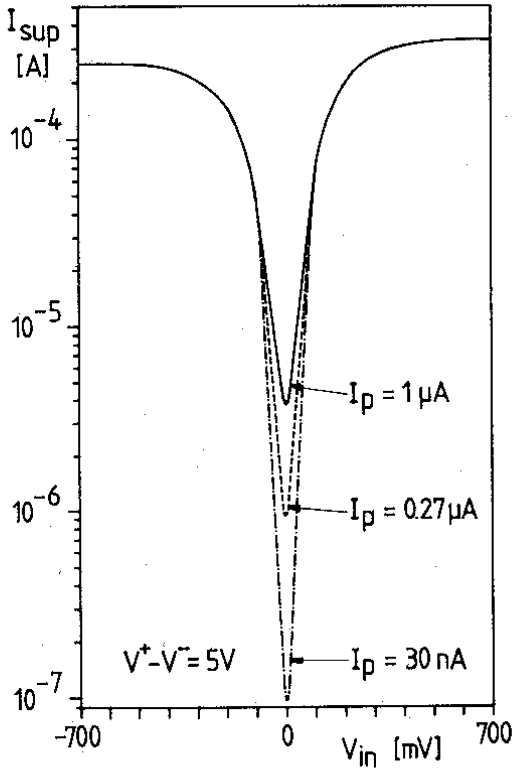
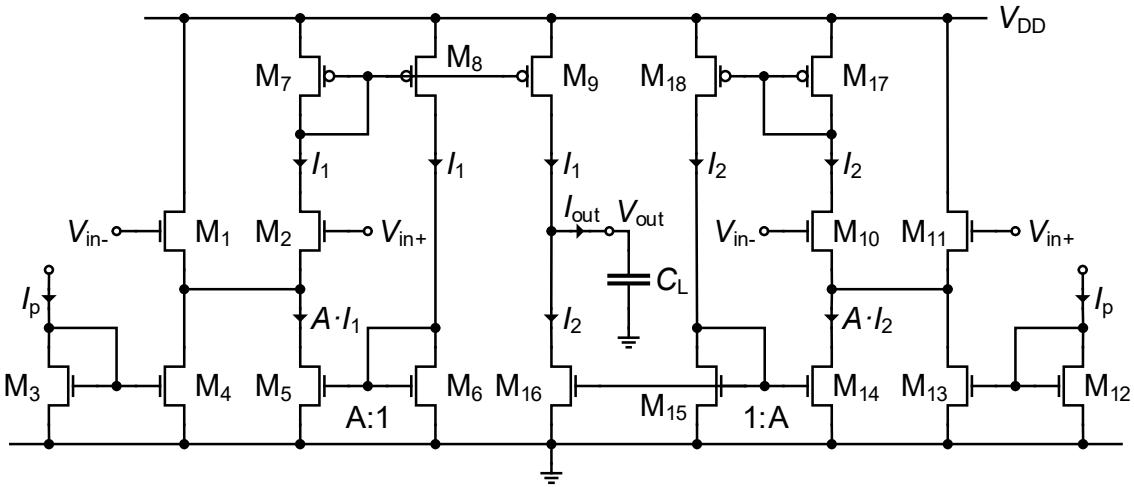


Fig. 9. Supply current as a function of the input signal.

M. Degrauwe, *et al.*, JSSC, 1985

Direct Feedback Amplifier – Principle



- When the differential input voltage $V_{in} = V_{in+} - V_{in-}$ equals zero, the quiescent currents I_1 and I_2 are equal and given by

$$I_{1(2)} = \frac{1}{2} \cdot \left(I_p + A \cdot I_{1(2)}\right)$$

- Which can be solved for I_1 and I_2 resulting in

$$I_1 = I_2 = I_0 = \frac{I_p}{2 - A}$$

- Stability is then insured for a current gain $A < 2$

📖 M. Degrauwe, *et al.*, JSSC, 1985

Direct Feedback Amplifier – Output Current

- It can be shown that currents I_1 and I_2 depend on V_{in} according to

$$i_1 \triangleq \frac{I_1}{I_p} = \frac{1}{1-A+e^{-v_{in}}} \text{ and } i_2 \triangleq \frac{I_2}{I_p} = \frac{1}{1-A+e^{+v_{in}}} \text{ with } v_{in} \triangleq \frac{V_{in}}{nU_T}$$

- Resulting in the output current $I_{out} = I_1 - I_2$ is given by

$$i_{out} \triangleq \frac{I_{out}}{I_p} = i_1 - i_2 = \frac{2\sinh(v_{in})}{1+(1-A)^2+2(1-A)\cosh(v_{in})}$$

- In the particular case where there is no feedback ($A = 0$) we recover the differential pair transfer characteristic

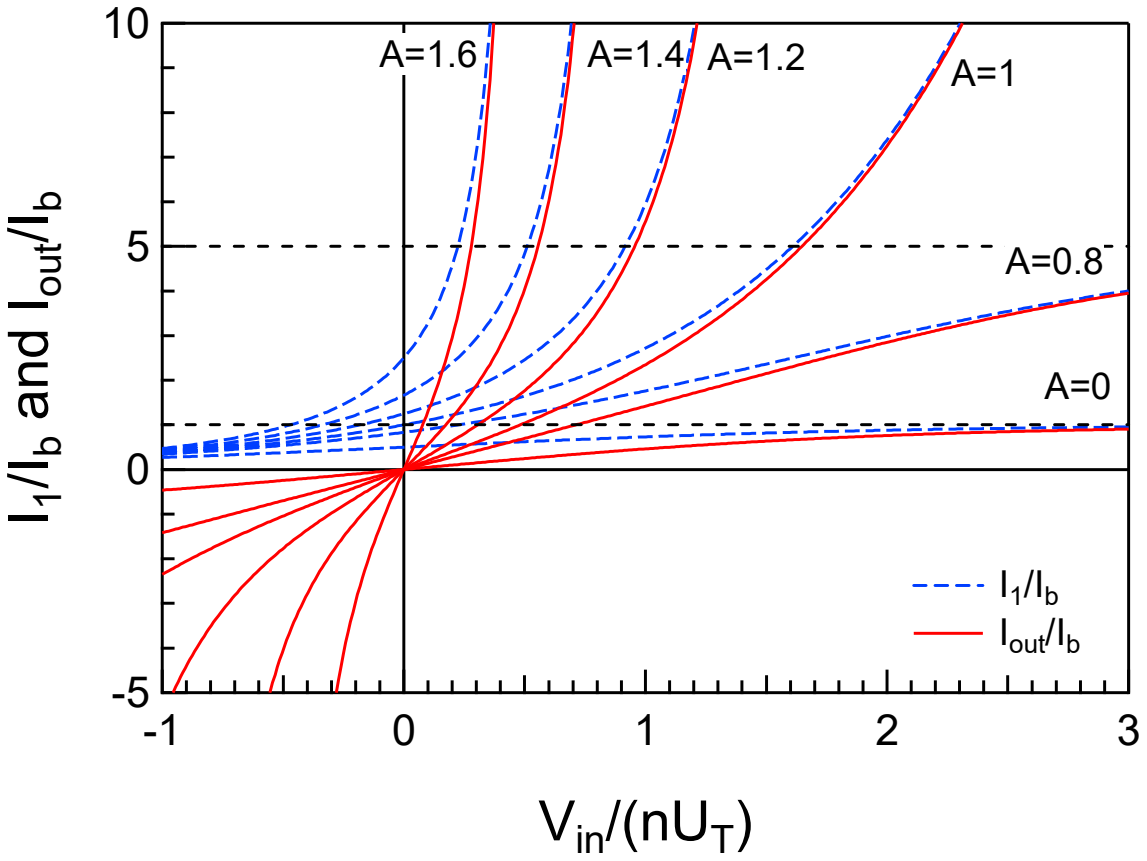
$$i_{out} = \tanh\left(\frac{v_{in}}{2}\right)$$

- For $A < 1$, the output current is limited to $I_p/(1-A)$
- For $A = 1$, the currents become exponential and the output current is no more limited and becomes

$$i_{out} = 2\sinh(v_{in})$$

- For $A > 1$, the current tends to infinity for $v_{in} = \cosh^{-1}\left(\frac{A^2-2A+2}{2(A-1)}\right)$

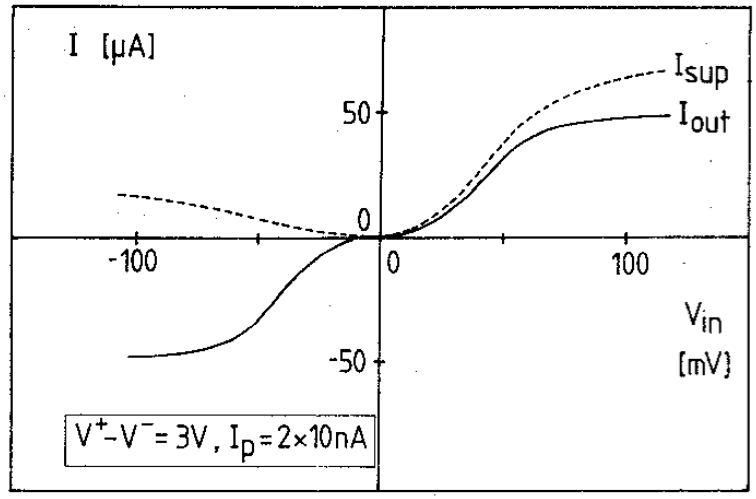
Direct Feedback Amplifier – Output Current

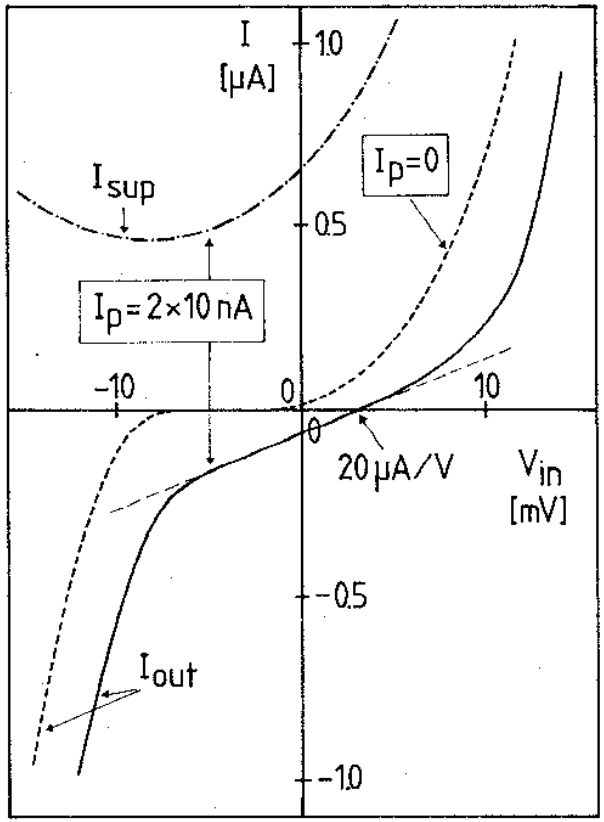


- As shown in the next slide, the output current will be limited by the maximum current that can be provided by the supply

Direct Feedback Amplifier – Experimental Validation

$$A = 1.4$$





M. Degrauwe, *et al.*, JSSC, 1985