

# **EE-334**

# **Digital System Design**

## **Organization and Outline of the Course**

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# Content and Focus of this Course

- **Focus on the design of Digital Systems**
  - **based on hardware** as opposed to software
  - **using** state-of-the-art **abstraction** to be able to design complex circuits
  - **realize them** on programmable logic (**FPGAs**) devices
    - Note that the same concepts also apply to ASICs
- **To efficiently design and optimize such systems we need**
  - A design methodology with corresponding theory **SYNCHRONOUS DESIGN**
  - Suitable way to describe hardware **(V)HDL**
  - Tools to expand the abstract description **XILINX Vivado**

# Specific Topics

- **Specifically we will**
  - **See how to approach the design of a complex system** from different components and on different levels of abstraction
  - **Introduction to register transfer level design**
    - describe and control structures and datapaths
    - apply systematic transformations to explore tradeoffs between area and speed
  - **Introduce the principles and rules of synchronous digital design**
    - determine, optimize, and verify the speed of a design
    - investigate tradeoff between different metrics
  - **Introduce VHDL** as a language for simulation, synthesis, and verification HW
    - have a library of useful VHDL models and templates to build digital systems
  - Practice the steps for **verifying and implementing** a system **on FPGAs**
- **Topics will be interleaved to be able to apply theory early on**

# Organization of the Class

- **The class comprises**
  - **Theory lectures** on
    - Theoretical background and the methodology
    - Hardware description language VHDL
  - **Theoretical pen & paper homework** partially to prepare for the lab
    - Solving the exercises BEFORE the lab will make things much easier (believe me 😊)
  - **Small labs** to practice VHDL and get warm with the tools
    - In groups of two (max 3)
  - **A project**
    - In groups of two (max 3)
- **Exercises and labs built on each other, so try not to fall behind!**

# Schedule

- 4 ECTS credit course: 4h in class (+ up to 4h homework)
  - Allocate some time to work on the project outside the class hours

## Semester

 Fall


## Credits

4

## Lecture

2 Hour(s) per week x 14 weeks

## Exam form

 Written

## Subject examined

Digital systems design

## Exercises

2 Hour(s) per week x 14 weeks

- **Lectures/Labs/Q&A:**

- Lectures:

BS 170

- Lab sessions:

INF 3

**In groups of two (max 3)**

- Q&A sessions:

On Site during Lecture/Labs

- **Schedule:**

**Wednesday 08:15-12:00**

- **CHECK SCHEDULE** (Lecture/Lab) **REGULARLY ON MOODLE**

- **ATTEND ALL LECTURE AND LAB SESSIONS** as scheduled

	Mo	Tu	We	Th	Fr
8-9			INF3 BS170		
9-10					
10-11			INF3 BS170		
11-12					
12-13					
13-14					
14-15					
15-16					
16-17					
17-18					

# Exams and Grading

- **Grading is based on**
  - Final project
    - project report in form of a presentation & code
  - Final exam
    - Pen and Paper & on computer
    - Skills from exercises/labs/project help you significantly for the exam (similar tasks)

	<b>Weight</b>	
• <b>Project:</b>	<b>50%</b>	<b>during the semester</b>
<b>Final Exam</b>	<b>50%</b>	<b>during the exam session</b>

# Logistics

- **Labs require access to an FPGA board and FPGA design tools**
- **Labs and projects in groups of two (max 3)**
- **Access to FPGA boards**
  - We provide at least **one board per group** of two (to be returned by end of the semester)
  - Collection of the boards:
    - Week 2 of the semester during the class (pls. be there).
- **Access to XILINX Software:** details / instructions on Moodle
  - Installation on your personal computer (best, but resource expensive... 20GByte on disk)
  - Use **computers in any EPFL computer room**
    - **Program FPGAs with your laptop and a light version of the tools**  
(or on the computers in ELG 022)

# Detailed Course Schedule 2025

Wk	Date	Room	Time	Content
1	10 Sep		8h15 – 11h00 11h15 – 12h00	Organization of the Course Introduction to Digital Systems and Components Fundamentals of Synchronous Design Exercises: System Level Design & RTL Design Basics (drawing block diagrams)
2	17 Sep		8h15 – 09h00 9h15 – 10h00 10h15 – 12h00	FPGA Background Introduction to VHDL: HDLs, MODELING & DESIGN, HDL-based Design Flow VHDL for RTL Design and Synthesis (Fundamental Structure) & Packages Vivado Tutorial: get to know the tools
3	24 Sep		8h15 – 11h00 11h15 – 12h00	VHDL for Synthesis (Part 1): Concurrent statements More VHDL for Synthesis: (Part 2) Processes and Sequential Statements Exercise: Block Diagram of PWM Controller
4	01 Oct		8h15 – 12h00	RTL to VHDL and Vice-Versa VHDL Introductory example: PWM Controller
5	08 Oct		8h15 – 10h00 10h15 – 11h00 11h15 – 12h00	Finite State Machines VHDL for Simulation and Testbenches Exercise (preparation): Finite State Machine on paper: Door Lock
6	15 Oct		8h15-10h00 10h15-12h00	Timing of Synchronous Circuits From Algorithms to Architecture (Part 1) Exercise on Static Timing Analysis

# Detailed Course Schedule 2025

Wk	Date	Room	Time	Content
	22 Oct			VACATION
7	29 Oct		08h15 – 12h00	FSMs in VHDL: Door Lock RTL & Testbenches
8	05 Nov		8h15 -11h00 11h15 – 12h00	From Algorithms to Architecture (Part 2) Fixed Point Arithmetic and Datapath in VHDL Exercise from Algorithms to Architectures using Mandelbrot
9	12 Nov		08h15 – 12h00	Exercise: Lab on Simulating and Debugging VHDL
10	19 Nov		8h15 – 9h00 9h15 – 12h00	Project Intro, Video Interface & VGA Project: VGA Interface
11	26 Nov		8h15 – 12h00	Project: Pong (Video Memory & Pong Game)
12	03 Dec		8h15 – 10h00 8h15 – 12h00	Mandelbrot Data Paths Project: Pong (Mandelbrot)
13	10 Dec		8h15 – 12h00	Project: Pong
14	17 Dec		8h15 – 12h00	Project: Pong PRESENTATIONS

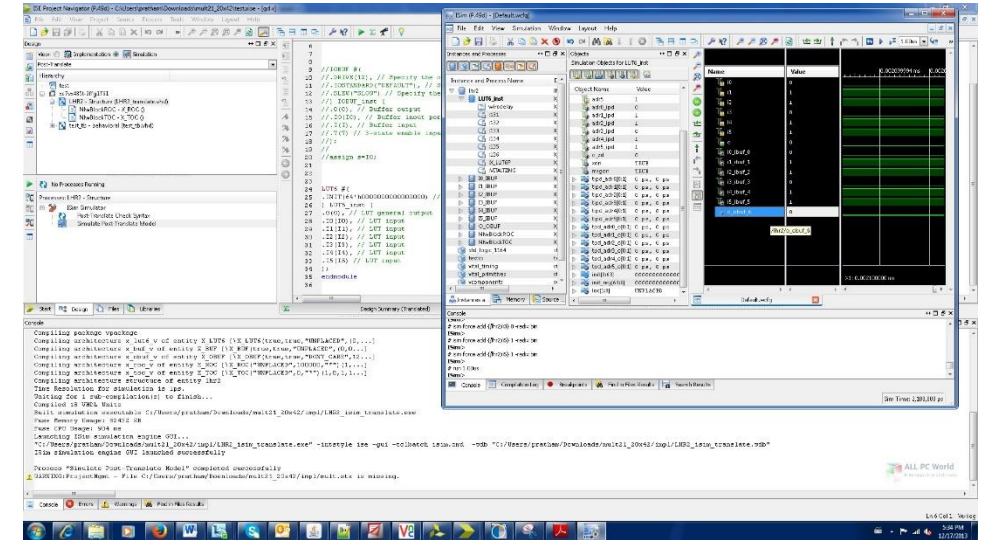
THEORY CLASS

VHDL LANGUAGE CLASS

LAB/EXERCISE SESSION

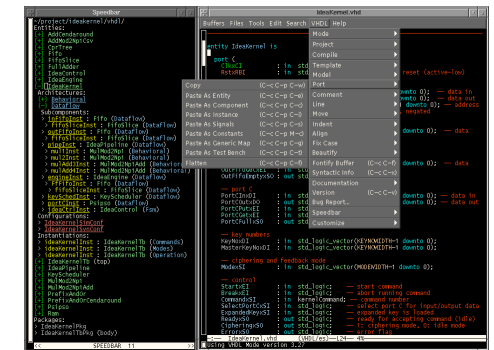
# EDA Tools

- **Xilinx VIVADO** - FPGA tool suite (all-in-one)
  - Project management and design flow automation
  - Design entry (editor)
  - VHDL simulation
  - Synthesis
  - Place & Route
  - FPGA programming
  - (In-system) debug



<https://www.xilinx.com/products/design-tools/vivado.html>

- **EMACS (with VHDL mode)** – Text editor
    - Design entry with LOTS OF SUPPORT for easy typing and VHDL language
    - Optional: initially painful, but will make your life so much easier after a while
- <http://doc.endlessparentheses.com/Fun/vhdl-mode.html>
- <https://www.gnu.org/software/emacs/refcards/pdf/refcard.pdf>



See Moodle for links to installers and manuals



# Literature

- Slides from the lecture will be weekly available on Moodle
- Videos from previous editions of the course (Note: not all material may be included in the recordings and the exam and course requirements are based on the in-presence course from this year)
- Hubert Kaeslin, “**Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication**”, Cambridge Univ Press, 2008, ISBN:9780521882675 (available in the Rolex-Center Library)
- P. Ashenden, “**The Designer's Guide to VHDL**”, 3<sup>rd</sup> ed.: Morgan Kaufmann (MK), 2008.
- P. Ashenden, “**Digital Design - An Embedded Systems Approach Using VHDL**”, MK, 2008.
- P. Ashenden, J. Lewis, “**VHDL-2008 - Just the New Stuff**”, MK, 2008.
- P. P. Chu, “**RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability**”, Wiley-Interscience, 2006.
- S. Moutault, J. Weber, M. Meaudre, “**Le langage VHDL - Du langage au circuit, du circuit au langage**”, 4e éd.: Dunod, 2011.
- A. Rushton, “**VHDL for Logic Synthesis**”, 3<sup>rd</sup> ed.: Wiley, 2011.
- A. Vachoux, “**VHDL Instant**”, EPFL, 2013.
- IEEE, “**1076-2008: IEEE Standard VHDL Language Reference Manual**”, IEEE, 2009.