EE-320 ANALOG IC DESIGN TP-2025/2026
PRACTICAL EXERCISE SESSION No. 4

Note: For students connecting virtually, the details of the Zoom Meeting for the TP sessions are given below (The same link, meeting ID, and passcode are valid for all 4 TP sessions)

Meeting link:
https://epfl.zoom.us/j/63888844351?pwd=dbKCKx75b0Y9tfd7sqfjJ0WXUhjRxX.1
Meeting ID: 638 8884 4351
Passcode: 354172

In this TP, we will

- Introduce layout and do the layout for the "diff" cell that we created in TP-3.
- Introduce current mirrors and replace the ideal tail current source ("idc" from analogLib) in TP-3 differential amplifier "tb_diff" with a NMOS based current source

1. Layout of NMOS differential pair

We will now layout the differential pair we designed in TP-3. To start the layout, open the "diff" schematic and from the top toolbar choose **Launch > Layout XL**. In the **Startup Option** pop-up, choose **Create New** option under **Layout**, **Automatic** option under **Configuration** and press OK to all future pop-ups. This will open a blank layout canvas corresponding to the schematic. To the left of the layout window, you see a palette showing the layers that are available in the design kit for the layout.

Following are a set of useful keyboard shortcuts listed below that are very handy while drawing the layout:

Shortcut	Menu Point	Description
i	Create > Instance	Instantiate another design/device in the current design
r	Create > Rectangle	Create a rectangle for drawing any layer in layout
p	Create > Path	Draw path with pre-defined width between two points
o	Create > Contact	Add contacts/vias between multiple layers from the technology library
l	Create > Label	Create labels to indicate the terminals in the layout
q	Create > Properties	View and edit properties of the geometry in the layout
c	Edit > Copy	Copy any shape, instances in the layout
m	Edit > Move	Move any shape, instances in the layout
s	Edit > Stretch	Stretch any shape one side at a time

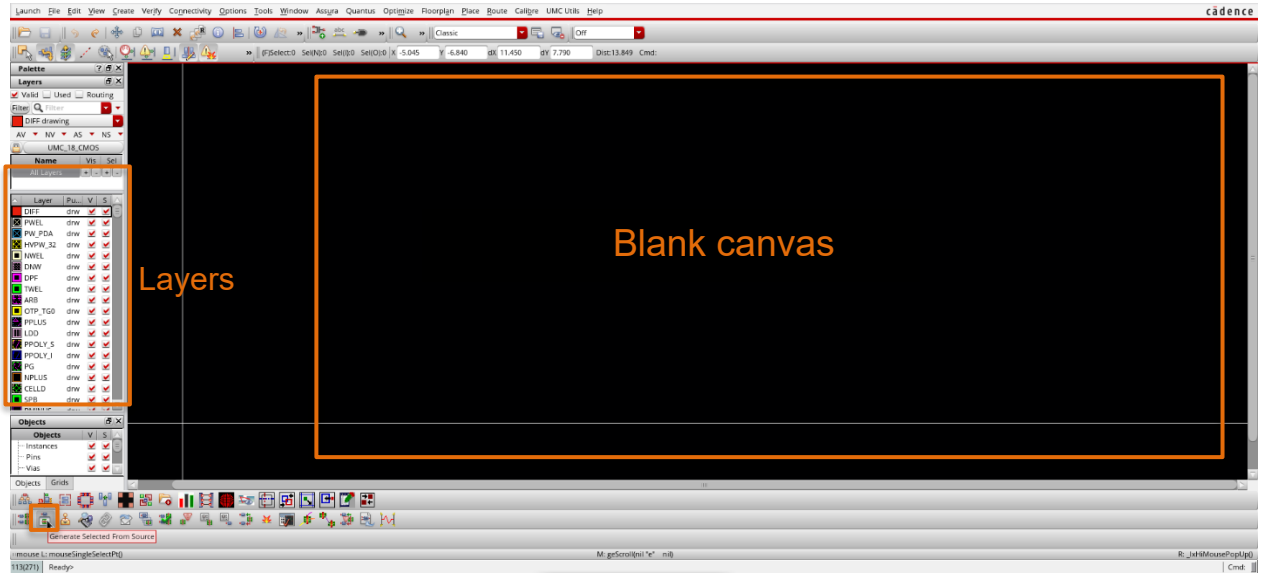
u	Edit > Undo	Undo actions one at a time
F3	N/A	Show additional properties for the selected command
f	Window > Fit All	Fit the entire layout into the layout window
k	Window > Create Ruler	Create a ruler to measure the distance between two points
z	Window > Zoom > In	Zoom in inside the layout window
e	Options > Display	To change the layout window display settings

The design kit we are working with is a 6 Metal process meaning we have a total of 6 metal layers for routing starting from ME1 (bottom most) to ME6 (top most). For this TP, we will limit ourselves to ME1, ME2 and ME3 layers since the design is very simple and higher metals are usually used for top-level routings.

Instantiating the MOSFETs

To add a MOS device into the layout window,

- Go to the schematic and click on the MOSFET that you would like to add to the layout.
- In the layout window, on the bottom left corner click on the "**Generate selected from Source**" button as shown below:



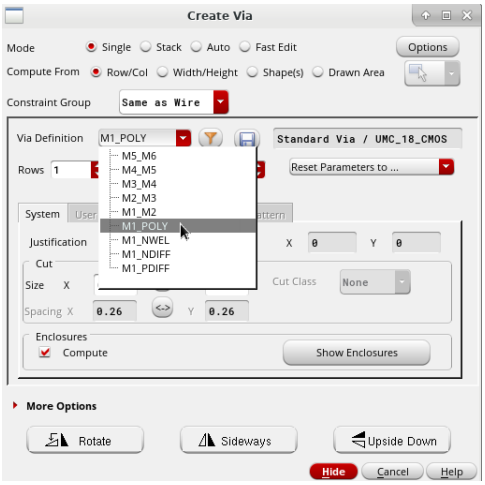
When you hover the mouse inside the layout window, the MOSFET will be available. Click on the point where you would like to place the MOSFET and the instantiation is complete.

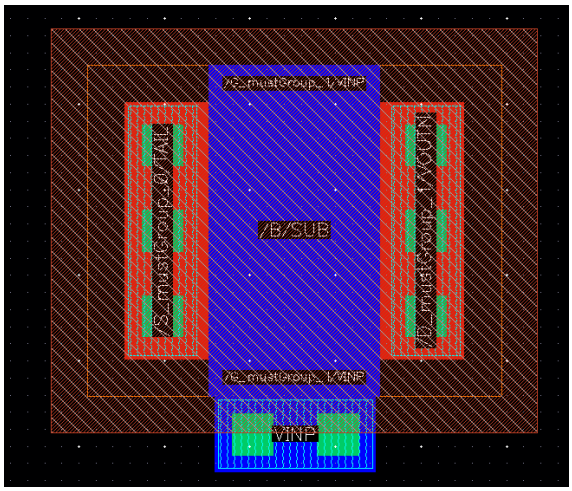
Adding Contacts to the MOSFETs

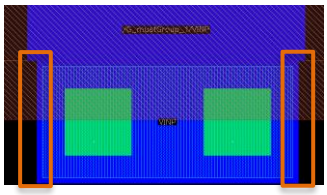
By default, the instantiated MOS will have Source and Drain connections available through ME1. However, we need to add a poly-to-metal contact in order to provide electrical contact to the Gate of the MOSFET. Press **"o"** and choose **M1_POLY** from the dropdown as shown below. You can change the number of rows or columns of contacts needed based on the dimension of the Poly

itself. Make sure that you use more than one row/column if applicable. Once chosen, place this contact on the Poly of the instantiated MOSFET.

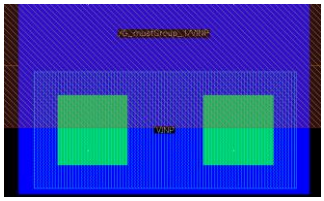
Once you add the contact, to avoid any design rule violation (refer to **DRC** in Page 6), we need to fill the poly in the open spaces next to the contact (refer to the image below).







Notice the open space on the left and right – which would cause a design rule violation



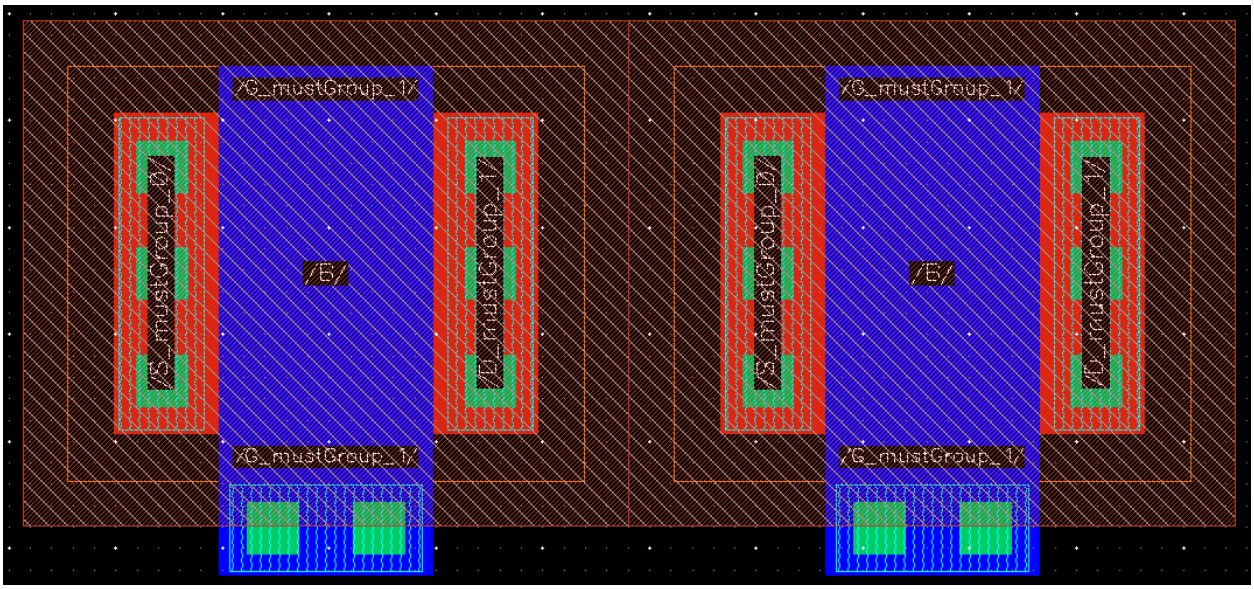
After filling the open space by drawing a poly rectangle

To draw a poly rectangle, click on PO1 in the layer palette (this selects the poly layer) and then press "**R**". Fill the poly rectangle so that you do not have any openings. Use the zoom shortcut "z" to be precise.

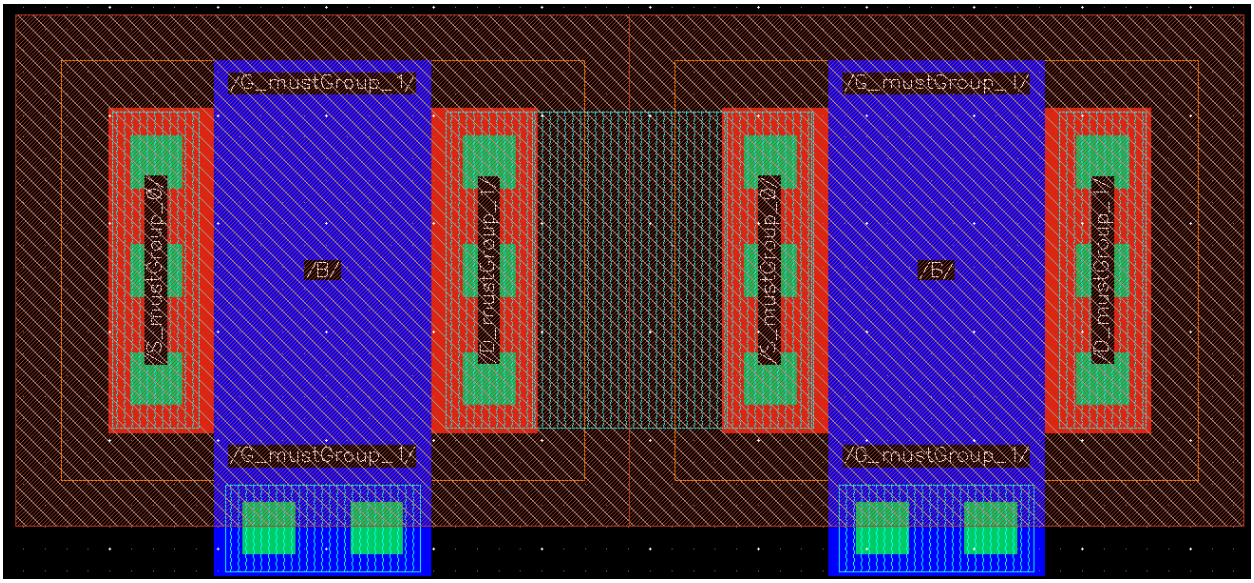
Similarly, instantiate the second MOSFET of the diff-pair and place them side by side. (Alternatively, you can select the whole structure that you have created and use the copy command to make a copy for the other diff-pair MOSFET).

Routing the NETs

Once the diff-pair MOSFETs are placed next to each other (as shown below), we need to make the connection between the source of the two MOSFETs (which is the net “TAIL” in the schematic). Note that you can choose any of the terminals as Source/Drain in the layout.

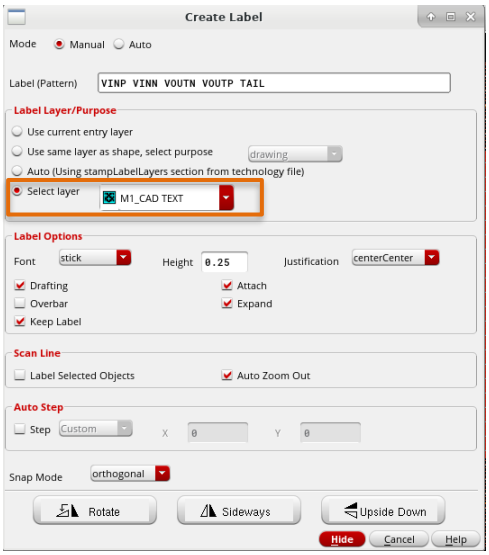


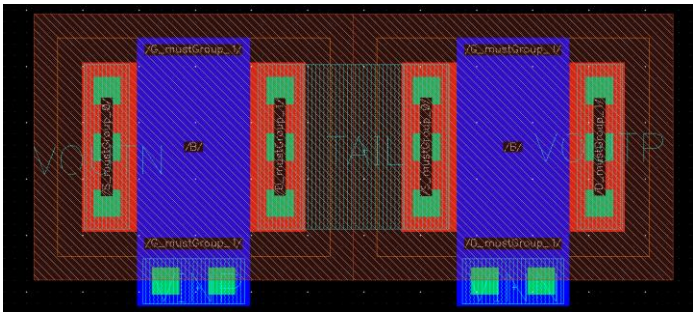
Draw a ME1 rectangle (by selecting the ME1 layer from the Layers Palette and then pressing “R”) as shown below between the two adjacent source terminals of the MOSFETs, to create the “TAIL” connection/terminal.



Creating Terminals on the Layout:

Finally, we need to place the terminal names matching the Pin names on the schematic for the tool to identify the nets. To do this, press “L” and based on the metal layer on which you want to place this, choose the suitable layer under the “Select Layer” option. For example, in our case, we would like to place the labels “VINP”, “VINN”, “VOUTN”, “VOUTP”, “TAIL” all in the ME1 layer since all the contacts are available in ME1. So, we choose the M1_CAD_TEXT option in the “Select Layer” and type the label names that we need. Refer to the image below to see the same.

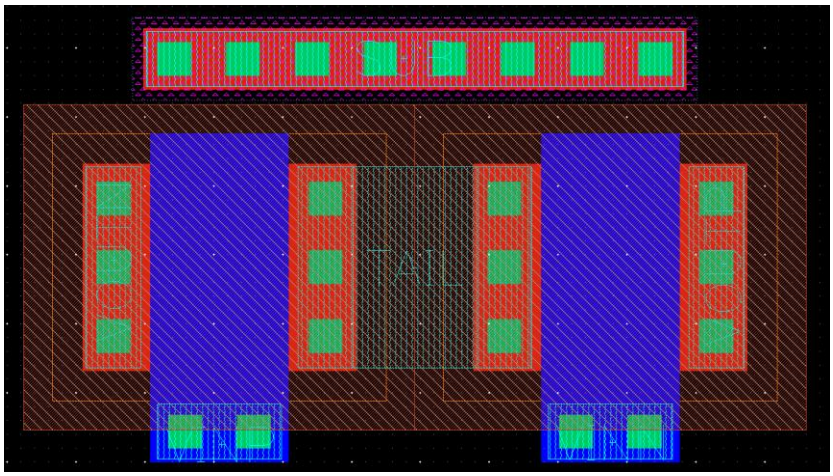




Press Hide and place the labels one by one (as they appear) on the corresponding positions as shown above. This will complete all the pins except for the substrate connection (“SUB” terminal in the schematic). This begs the question; how do we connect the substrate (P-sub for NMOS devices) electrically? Where is the substrate in the layout window?

Creating Substrate connection in the Layout:

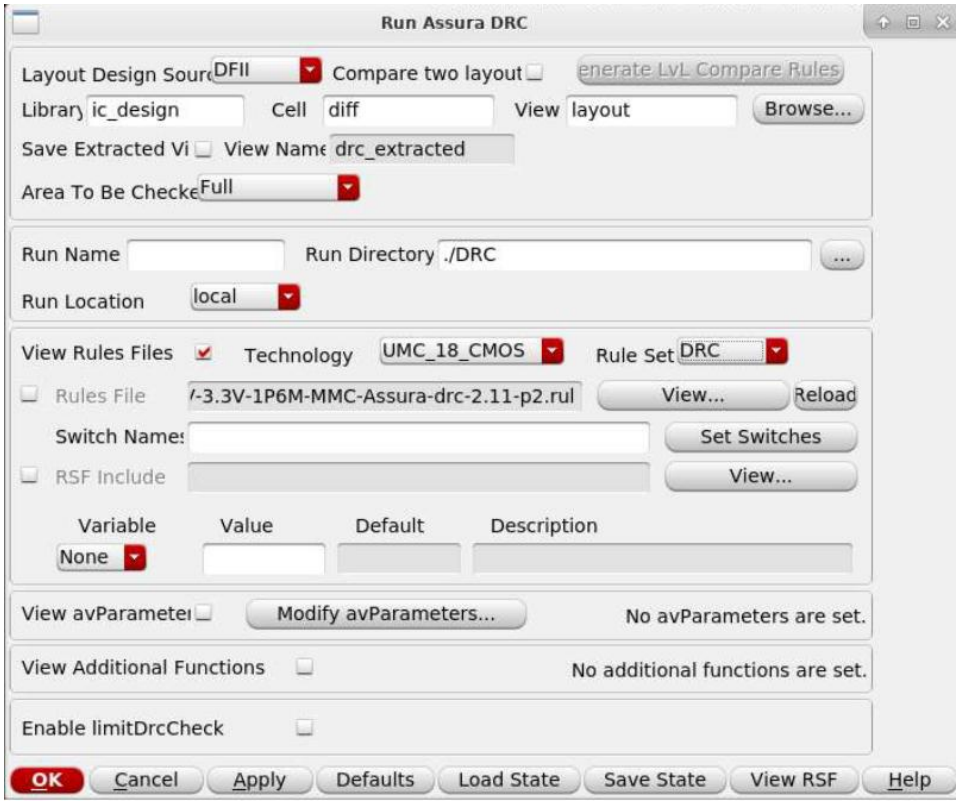
The most important thing to be noticed is that all the NMOS devices are placed on a common P-substrate. In the layout window, the black background corresponds to this P-substrate. You can place the P-substrate to metal contact anywhere on the black background. However, the farther away you place the contact from a MOSFET, the weaker the substrate connection near the MOSFET is going to be tied to that potential. We will place a common substrate connection close to the two NMOS diff-pair MOSFETS. Again, press **“o”** to bring up the contacts menu and choose **“M1_PDIFF”** and add as many columns as possible since the connections to the substrate need to offer very low resistance. Press hide and place the contact next to the MOSFETS, as shown below and label this as net “SUB”.



Running DRC and LVS:

Once we have finished our layout, we need to run two important checks:

DRC (Design-Rule-Check): These are the set of rules provided by the foundry which dictates rules like minimum spacing between two layers, minimum width between two layers, etc. based on the fabrication process. To run DRC, use **Assura > Run DRC**. This will open up a form as shown below. Adjust the settings to match the form shown below and click **OK**.



LVS (Layout-Vs-Schematic): The layout netlist obtained from the layout that we have drawn must be compared with the schematic to verify that the two are the same in terms of network and dimensions. To run DRC, use **Assura > Run LVS**. This will open up a form as shown below. Adjust the settings to match the form shown below and click **OK**.

We will briefly demonstrate these two checks in the TP session so that the students get a feel of what kind of errors are possible in the layout.

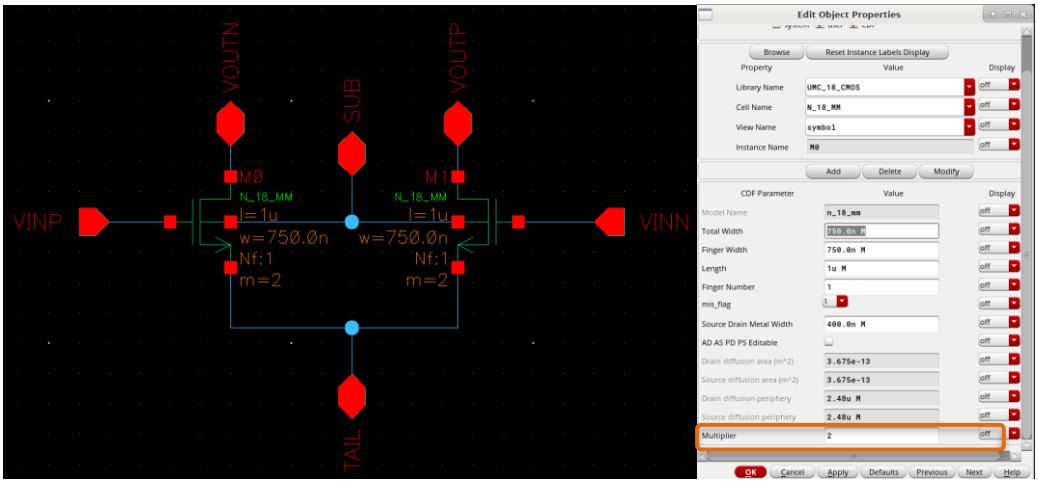
<u>Extracting the parasitics from the layout & comparing results with schematic:</u>

The final step is to extract the parasitic netlist from the layout and compare the simulation performance with the schematic results. To do this, we run what is called a **"PEX" (Parasitic Extraction)** to generate the parasitic netlist.

In the TP session, we will demonstrate the ac response of the diff-pair amplifier that we have implemented pre-layout (i.e., schematic) and post-layout to see the effects of parasitic. Normally, we would refine the layout iteratively and run PEX simulations until the required specifications are met post-layout. This will complete the design cycle.

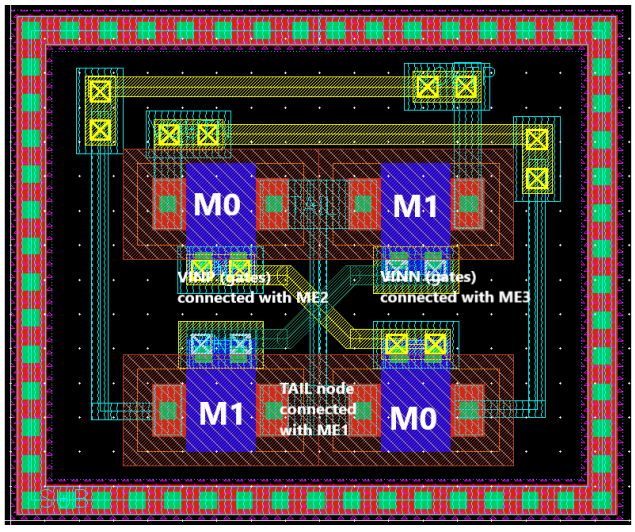
Better Layout techniques:

For better matching, the diff-pair can be laid out in a **common-centroid fashion (see references [1] and [2])**. To achieve this, we break the individual MOSFETs into two multiples as shown in the schematic below:



Notice that the widths are halved, and the “Multiplier” is doubled (m=2). Hence, in the layout, we now have a total of four MOSFETs that need to be laid out instead of two.

The figure below shows one such example of a common centroid layout of the diff-pair designed in this TP session. **Students are encouraged to try this layout implementation and approach the TAs in case of any difficulty.**

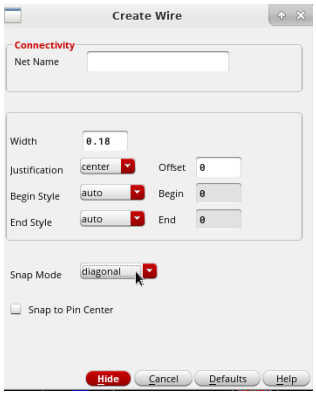


Guard ring/ substrate connection

References

[1] https://www.aspdac.com/aspdac2022/taoka/pdf/2B-3.pdf
[2] https://people.engr.tamu.edu/spalermo/ecen474/Lab2.pdf

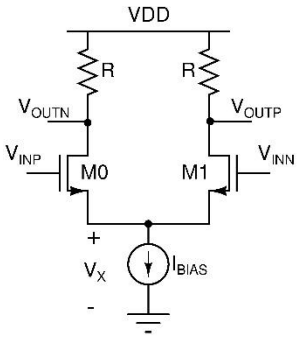
Note 1: The substrate connection is achieved with a **guard ring (which acts as a shield).** To create a guard ring, press **Shift+G** and choose **P-tap** to draw a guard ring on the **P-substrate**. Press Hide and then click on the corners/edges where you want it to be located.

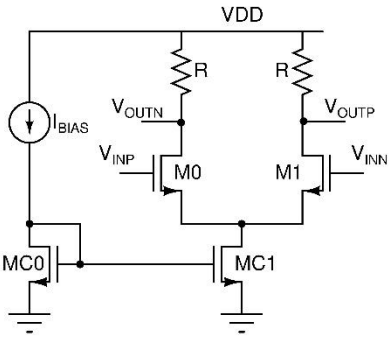


Note 2: To draw paths that are at an angle (like the gate connections above), press **"P"** for path and press **"F3"** and in the pop-up under the Snap mode, choose the **"diagonal"** option as shown above.

2. Current Mirror Design

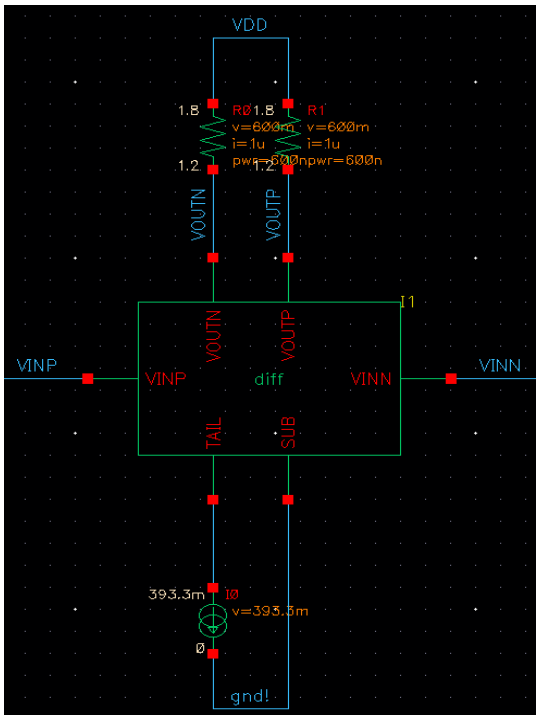
In TP-3, we designed the differential amplifier with an ideal tail current source. In this TP, we will design the tail current source using an NMOS transistor and the corresponding current mirror circuit for the differential amplifier. We will also investigate this current source's role in the common-mode gain of the differential amplifier.
Referring to the figure below, we need to introduce two extra NMOS MC0 and MC1 into our existing differential amplifier design.

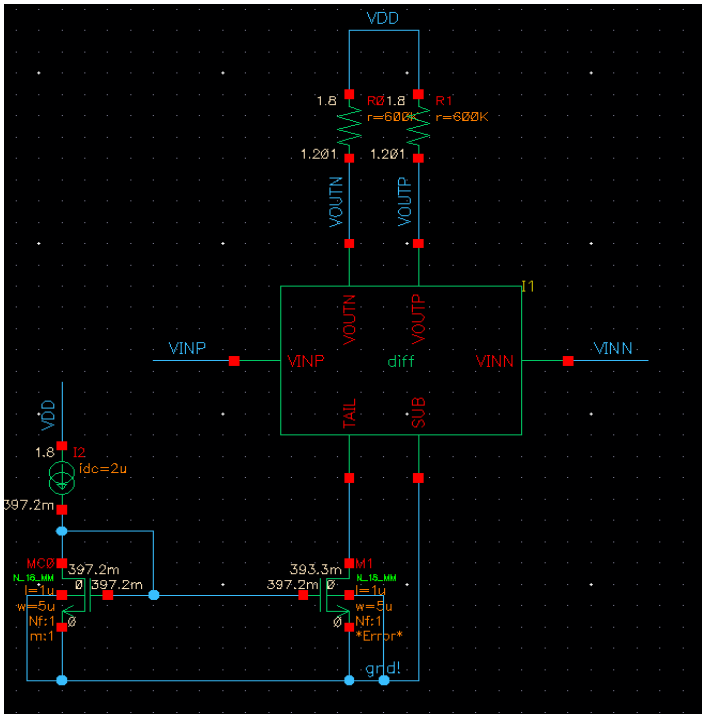




a) **<u>Sizing the current source MOSFETs for 1:1 mirror ratio</u>:**
We start with the very basic idea that an exact 1:1 mirroring of the current is possible between MC0 and MC1 only if the V_{GS} and V_{DS} of the two MOSFETs are exactly the same. Remember that with the same V_{GS}, it is still not guaranteed to have a matched mirroring with different V_{DS} (because of the non-zero λ).

In the schematic shown above, MC0 has the same V_{GS} and V_{DS} due to the diode connection. This implies that MC1 also needs to have the same V_{GS} and V_{DS} for exact matching. The V_{DS} required for the current source (MC1) to maintain the required current can be obtained from our previous circuit with the ideal current source (voltage V_X in the figure above). Re-run the dc simulation of your differential amplifier designed in TP-3 and notice that this voltage is around 393.3 mV (shown below).
Based on our previous argument, MC0 and MC1 will then have $V_{GS} = V_{DS}$ = 393.3 mV for a current of 2µA. We can now use the saturation current equation and solve for (W/L) for MC0 and MC1.





$$2\mu A = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(393.3m - V_{TH,N}\right)^2$$

For an NMOS with L = 1µm (note that the length of MC0 and MC1 must be the same for better V_{TH} matching and hence current matching), this will yield a W of 15µm. Plug these values into the schematic and iterate the width, W of the MOSFETs MC0 and MC1 until you obtain the VGS and VDS of these MOSFETs close to 393.3mV. You will arrive at the final (W/L) of **(5µ/1µ)** for MC0 and MC1. The final schematic with the annotated dc voltages and currents are shown above.

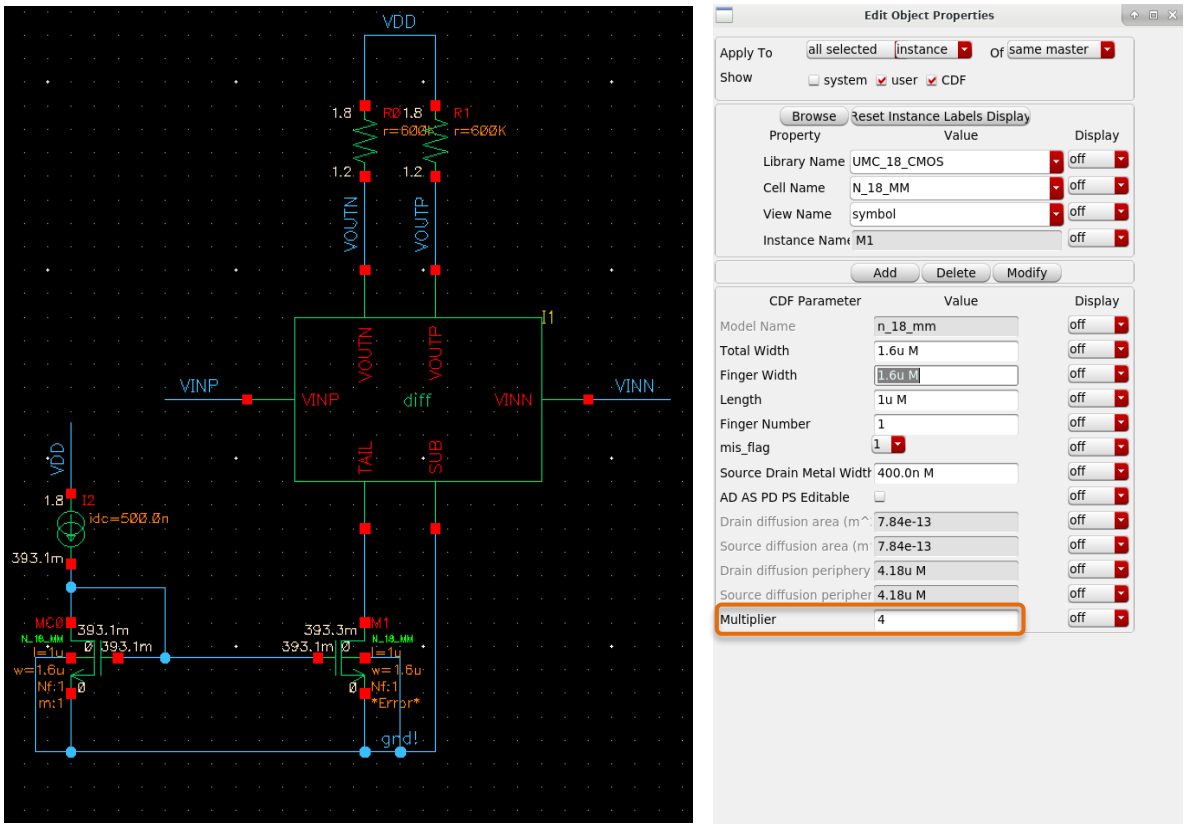
You can now **run the ac and transient simulations** for the differential amplifier and verify that the gain of the circuit has not changed.

b) <u>Sizing the current source MOSFETs for 1:4 mirror ratio</u>:

The bias circuit (MC0) is an additional circuit that adds to the power overhead and must be designed with a low current. Hence, the mirroring in practice will not be 1:1.

Let us consider the example where the bias current available is 500nA and we need to generate the 2µA current for the differential amplifier using a 1:4 current mirroring.

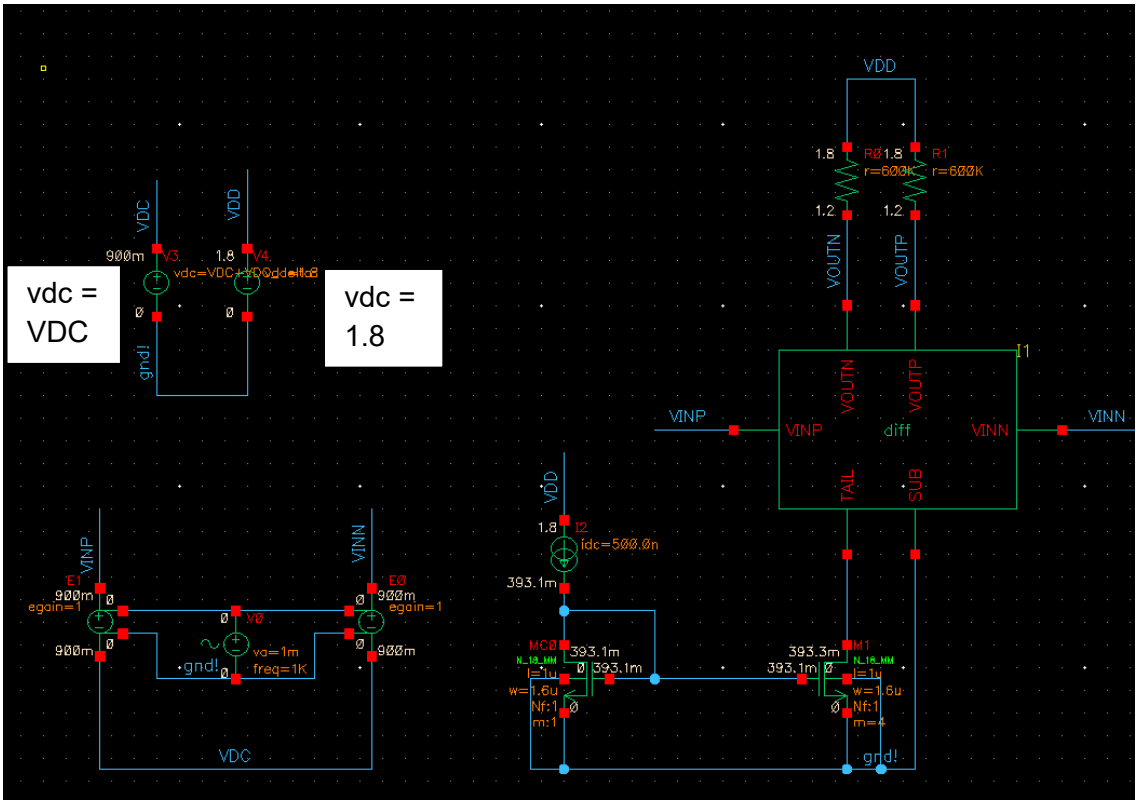
First, we will re-design the NMOS MC0 (with L = 1µm like before) for this new current of 500nA and the same operating point voltage of around 393.3mV. After iterating over the simulation, we will arrive at (W/L) of (1.6µ/1µ). M1 now will have to be sized 4 times that of MC0 for a 1:4 current mirroring. However, instead of simply multiplying the width of the NMOS MC1 by 4, use the "**Multiplier**" option in the MOSFET configuration. This implies that MC1 will be equivalent to having **4 multiple units of NMOS MC0** leading to **better matching** (since unit MOSFETs will have the same length and width).



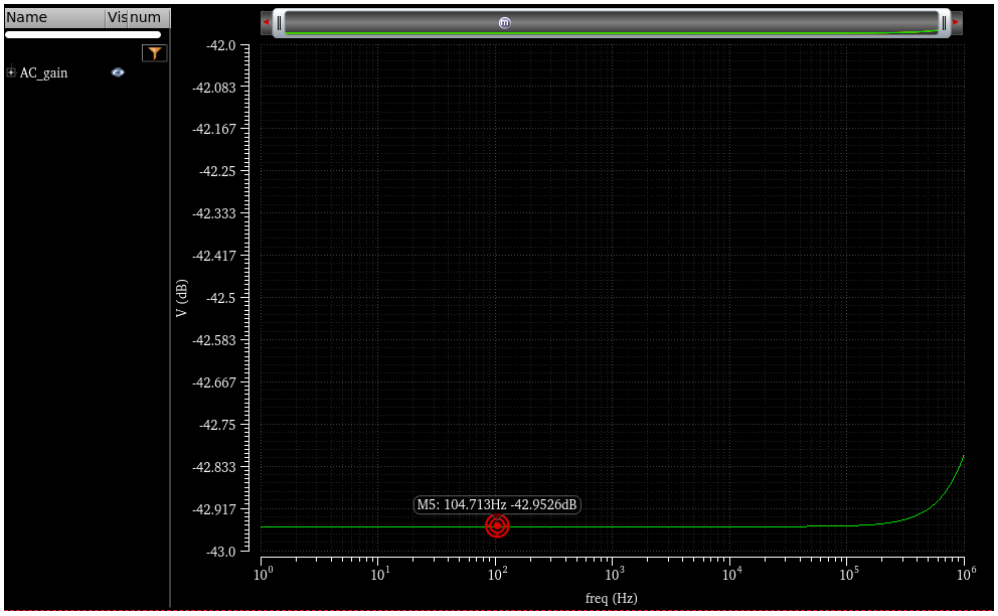
Verify the differential gain of the amplifier ($|A_{dm}|$ = 20 dB) using the same setup used in TP-3.

c) <u>Simulating the common-mode gain (Optional)</u>:

At this point remember the setup that was used to measure the differential gain of the amplifier with the help of two VCVS with gains of 0.5 and -0.5 to split the input differentially to the amplifier. The common-mode gain will be measured with the same setup but with the gain set to 1 for both VCVS (i.e., the same input is applied to both inputs of the differential amplifier). Refer to the schematic snapshot below and re-use the same ac simulation setup to plot the common-mode gain.



With the ac simulation, you will see a common-mode gain of -6.4kdB (meaning ~ 0 in absolute terms) which is not practical. This is due to the fact that the circuit is assumed to be precisely symmetrical in all aspects which again will not be the case practically. To get some idea of the common-mode gain with mismatches, let us introduce a 10% mismatch in the resistors (i.e., 60k mismatch between the left and right resistors). In the schematic, change the resistor value (from 600 KΩ) to 570 KΩ and 630 KΩ (left and right) to introduce this mismatch. Now, let us simulate the common-mode gain with this 10% resistor mismatch.



The simulated common-mode gain is approximately -43 dB. We have already simulated the differential gain of 20 dB. This leads to a CMRR of 63 dB ($|A_{dm}|/|A_{cm}|$ in linear scale will be a difference in log scale).

d) Effect of current source MOS length on the CMRR **(Optional)**:

Having designed the current mirror circuit with an NMOS length of 1µm, we will leave it as an exercise for the students to **redesign the current mirror circuit (for the 1:4 ratio) for two different NMOS lengths of 2µm and 4µm**. Tabulate the final NMOS sizes below for the three different lengths:

MC0			**MC1**		
L = 1u	W = 1.6u	m = 1	L = 1u	W = 1.6u	m = 4
L = 2u	W =	m = 1	L = 2u	W =	m = 4
L = 4u	W =	m = 1	L = 4u	W =	m = 4

Hint: The aspect ratios do not scale linearly with length since the MOS V_{TH} changes with length as well.

Simulate the common-mode gain for these three cases and plot the gain plots in the ac simulation.

Notice that the common-mode gain performance (and hence the CMRR) improves with an increasing channel length of the tail current source (in this example, 6 dB improvement for every doubling of the channel length). It is very important that the tail current source be designed with a large resistance (as the resistance approaches infinity, we are closer to an ideal current source) for good CMRR performance. In practical designs, cascode tail current and mirror circuits are used to improve the CMRR performance.