EE-320 ANALOG IC DESIGN TP-2025/2026
PRACTICAL EXERCISE SESSION No. 3

Note: For students connecting virtually, the details of the Zoom Meeting for the TP sessions are given below (The same link, meeting ID, and passcode are valid for all 4 TP sessions)

Meeting link:
https://epfl.zoom.us/j/63888844351?pwd=dbKCKx75b0Y9tfd7sqfjJ0WXUhjRxX.1
Meeting ID: 638 8884 4351
Passcode: 354172

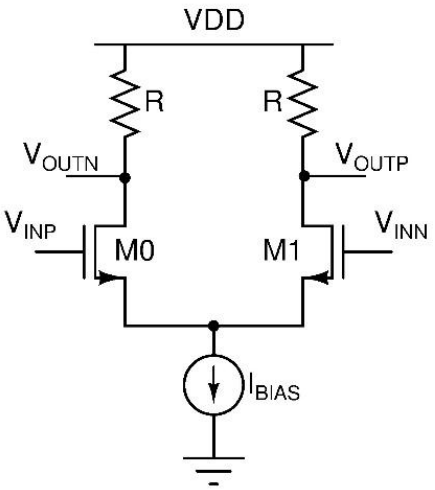
In this TP, we will design a Differential Amplifier. We assume that you are now well versed in creating the schematic and simulating using Cadence Virtuoso, based on TP-1 and TP-2. (You can check TP-1 and TP-2 documents in case you need details.)

Note: For hand calculations, use the following values extracted from the design kit:
$\mu_n C_{ox}$ = 278µA/V², $V_{TH,N}$ = 0.4V, $\mu_p C_{ox}$ = 61µA/V², $|V_{TH,P}|$ = 0.54V, VDD = 1.8V.

1. Design of NMOS Input Differential Amplifier

We will go through the methodology to design an NMOS-Input Differential Amplifier with resistive load for the following specifications:

$V_{IN,CM}$ = 0.9V, $V_{OUT,CM}$ = 1.2V, I_{BIAS} = 2µA,
Differential voltage gain $|A_v| \geq 10$.



Hand calculations:

a) We start with the first design iteration as follows:

$$I_D . R = V_{DD} - V_{OUT,CM}$$

$$R = \frac{1.8 - 1.2}{1u} = 600K\Omega$$

From half-circuit analysis, gain $|A_v| = g_m . R$

$$g_m . R > 10$$

$$g_m > 16\mu S$$

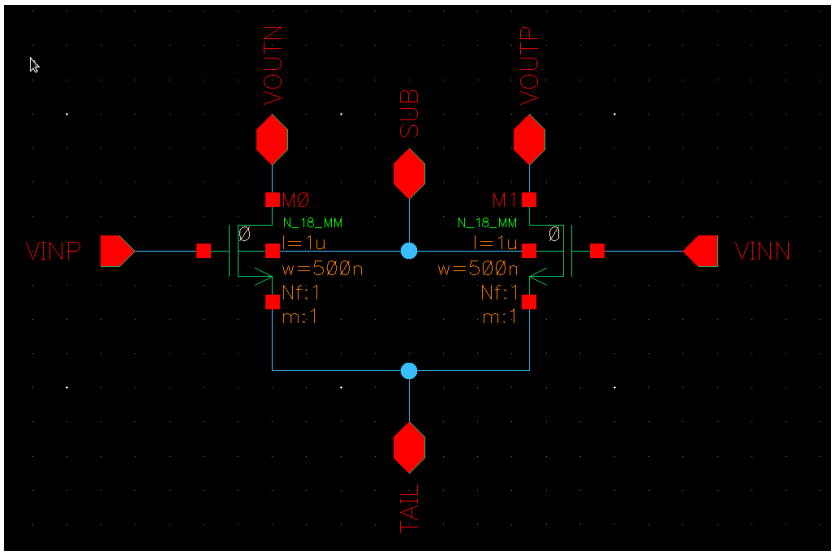
$g_m = \sqrt{2I_D \mu C_{ox} \left(\frac{W}{L}\right)}$, therefore (W/L) > 0.47.

We start with L = 1µm and W = 0.5µm and iterate to obtain the required gain.

Building the schematic:

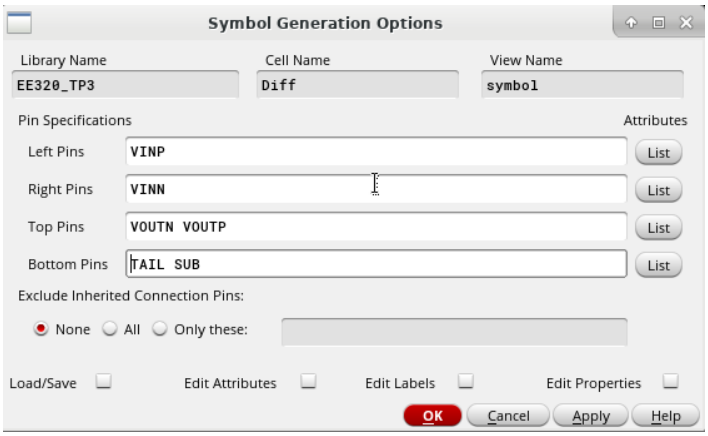
b) In the previous TPs, we created test benches that contained all the components within the same canvas. In this session, we will create a **hierarchy** where our circuit is a standalone component that can be instantiated within other schematics. Having hierarchies in your design facilitates the re-use of certain blocks (without having to connect them up again), improves the readability of your schematics, and allows you to separate your "design" from your "testbench". Creating a component is also necessary to draw its physical layout, as ideal test bench elements like voltage or current sources do not belong to the circuit itself.

Create the differential pair (diff pair) schematic as shown below, named "diff". Here, we use **pins** (red elements in the schematic) instead of nets to define the connection points/terminals from a higher level to the nodes in this circuit. Use the keyboard shortcut **"P"** for placing these pins. Make sure that you use the correct direction (input, output, inputoutput) for each connection, as shown in the figure below.

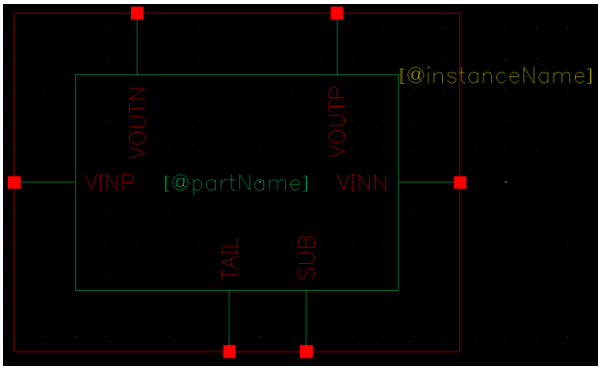


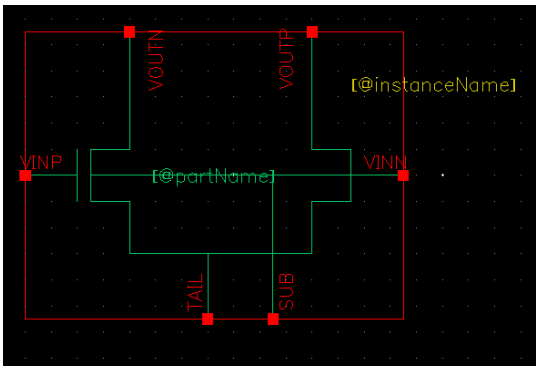
Note: To **rotate or flip** a component in the schematic, **use the rotate button** on the toolbar  . Alternatively, you can also use the keyboard shortcut "**R**" for rotate and "**Shift + R**" for vertically flipping components.

The next step is to create a symbol for the diff pair. Click **Create > Cellview > From cellview and click OK**. Arrange the list of pins as shown below to have the inputs on the left and right sides of the symbol, outputs on the top, and inputoutput pins on the bottom, as shown in the figure below.

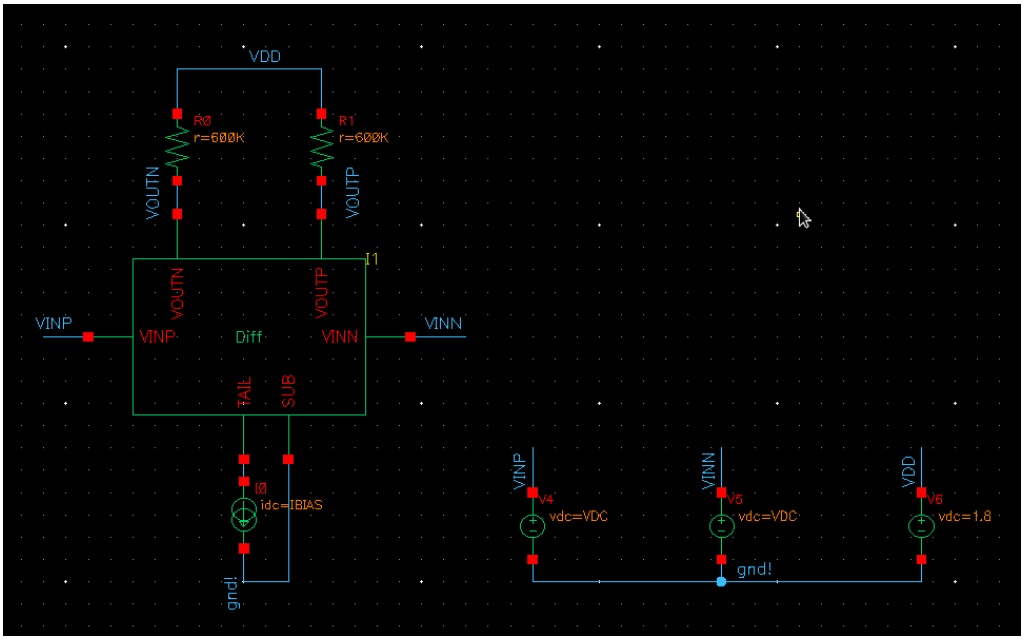


After clicking OK you will see that the symbol is automatically generated. You can edit the symbol using the toolbar to make it look more representative of what is inside (as shown below on the right), but for this TP, you can skip this step. You can close the symbol window when you are done.



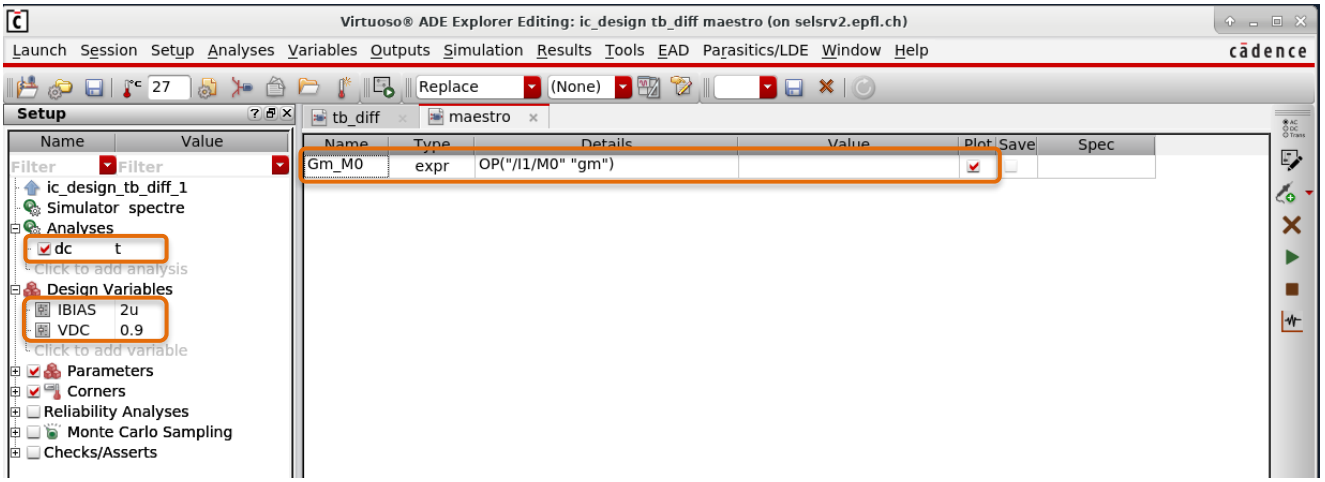


Create the testbench below for the diff pair, named “tb_diff”. **Place your component “diff” by browsing its symbol view in your own library.** Make sure that the instance name of this component is “I1”. After you place all the components, check and save. To change the transistor parameters, you can descend into your component “diff” by pressing **“Shift+E”** on your keyboard and then clicking on the component. To ascend back to the test bench level press **“Ctrl+E”.**



Setting up ADE-Explorer and performing DC simulation:

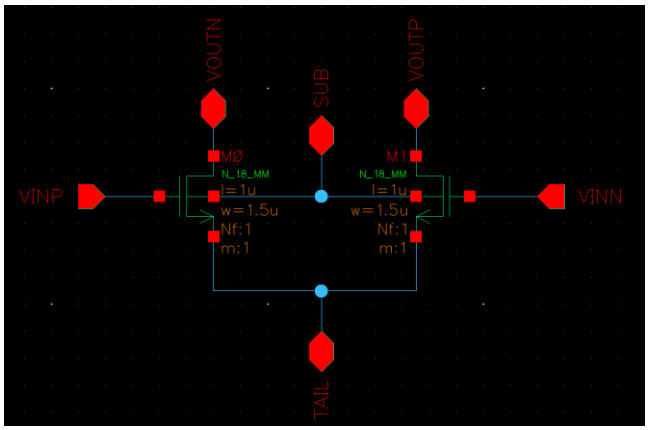
a) Create a new ADE-Explorer simulation setup with DC analysis and save the required DC operating points in ADE-Explorer. Set the IBIAS value to 2µA and VDC to 0.9V. Make sure that the transistor instance name is “M0” and “M1” inside the “diff” instance and ensure that the instance name is “I1”. Save the operating point g_m (using OP(“/I1/M0” “gm”)). The ADE-Explorer window will look as shown below.

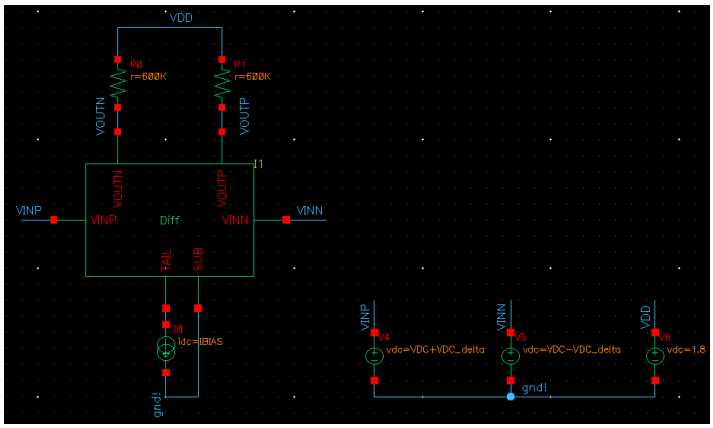


b) Run the DC operating point simulation and note the g_m and the output dc voltage. Adjust the width of the MOSFETs “M0” and “M1” until you hit the required gm (based on hand calculations). In this example, the final value of (W/L) for the required gm is (1.5µm/1µm). You can iterate and check that you will arrive at this final value of (W/L) to meet the required gm and hence the gain.

Setting up **ADE-Explorer** and performing DC sweeps:

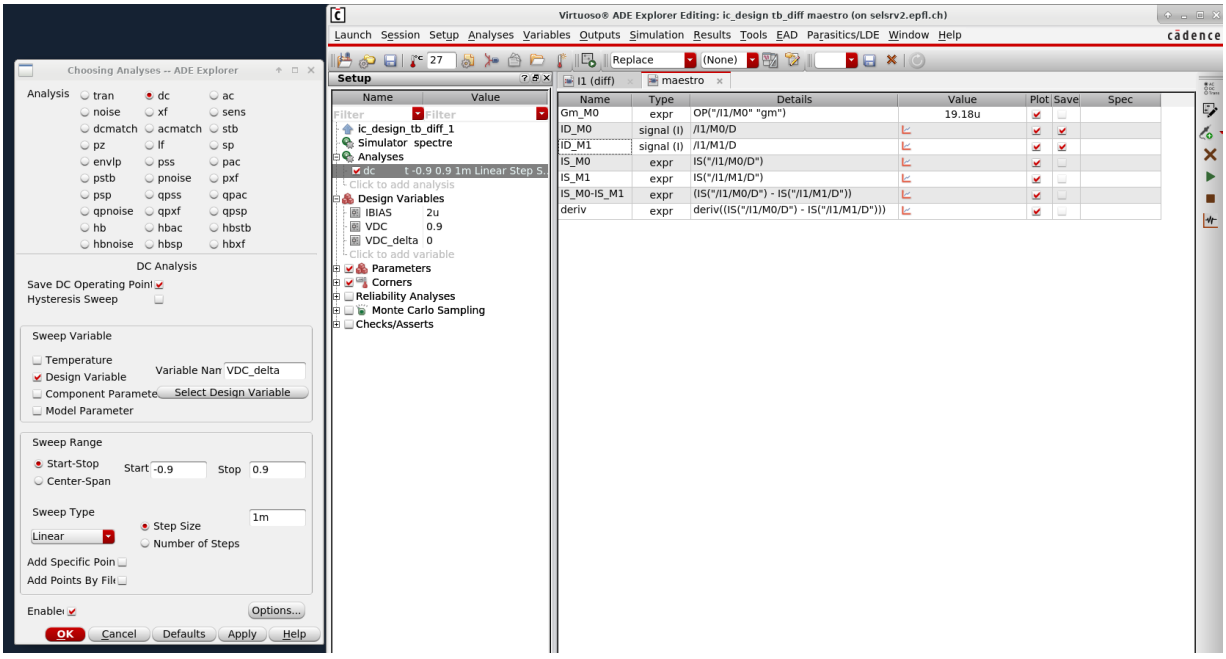
Now that we have met the required operating point conditions, we will verify the usable range of the diff pair. Create a DC sweep analysis of the parameter “VDC_delta” as shown below:



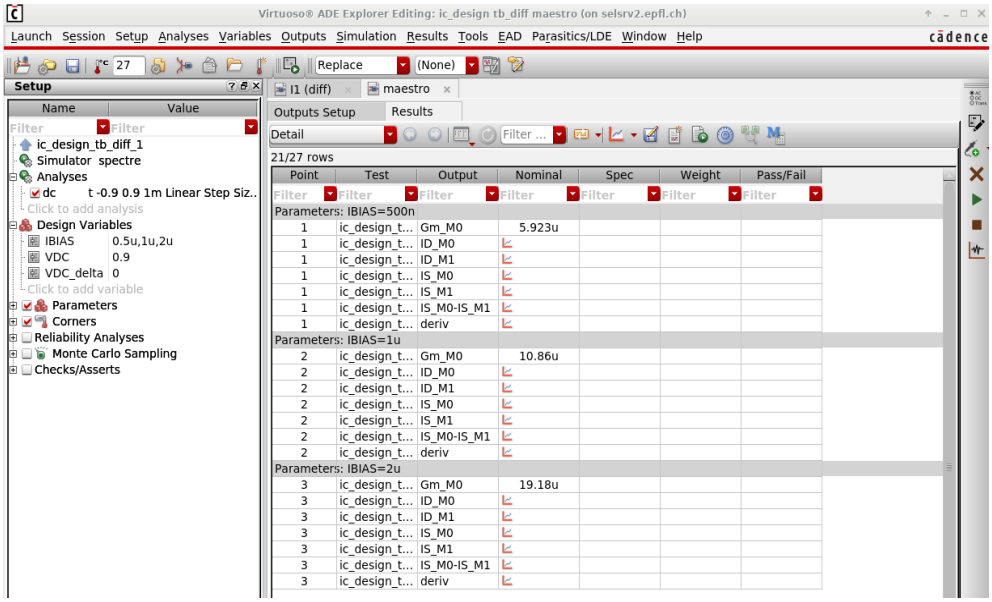


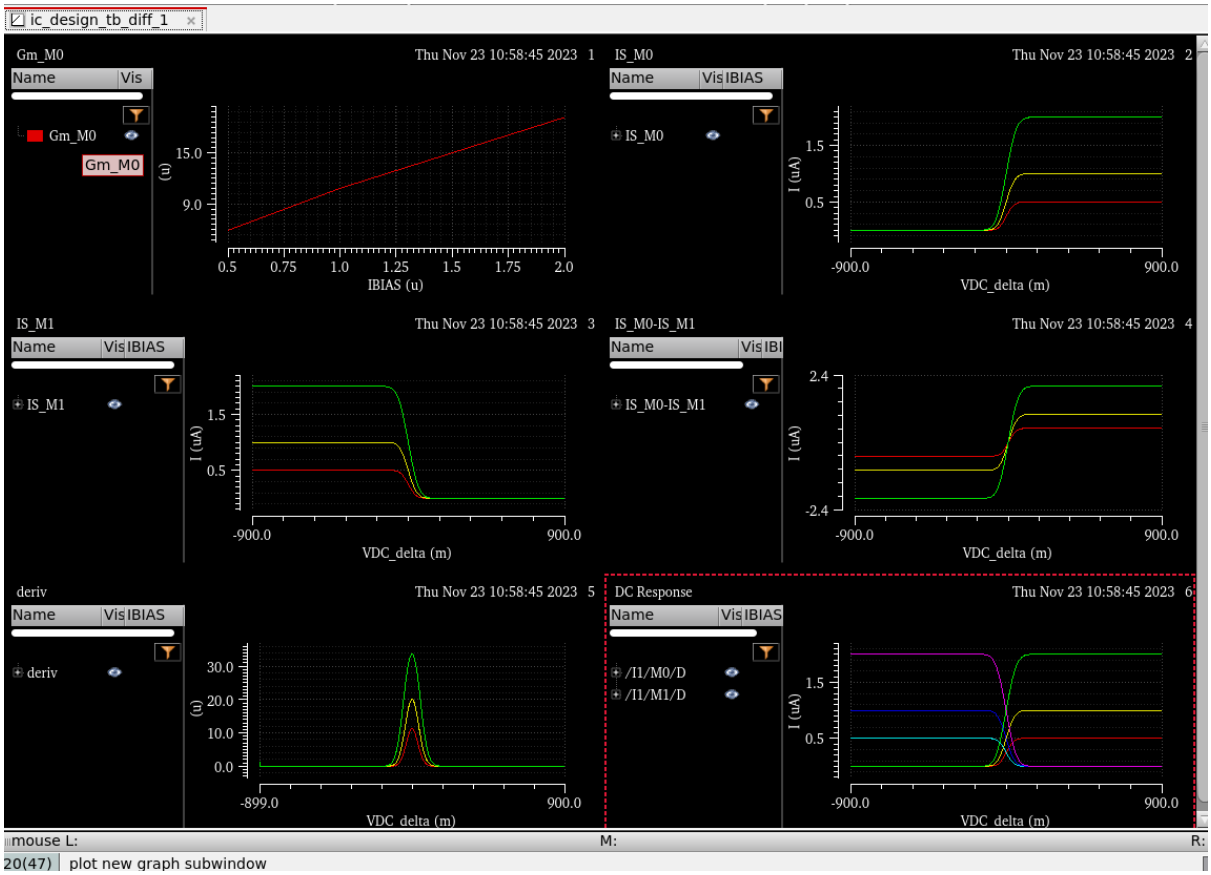
In the ADE window, define the following six outputs:

1. /I1/M0/D
2. /I1/M1/D
3. IS(“/I1/M0/D”)
4. IS(“/I1/M1/D”)
5. (IS(“/I1/M0/D”)- IS(“/I1/M1/D”))
6. deriv(IS(“/I1/M0/D”) - IS(“/I1/M1/D”))



Run the dc sweep simulation for different bias currents of 500nA, 1µA and 2µA. Identify the useful range of the amplifier from the difference of drain currents (expression 3 above). Notice that the derivative of this plot (expression 4 above) reminds us that the gain is considered linear only for a small signal around the operating point bias conditions and not for the entire useful range.

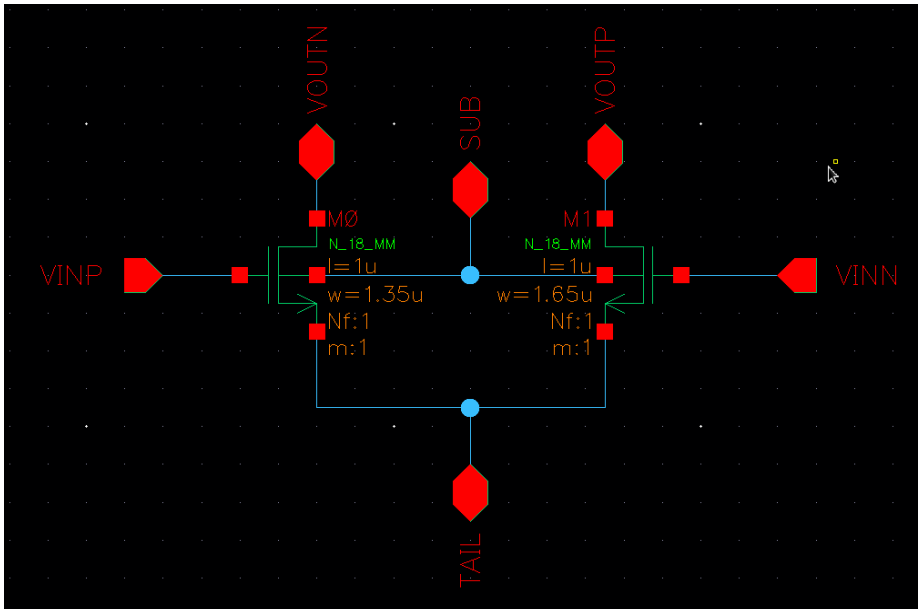


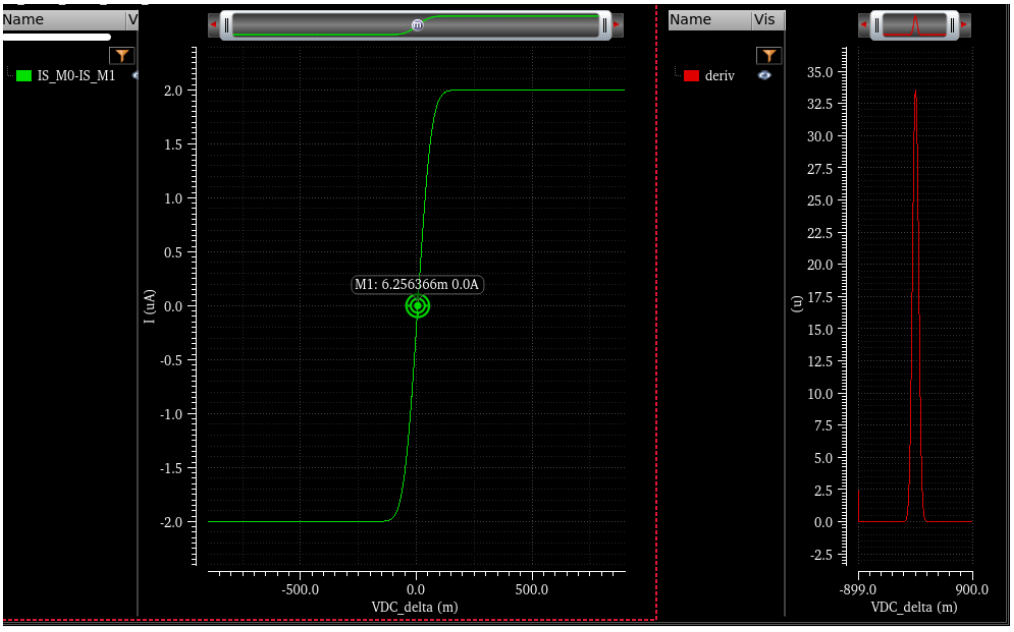


Effect of mismatch in the diff-pair:

We will now evaluate the effect of mismatch in the diff-pair using dc-sweeps. During the design, we sized the input NMOS differential pair to be identical in geometry with the assumption that their parameters (mobility, oxide capacitance, threshold voltage etc.) are identical. In reality, post silicon fabrication, the geometry of these devices will never be identical. The parameters will be different due to systematic and random influences during the fabrication process. Therefore, there will always be a certain degree of asymmetry associated with the fabricated differential pairs.

To simulate the effect of this mismatch, consider a scenario where the NMOS width deviates by ±10% (i.e., M0 width by -10% and M1 width by +10%), as shown in the schematic below. For simplicity, assume the length of the MOS remains unchanged.

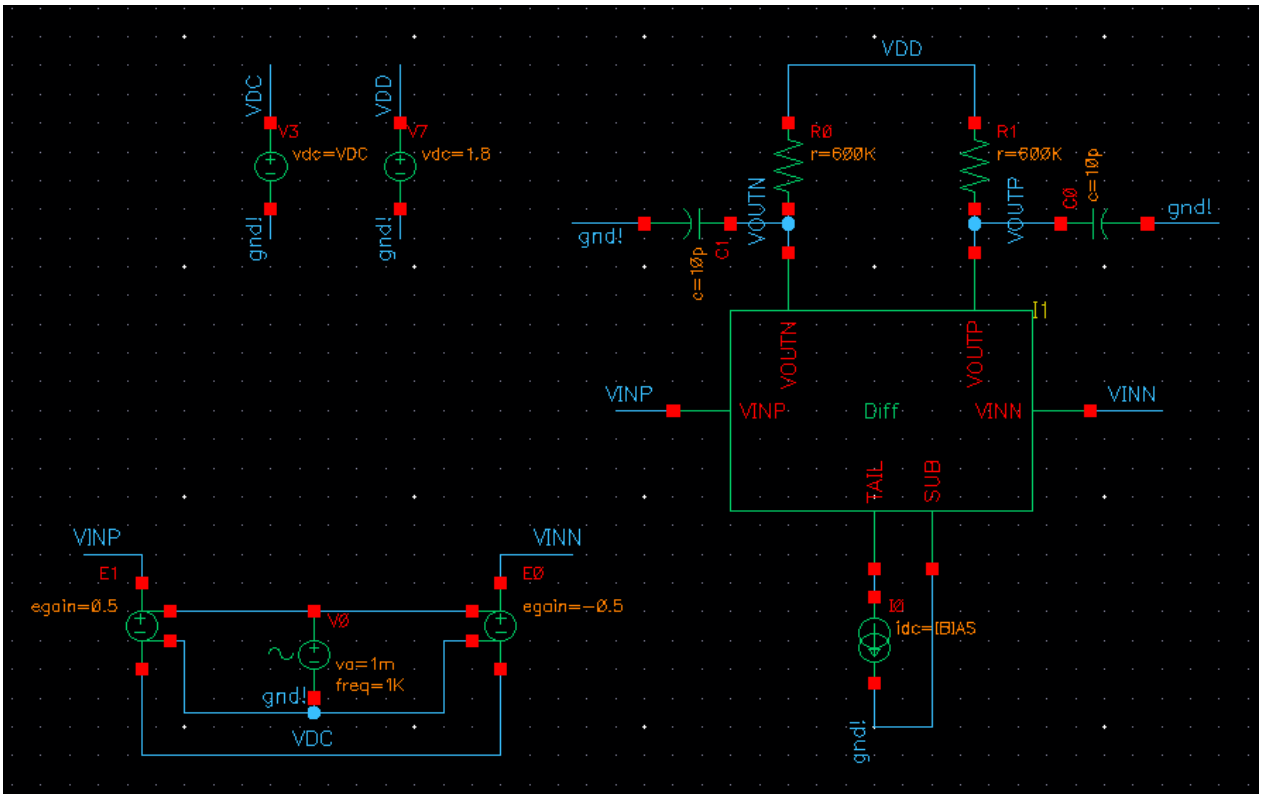




Simulate the circuit with these new MOS width dimensions with the bias current of 2μA (design specification). Notice that the point where the differential current crosses 0A does not correspond to a 0V input difference. This deviation of the zero-crossing point from the ideal case due to mismatch is termed **"input-referred offset".** In the plot above, the input-referred offset is 6.25 mV.

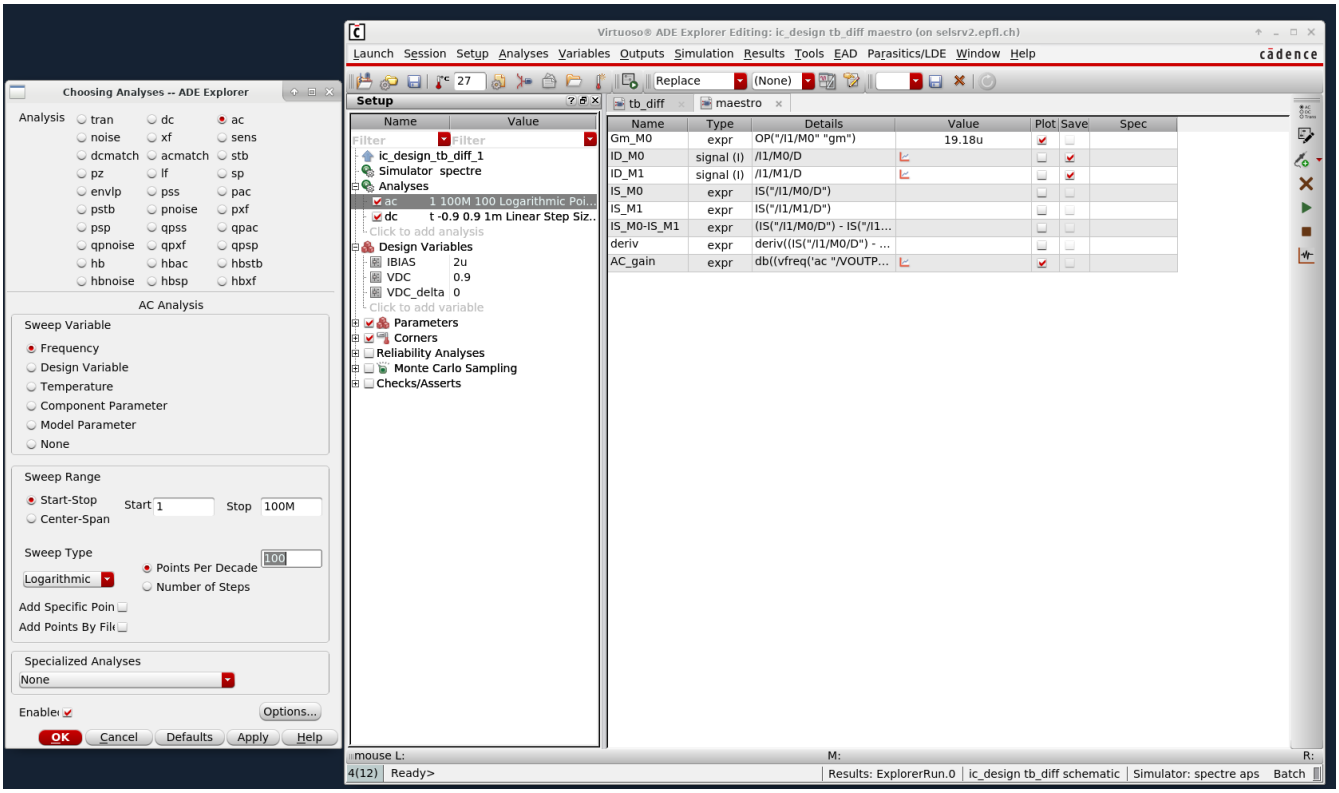
Performing AC small-signal simulation:

Revert the width of the NMOS input pair back to 1.5μ to perform the ac analysis without any mismatch. Note that as against a single-ended input circuit, the differential input circuit needs a different setup to run the ac analysis as shown below. To split the input ac signal differentially between the two inputs we use two ideal voltage-controlled-voltage-source (VCVS) from the analogLib and set the gain to 0.5 and -0.5, respectively. The ac signal is then applied as inputs to these two VCVS with the AC magnitude set to 1.



Note that we have added two capacitors of 10 pF on both output nodes. This capacitor will act as the load capacitor (mimicking the input capacitance of the next stage that the differential pair drives). We will get back to this capacitance later in the tutorial.

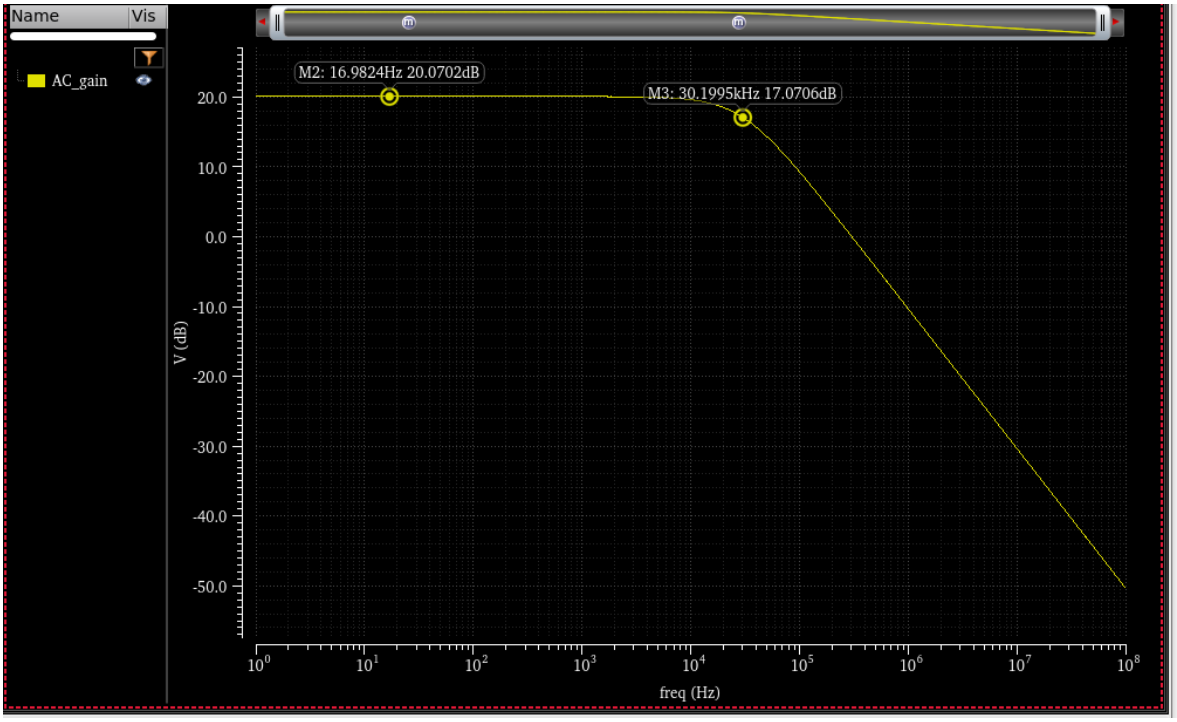
Add a new analysis in ADE-Explorer and choose “ac”. The ac simulation setup is shown below:



Run the ac simulation using ADE- Explorer and verify the gain obtained.
Add the following expression to the ADE window to plot the ac response as a function of frequency (ensure that the output nets are labeled VOUTP and VOUTN in the schematic).

db((vfreq('ac "/VOUTP") - vfreq('ac "/VOUTN")))

The AC response plot will look like below.



Notice that the dc gain is around 20 dB (i.e., 10 in linear scale), which is our required specification. Also, the -3dB frequency (i.e., the frequency when the gain drops to 17 dB) is around 30 kHz as seen from the plot.

Analyzing the frequency response (Optional):

To analyze this 3-dB frequency analytically we need to use the small-signal model and evaluate the frequency response of the circuit using this linear model. While this is not covered in the lectures, we will briefly present the idea behind this here. Based on the half-circuit of the differential pair, at the output, we will have the load resistance R, the load capacitance C, and the small-signal resistance r_o of the NMOS. If we ignore the small-signal resistance r_o (as $r_o >> R$), the effective time constant at the output node will be RC (R being the load resistor and C being the load capacitor).

In our example, R is 600 KΩ and C is 10 pF. This RC will present a pole at the output node whose frequency is given by, $f_{pole} = f_{-3dB} = 1/(2\pi RC) = 26.5$ kHz. Compare this with the 3dB frequency that we obtained in our simulation (around 30 kHz). If you consider the finite r_o of the NMOS, the 3dB frequency will be roughly around 30 kHz.

Change the load capacitance from 10 pF to 1uF and verify that the simulated and the hand-calculated 3dB frequencies match.