EE-320 ANALOG IC DESIGN TP-2025/2026
PRACTICAL EXERCISE SESSION No. 2

Note: For students connecting virtually, the details of the Zoom Meeting for the TP sessions are given below (The same link, meeting ID, and passcode are valid for all 4 TP sessions)

Meeting link:
https://epfl.zoom.us/j/63888844351?pwd=dbKCKx75b0Y9tfd7sqfjJ0WXUhjRxX.1
Meeting ID: 638 8884 4351
Passcode: 354172

In this TP, we will design and simulate two variants of the common-source amplifier and a source-follower circuit. We assume that you are now well versed with creating the schematic and simulating using Cadence Virtuoso, based on TP-1 and hence we do not explicitly show all the steps. Please refer to TP-1 in case you need any additional details regarding the same.

⚠ Do not repeat the steps to setup the environment again. After connecting to the jed servers and executing *"/work/fvlsi/run_edadk"*, go to your CDS_VISO folder that was created in TP1 and start your design in Virtuoso.

Methodology:

We will follow the steps described below in designing and simulating the circuits for the given specifications:

1. To meet the specifications, use hand calculations based on the design equations provided in the class. Arrive at the MOS aspect ratios and any other passive component values.
2. Create the schematic in Virtuoso based on the hand-calculated values.
3. Run the dc-operating point simulation and verify the dc-operating points. Iterate the design to meet the desired operating point.

   ⚠ Do not proceed further until the DC operating point conditions are met.

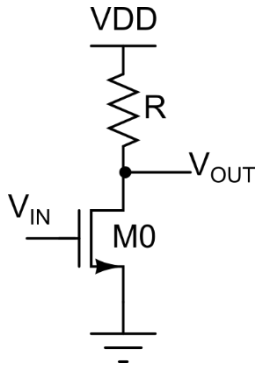
4. Run the small-signal ac analysis on Cadence Virtuoso and verify the results with your hand calculations. Iterate until the specifications are met.
5. Finally, run the transient simulation for the designed circuit and verify the waveforms.

Note: For hand calculations, use the following values extracted from the design kit:

$\mu_n C_{ox}$ = 278µA/V^2, $V_{TH,N}$ = 0.4V, $\mu_p C_{ox}$ = 61µA/V^2, $|V_{TH,P}|$ = 0.54V, V_{DD} = 1.8V.

1. Common-Source Amplifier with a Resistive Load

We will go through the methodology to design a common-source amplifier with resistive load for the following specifications:



V_{DD} = 1.8V, $V_{IN,\,DC}$ = 0.9V, $V_{OUT,\,DC}$ = 0.9V, I_D = 10µA, Voltage gain $|A_v| \approx 3$.

Hand calculations:

a) We need to figure out the values for the resistor R and the (W, L) for M0 to support the 10uA current.

We start with the first design iteration as follows:

$$I_D . R = V_{DD} - V_{OUT,DC}$$

$$R = \frac{1.8 - 0.9}{10u} = 90K\Omega$$

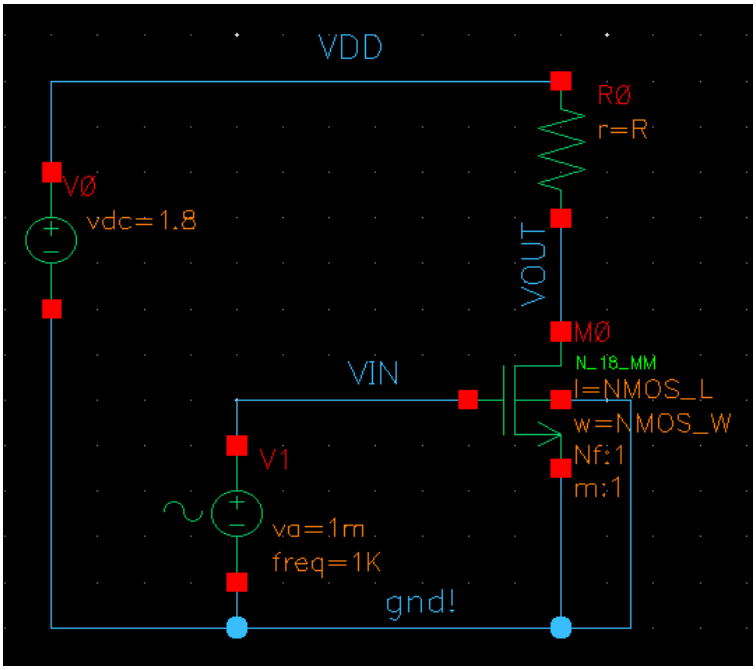
$$I_D = \frac{1}{2} . \mu_n C_{ox} \left(\frac{W}{L}\right) \left(V_{IN,DC} - V_{TH,N}\right)^2$$

$$\frac{W}{L} = 0.288$$

⇨ If we select minimum W = 240nm, then L ≈ 840nm.

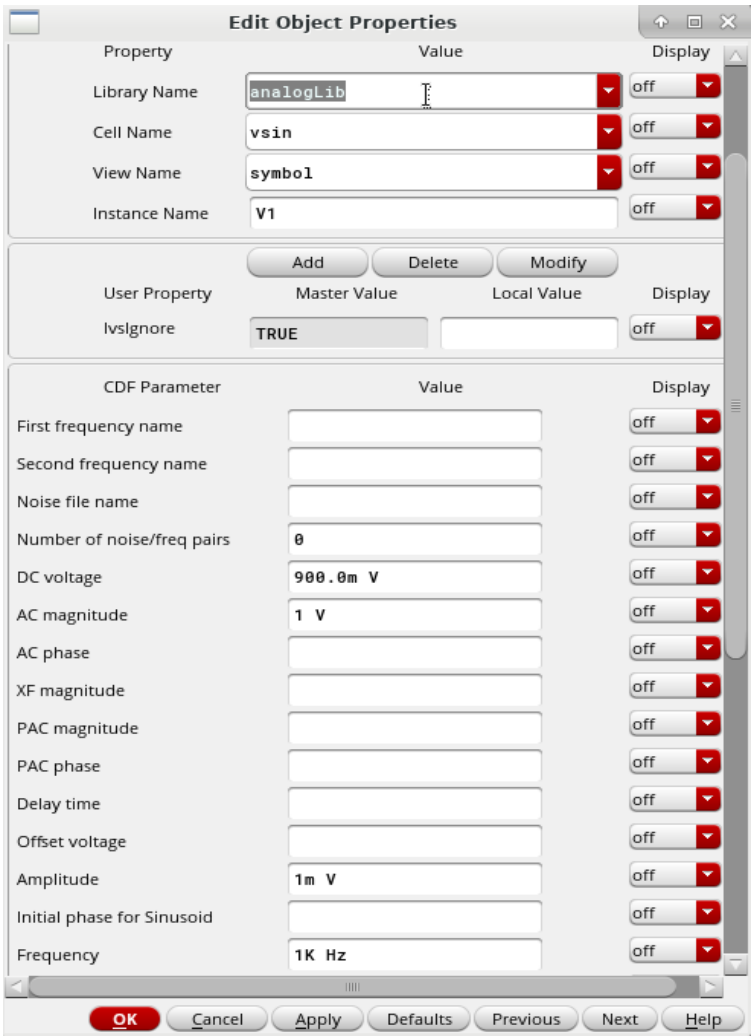
Building the schematic:

b) With this initial design, translate the design to Virtuoso and build the schematic as shown below. In Virtuoso, create a schematic using components from the UMC_18_CMOS library and the analogLib libraries. Define the parameters “NMOS_L”, “NMOS_W”, and “R” in the schematic. Also, configure the input source V1 as shown in the figure below. The **Amplitude, Frequency,** and **AC Magnitude** fields do not matter for the DC operating point simulation.



Handy Shortcuts Recap:

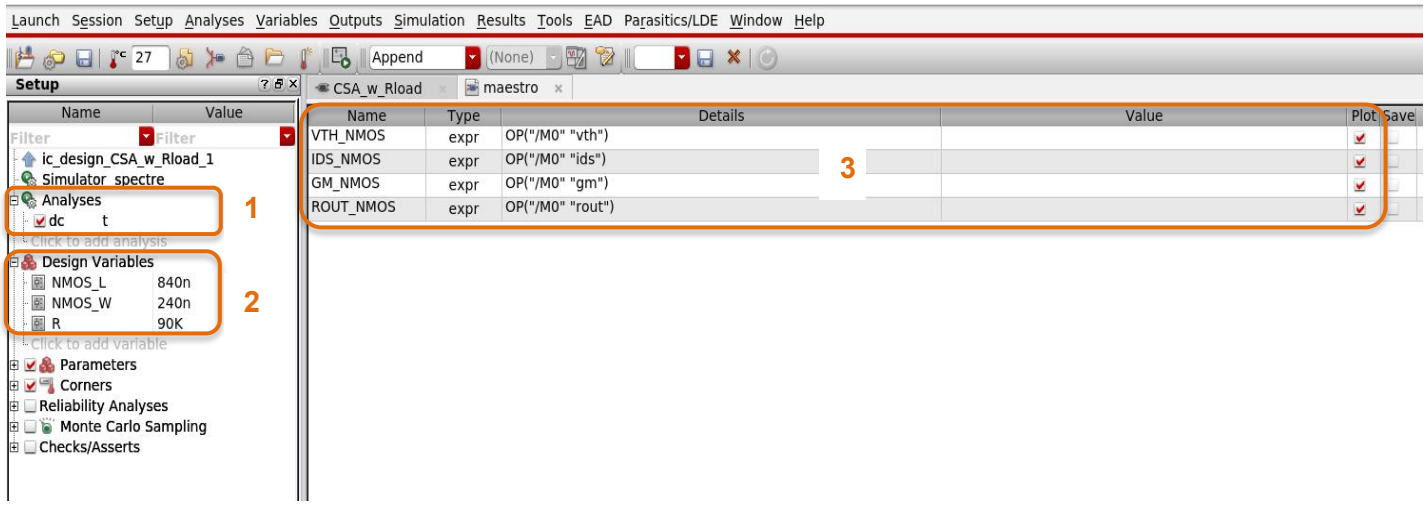
- To create a wire press **w** and draw between the two terminals you want to connect
- To edit properties of a component, click on the component and press **q**
- Press **lowercase 'L'** to create labels for nets like VDD, VOUT etc.



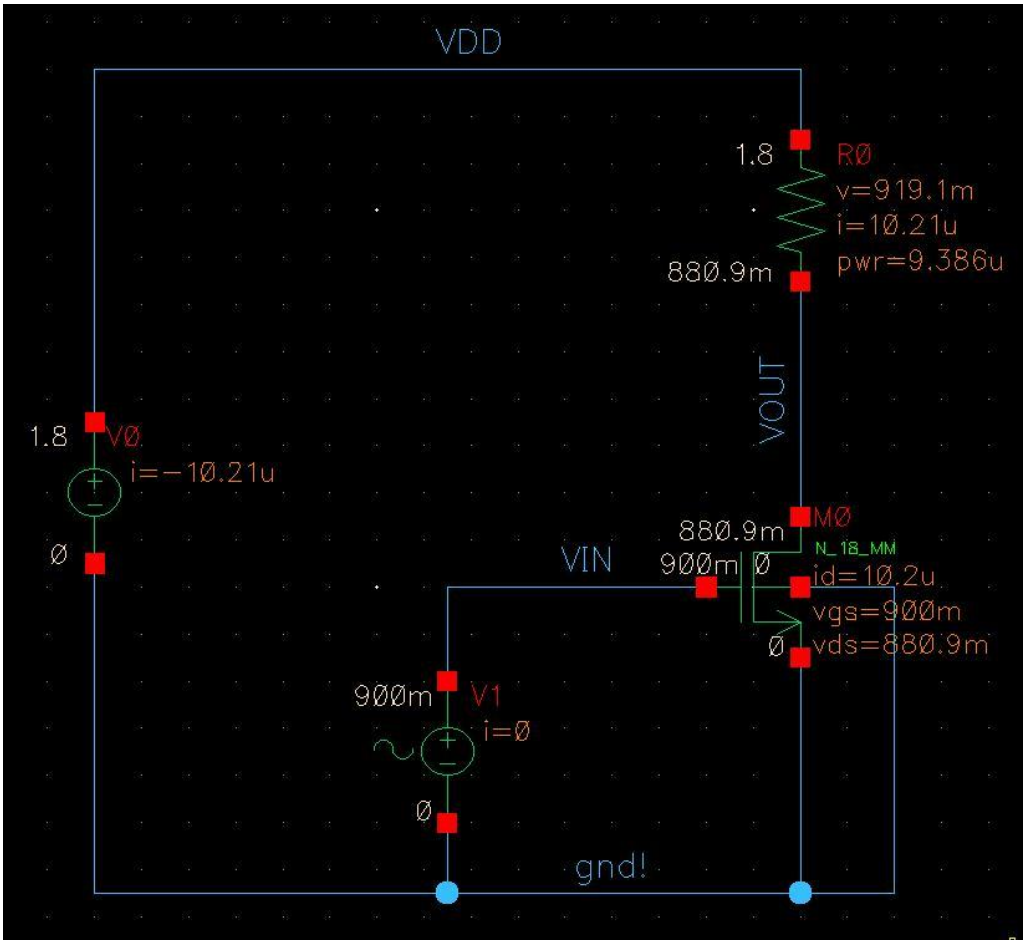
Setting up ADE-Explorer and performing DC simulation:

c) Create a new ADE-Explorer simulation setup (If facing any issue, refer TP1 - Page 13).

1. Create a DC analysis by clicking on “Click to add Analysis” in the **Analyses** palette of ADE-Explorer and save the required DC operating points in the DC analysis form
2. Set the resistor value, NMOS width and length in the ADE-Explorer **Design Variables** palette based on the hand calculations.
3. Make sure that the transistor instance name is “M0”. Save the following small-signal variables as the outputs (e.g., using OP(“/M0” “gm”)): vth, ids, gm, and rout (Again, you can do this from the calculator). The ADE-Explorer window will look as shown below. Please refer to TP1 - Page 21 if in doubt.



d) Run the DC operating point simulation and note the output dc voltage. The output dc voltage will be different than the required specification due to higher-order effects (i.e., we considered saturation current equation as a second-order equation. However, in reality, the MOS is modelled with higher-order equations. Further, the threshold voltage $V_{TH,\,N}$ will also be a function of the length of the MOSFET in actual simulations).



CSA_w_Rload | maestro

Name	Type	Details	Value
VTH_NMOS	expr	OP("/M0" "vth")	361.7m
IDS_NMOS	expr	OP("/M0" "ids")	10.2u
GM_NMOS	expr	OP("/M0" "gm")	34.46u
ROUT_NMOS	expr	OP("/M0" "rout")	1.346M

e) Iterate and arrive at the right dc operating point condition (change the width and/or length of NMOS). At every iteration, verify that the NMOS is in saturation.
(**Hint:** Annotate DC Node Voltages and DC Operating Points on the schematic (if in doubt, refer to TP1 – Page 15) or observe the saved current "IDS_NMOS" value and ensure that it is equal to 10uA. You don't need to match $V_{OUT,\,DC}$ to 0.9V or I_{DS} to 10uA exactly. An error of +/- 0.75% is okay.)

There are a few ways to make sure that your NMOS is in saturation:

- You can check that $V_{DS} > V_{GS} - V_{TH}$. However, note that this equation is based on a simpler model. In practice, there is a parameter called "vdsat". As long as your VDS > vdsat, the device will be in saturation.
- You can also check the parameter "region".

- If region = 0, the device is in cut-off (completely OFF)
- If region = 1, the device is in linear (or triode) region
- If region = 2, the device is in saturation region
- If region = 3, the device is in sub-threshold region
- If region = 4, the device is in breakdown region

- Both “vdsat” and “region” can be added to the Outputs as shown below.

Name	Type	Details	Value	Plot
VTH_NMOS	expr	OP("/M0" "vth")	383.1m	☑
IDS_NMOS	expr	OP("/M0" "ids")	9.965u	☑
GM_NMOS	expr	OP("/M0" "gm")	35.29u	☑
ROUT_NMOS	expr	OP("/M0" "rout")	1.509M	☑
VDSAT_NMOS	expr	OP("/M0" "vdsat")	432.1m	☑
REGION_NMOS	expr	OP("/M0" "region")	2	☑

f) Calculate the small-signal gain of the circuit using the CS amplifier gain equation as discussed in the class. Write (DON’T copy and paste) the following gain expression of the CS amplifier in ADE-Explorer and save it as an output as well:
OP(“/M0” “gm”) * (VAR(“R”) * OP(“/M0” “rout”)) / (VAR(“R”) + OP(“/M0” “rout”))
Please check with the TAs if you face any issues writing these expressions.

Note: By using VAR(“R”), ADE-Explorer lets you access the value of R specified by the user in the **Design Variables** palette.

Name	Type	Details	Value	Plot
VTH_NMOS	expr	OP("/M0" "vth")	383.1m	☑
IDS_NMOS	expr	OP("/M0" "ids")	9.965u	☑
GM_NMOS	expr	OP("/M0" "gm")	35.29u	☑
ROUT_NMOS	expr	OP("/M0" "rout")	1.509M	☑
VDSAT_NMOS	expr	OP("/M0" "vdsat")	432.1m	☑
REGION_NMOS	expr	OP("/M0" "region")	2	☑
R	expr	VAR("R")	90K	☑
GAIN_CALC	expr	((GM_NMOS * R * ROUT_NMOS) / (R + ROUT_NMOS))	2.997	☑

Does it meet the specification? If yes, proceed to the ac simulation in ADE-Explorer as shown in step **(g).** If not, how would you increase the gain? What is the theoretical limit of the gain that can be achieved? To answer this, consider the gain equation:

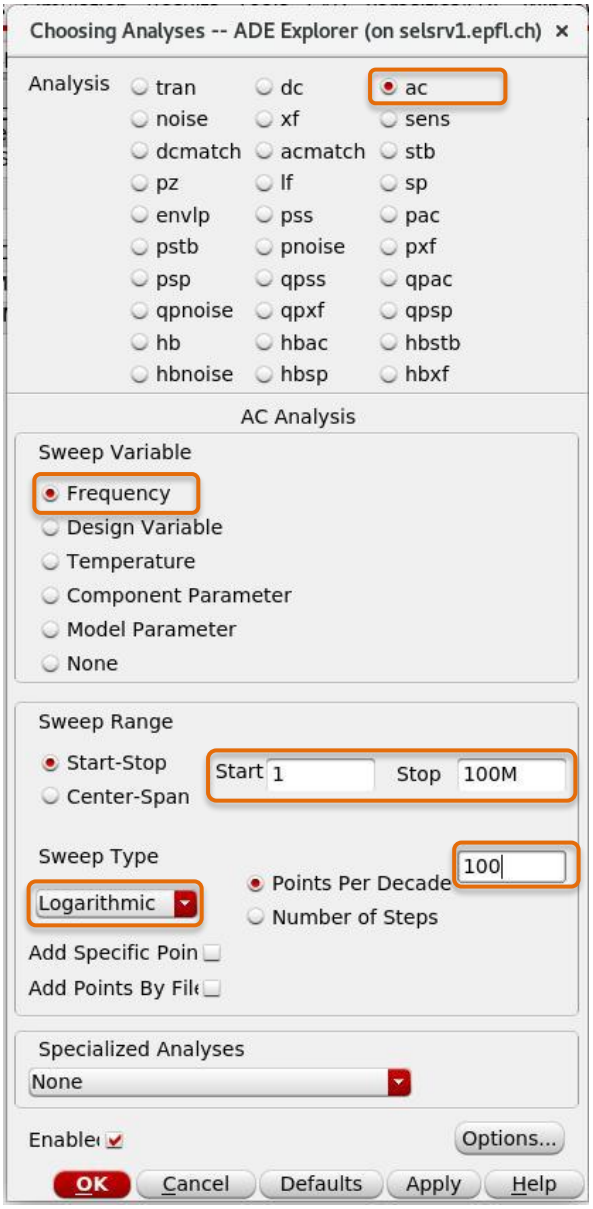
- $|A_v| = g_m (R \parallel r_o)$
- $|A_v| = g_m R$ (assuming $r_o >> R$). Make sure this is true for you!
- $|A_v| = \frac{2I_D R}{V_{IN} - V_{TH,N}}$
- $|A_v| = \frac{2(V_{DD} - V_{OUT})}{V_{IN} - V_{TH,N}}$

Given that all the parameters V_{DD}, V_{OUT}, V_{IN} are part of the specifications, the gain of a CS amplifier with a load of R is decided the moment the input and output dc voltages are fixed.

Note that at this point the maximum achievable gain for a CS amplifier with a load of R is dependent on the input and output dc voltages irrespective of the MOS current and aspect ratios. The only way to adjust the gain seems to be by exploiting the weak dependance of $V_{TH,N}$ on the length "NMOS_L" of M0.

Performing AC small-signal simulation:

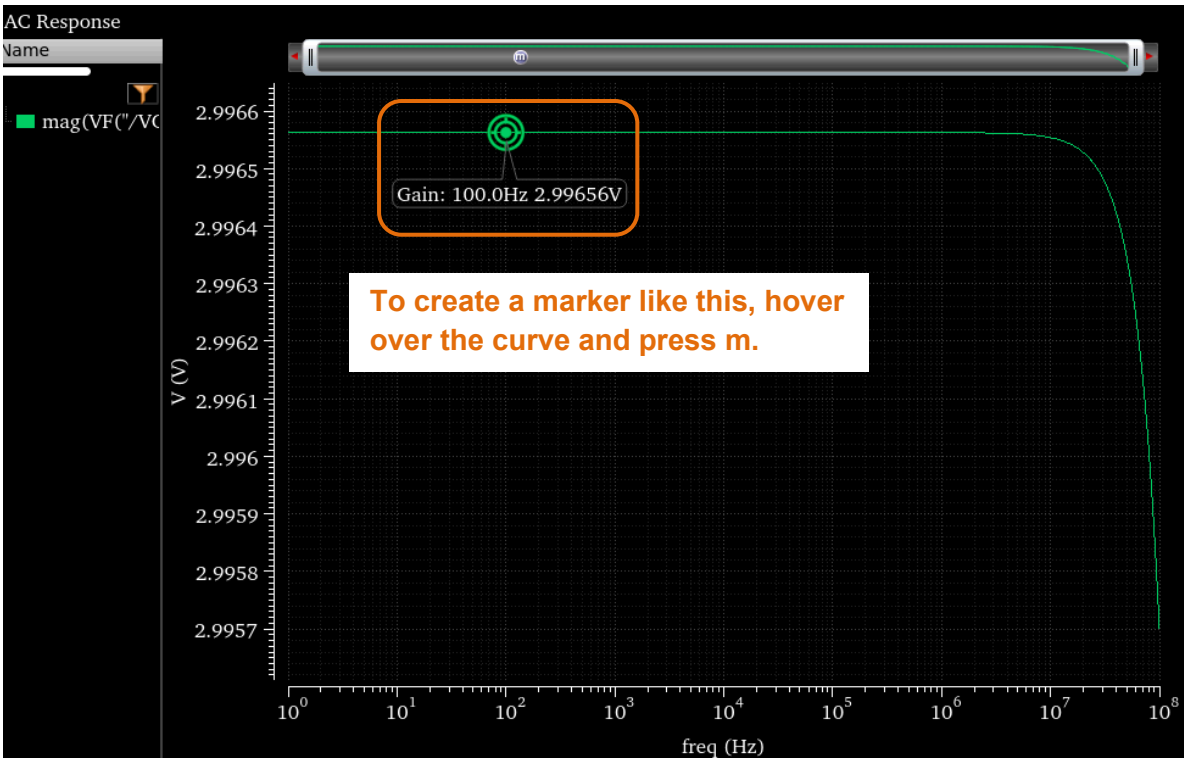
g) Add a new analysis in ADE-Explorer Analyses section by clicking 'Click to add analysis' and choose **"ac".** The ac simulation setup is shown below:



- Run the ac simulation using ADE-Explorer and verify the gain obtained.

- Once you run the ac simulation, plot the ac gain as a function of frequency (Frequency response similar to Bode-plot), in **ADE-Explorer -> Results -> Direct Plot -> AC magnitude**, click on the output node "VOUT" in the schematic and press the Esc key.

- Alternately, you can add the following expression to your ADE-Explorer outputs to plot the AC Gain: mag(VF("VOUT")/VF("VIN")). This will plot the AC response (ac gain as a function of frequency) as shown below:



The AC simulation linearizes the circuit around the DC operating point, like the small-signal analysis, then solves the **linear** circuit in the frequency domain (hence the syntax VF for the ac analysis). Since we are now in the frequency domain, the voltage and currents are in the complex number domain. This is why we take the magnitude of the gain expression with the **mag() function.**

In the resulting waveform, you should observe the gain computed at low frequencies, with a roll-off at high frequencies. At higher frequencies, due to the CGD of the NMOS, the circuit behaves like a first-order system. You might be familiar with this from your previous courses. However, we are not covering the frequency response of amplifiers in this course, so we won't examine this behavior in detail.

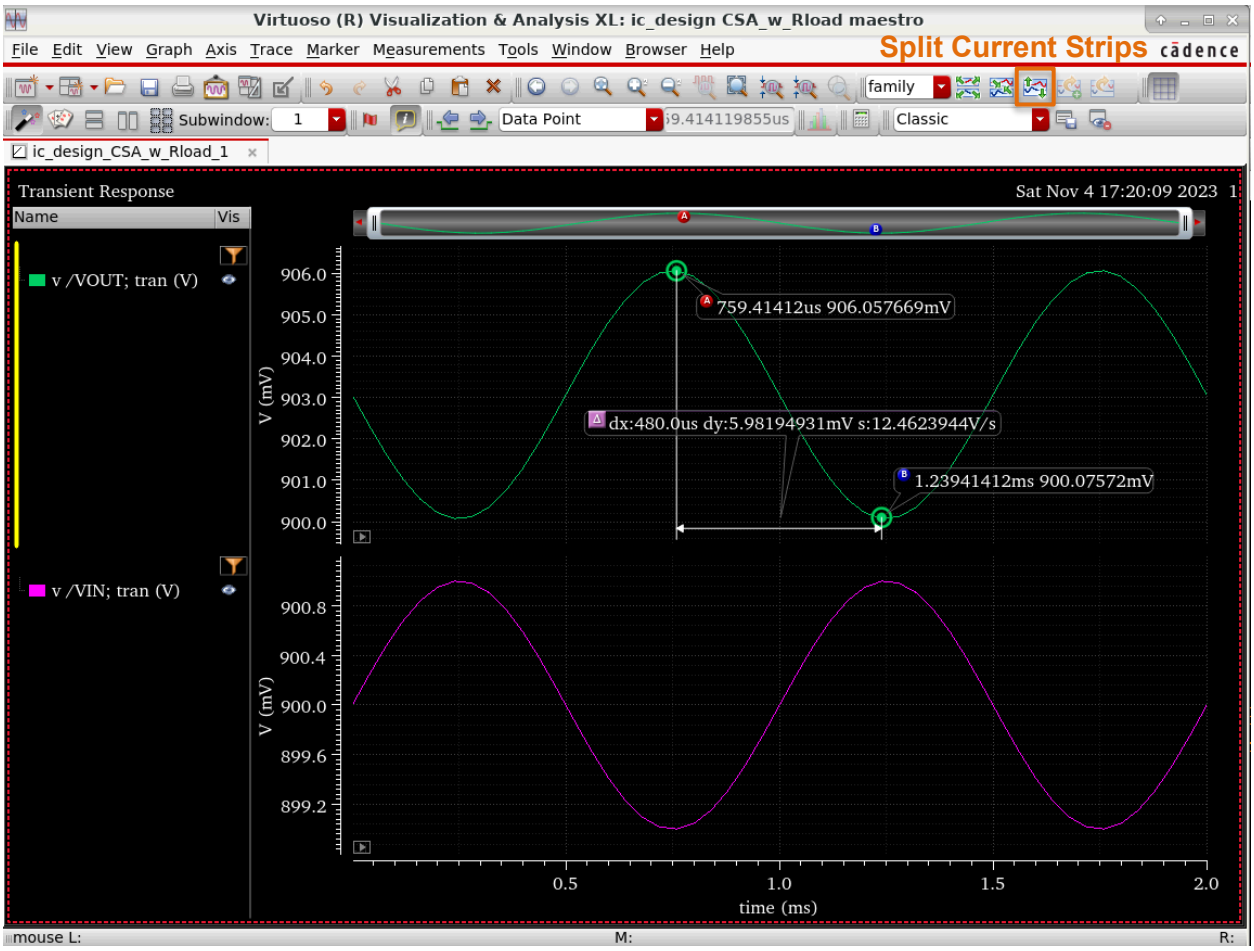
Verifying the gain with transient simulation:

h) Disable the **"dc"** and **"ac"** analysis and add a new transient analysis **"tran"** by clicking 'Click to add Analysis' in the **Analysis** palette of ADE-Explorer. Run the transient simulation for 2 ms (note that voltage source V1 had an input frequency set to 1 kHz). This should cover two cycles of the input sinusoid. Run the transient simulation.

Note that earlier you verified the gain with a small-signal model (linearized around the operating point). Here, you are verifying the gain with the large-signal model (actual nonlinear equations are solved).

To plot the waveforms in ADE-Explorer, go to **Results -> Direct plot -> Transient Signal** and click on the input and output nodes on the schematic. Now Press **Esc**. A waveform window will pop up.

Hint: Press on the “Split Current Strips” as highlighted in the figure below. Hover over the peak and press **“a”** and then hover over the trough in the waveform and press **“b”** to measure the peak-to-peak voltage (voltage swing) and verify the gain of the circuit. Also, note the output phase shift of 180 degrees.

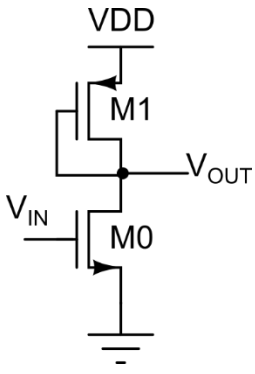


Now, to verify that the gain is highly coupled to the DC operating point, re-design the circuit with the same specifications except the output dc voltage of 0.6V instead of 0.9V. Verify all the simulations and compare with the hand calculations.

This completes the design and simulation of the CS amplifier with the R load.

2. Common-Source Amplifier with a Diode-Connected MOS Load

Continuing the CS amplifier with resistive load, we will now design a CS amplifier with a PMOS diode-connected load as shown in the schematic diagram.



The following specifications are given:
$V_{IN,\,DC}$ = 0.9V, $V_{OUT,\,DC}$ = 0.9V, I_D = 10µA.

a. Use hand calculations to arrive at the MOS sizing.
Hint: Note that you need to size only the PMOS device since NMOS will have the same sizing as the CS amplifier with a resistive load. This is because the NMOS still has the same operating point conditions (i.e., I_D, V_{GS} and V_{DS}) as the CS amplifier with R load.

b. Create the schematic in Virtuoso based on the hand calculation.

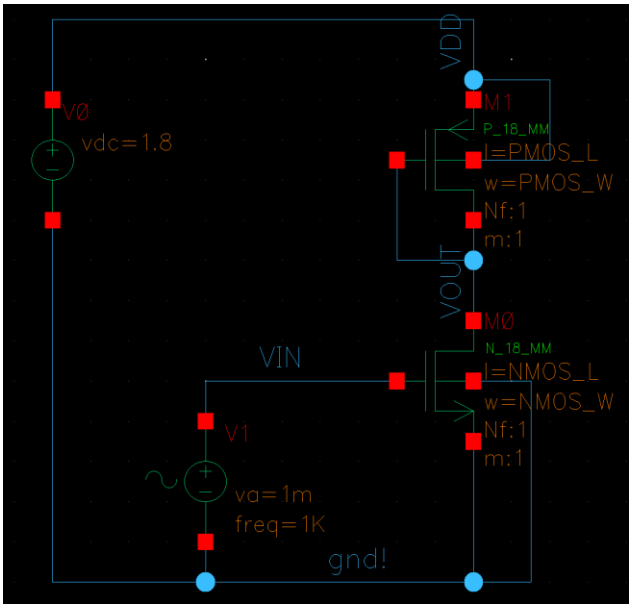
c. Perform DC simulation using ADE-Explorer and write the necessary output expression to plot the AC gain. Iterate the PMOS length and/or width to arrive at the desired specifications. (Again, an error of 0.5% in the operating point is fine)

d. Derive the limit on the small-signal gain based on the saturation current equation. Does the small-signal gain depend on the input and output dc node voltages irrespective of the MOS sizing (like the CS amplifier with resistive load)?

e. Perform ac simulation and verify the AC small-signal gain obtained with hand calculations and the expression.

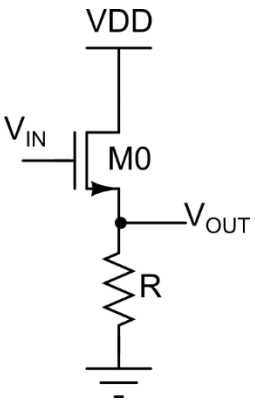
f. Perform transient analysis and verify the large signal gain.

g. Re-design the circuit for the following specifications and repeat steps (c) to (f)
$V_{IN,\,DC}$ = 0.9V, $V_{OUT,\,DC}$ = 0.6V, I_D = 10µA.



3. Common-Drain (aka Source Follower) Stage

We now design a source follower using an NMOS transistor (**with body terminal to ground**) to meet the following specifications:



$V_{IN,\,DC}$ = 0.9V, $V_{OUT,\,DC}$ = 0.4V, I_D = 1µA, L = 1µm (NMOS length), $V_{TH,\,N}$ = 0.45V

a. Use hand-calculations to arrive at the MOS sizing and the resistor value.

b. Create the schematic in Virtuoso based on the hand calculation.

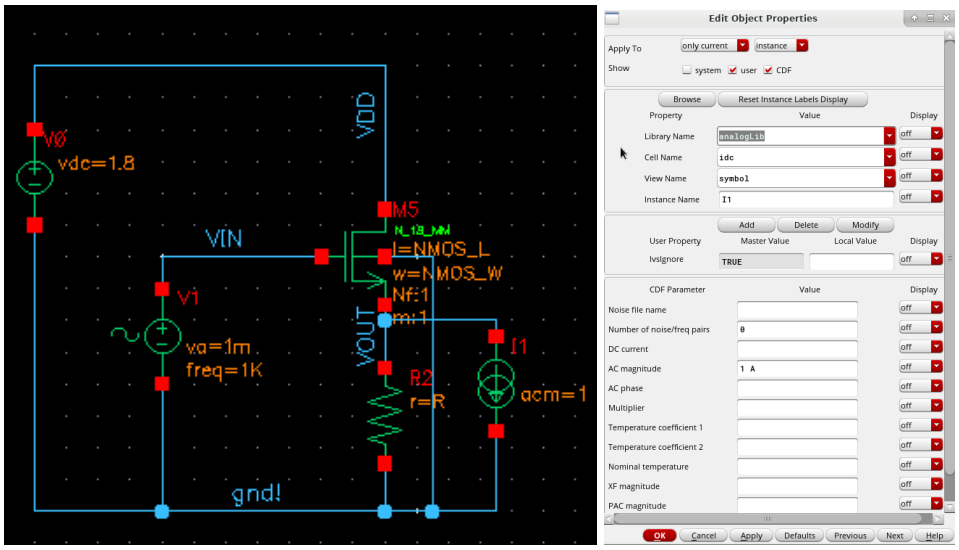
c. Perform DC simulation using ADE-Explorer. Iterate the NMOS width (if needed) to arrive at the specifications.

d. Obtain the ac small-signal gain equation (ignore r_o) in terms of g_m, g_{mb} and R. Write this output expression on ADE-Explorer to calculate the gain.

e. Perform ac simulation and verify the AC small-signal gain obtained with hand calculations and the expression.

f. Perform transient analysis and verify the large signal gain. Note that the gain is positive.

g. Derive the output resistance of the source follower in terms of g_m, g_{mb}, R and r_o.



h. Set the AC magnitude of the voltage source to 0. Add a current source I1 across the resistor R and set its AC magnitude to 1 (as shown above). Run an ac simulation and plot V_{OUT} from **ADE-Explorer -> Results -> Direct Plot -> AC Magnitude**. This in effect plots V_{OUT}/I_1 which is the output impedance. This is because the ac magnitude of the current source I_1 is set to 1. Compare the output resistance obtained from the simulation with the derived value.

i. Repeat the design for a bias current of 10µA. Compare the small-signal gain and output resistance for the two design cases.