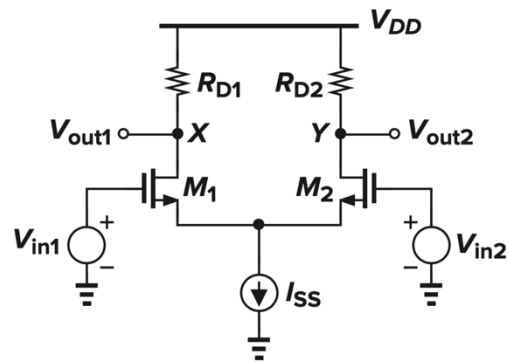


## Analog IC design (EE-320), Lecture 9

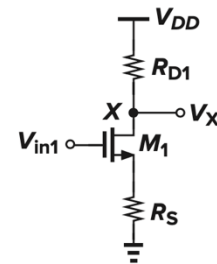
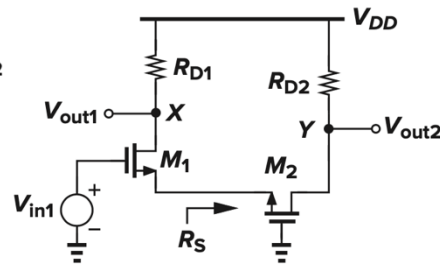
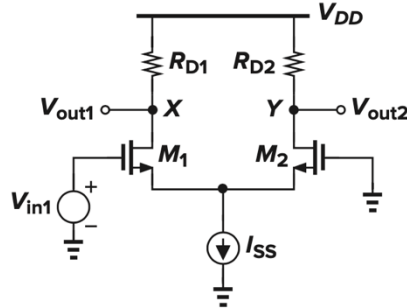
Prof. Mahsa Shoaran

Institute of Electrical and Micro Engineering, School of Engineering, EPFL

# Review: Diff Pair Small-Signal Model



## Small-signal analysis: gain (method 1)



$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

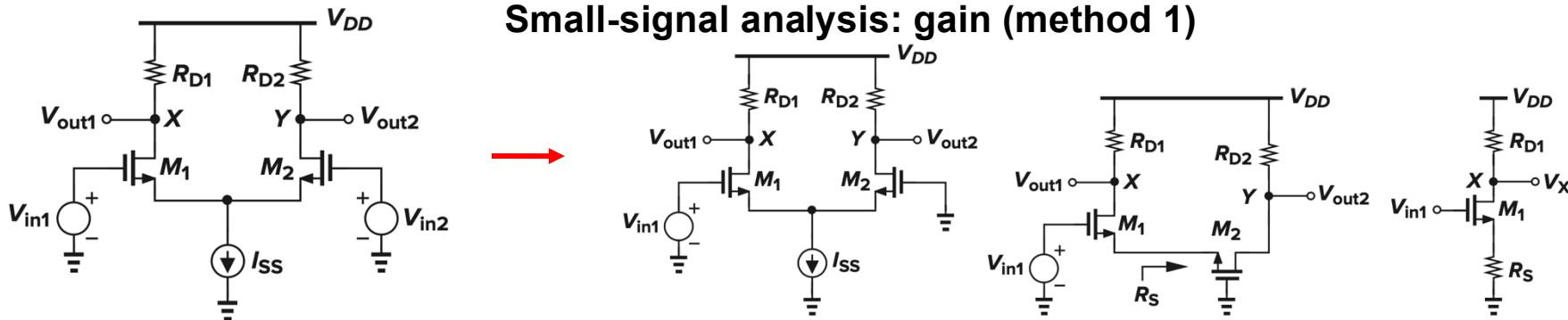
$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

$$(V_X - V_Y)|_{\text{Due to } V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

$$\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D$$

# Review: Diff Pair Small-Signal Model

## Small-signal analysis: gain (method 1)



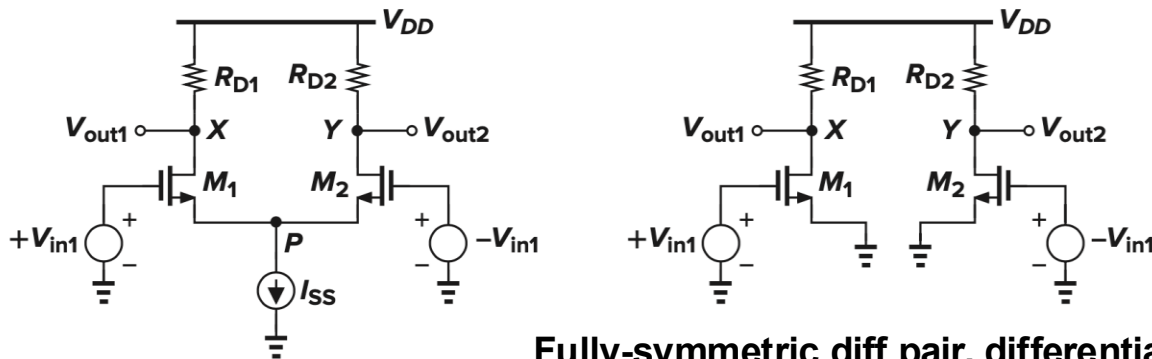
$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

$$(V_X - V_Y)|_{\text{Due to } V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

$$\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D$$

## Small-signal gain with half-circuit model (method 2)



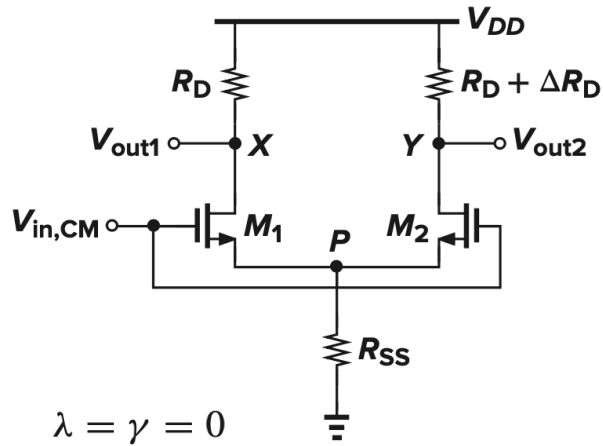
$$V_X/V_{in1} = -g_m R_D$$

$$V_Y/(-V_{in1}) = -g_m R_D$$

$$(V_X - V_Y)/(2V_{in1}) = -g_m R_D$$

Fully-symmetric diff pair, differential inputs

# Review: Diff Pair Mismatch, CMRR



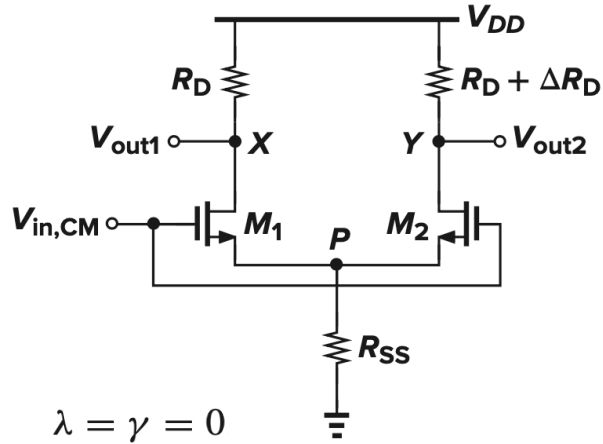
**Load/input mismatch: differential output changes by CM input**

$$\Delta V_P = \frac{R_{SS}}{R_{SS} + \frac{1}{2g_m}} \Delta V_{in,CM}$$

$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D)$$

# Review: Diff Pair Mismatch, CMRR

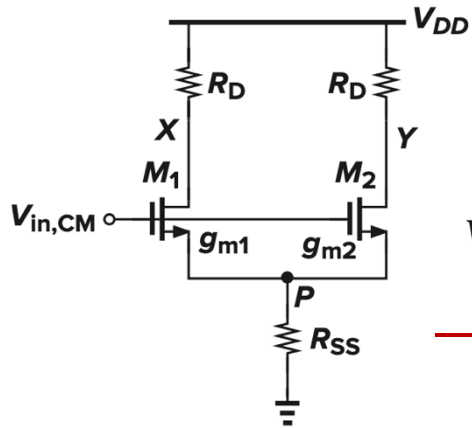


Load/input mismatch: differential output changes by CM input

$$\Delta V_P = \frac{R_{SS}}{R_{SS} + \frac{1}{2g_m}} \Delta V_{in,CM}$$

$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D)$$

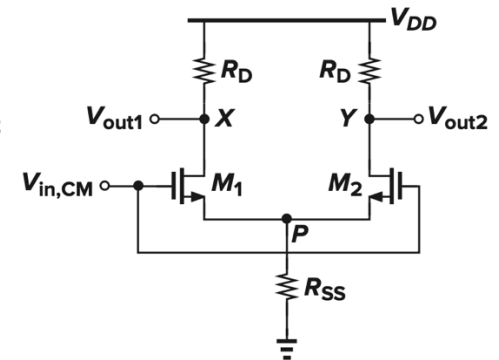
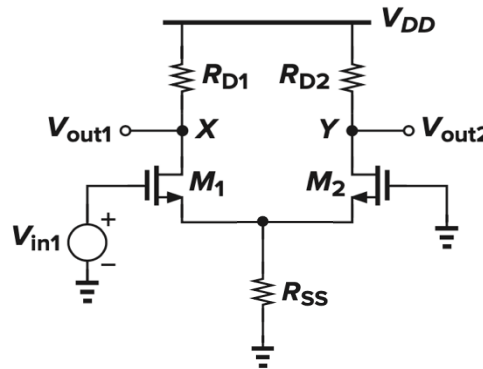


$$V_P = \frac{(g_{m1} + g_{m2}) R_{SS}}{(g_{m1} + g_{m2}) R_{SS} + 1} V_{in,CM}$$

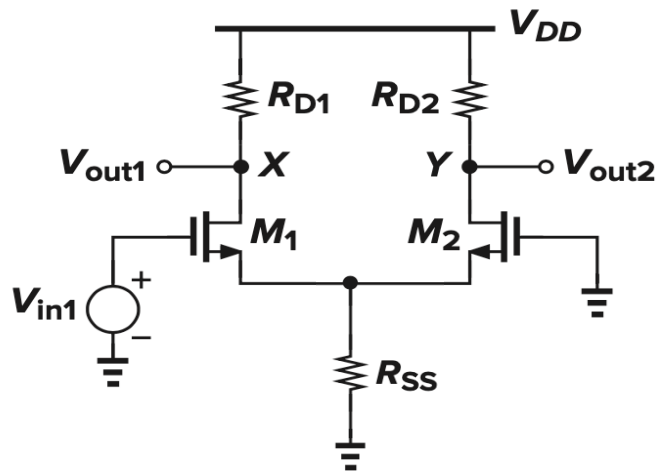
$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) R_{SS} + 1}$$

$$V_X - V_Y = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2}) R_{SS} + 1} R_D V_{in,CM}$$

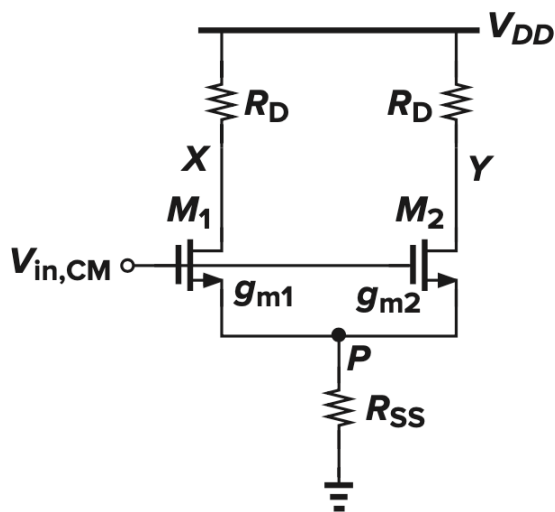
$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$



# CMRR



$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}$$



$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2})R_{SS} + 1}$$

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

$$\begin{aligned} \text{CMRR} &= \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} \\ &\approx \frac{g_m}{\Delta g_m} (1 + 2g_m R_{SS}) \end{aligned}$$

$$g_m = (g_{m1} + g_{m2})/2 \quad \Delta g_m = g_{m1} - g_{m2}$$

$$2g_m R_{SS} \gg 1$$



$$\text{CMRR} \approx 2g_m^2 R_{SS} / \Delta g_m$$

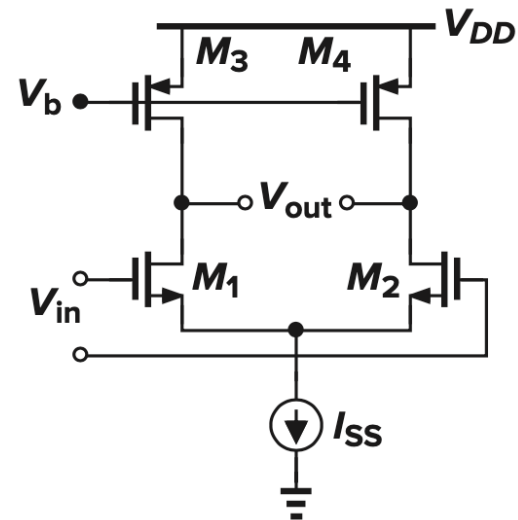
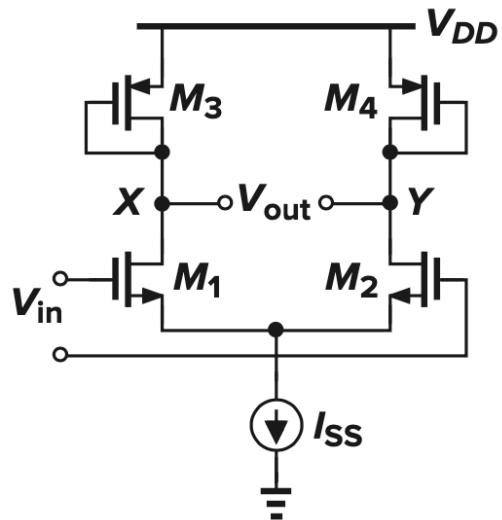
$$= \frac{2g_m R_{SS}}{\left( \frac{\Delta g_m}{g_m} \right)}$$

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

$$\text{in dB: } \text{CMRR}(dB) \equiv 20 \log \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

**CMRR should be as large as possible**

# Differential Pair with MOS Loads



$$A_v = -g_{mN} (g_{mP}^{-1} \parallel r_{ON} \parallel r_{OP})$$

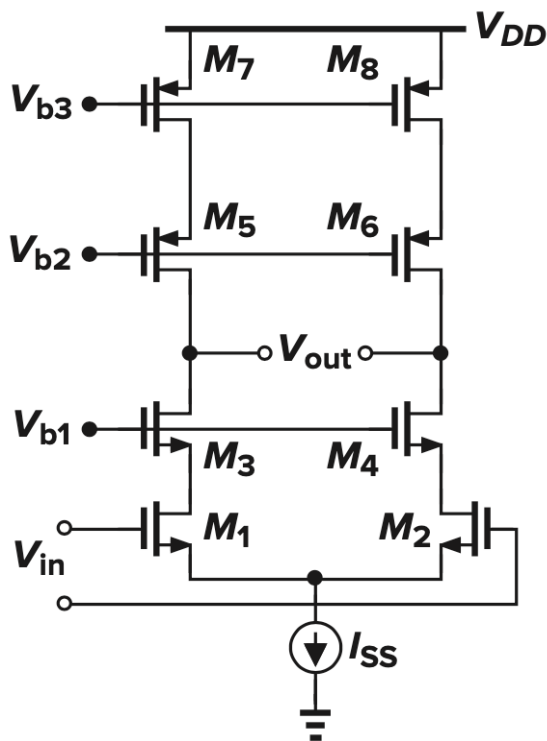
$$\approx -\frac{g_{mN}}{g_{mP}}$$

$$A_v = -g_{mN} (r_{ON} \parallel r_{OP})$$

$$A_v \approx -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$

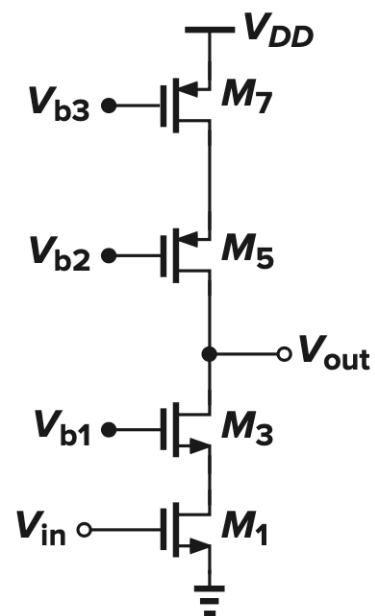
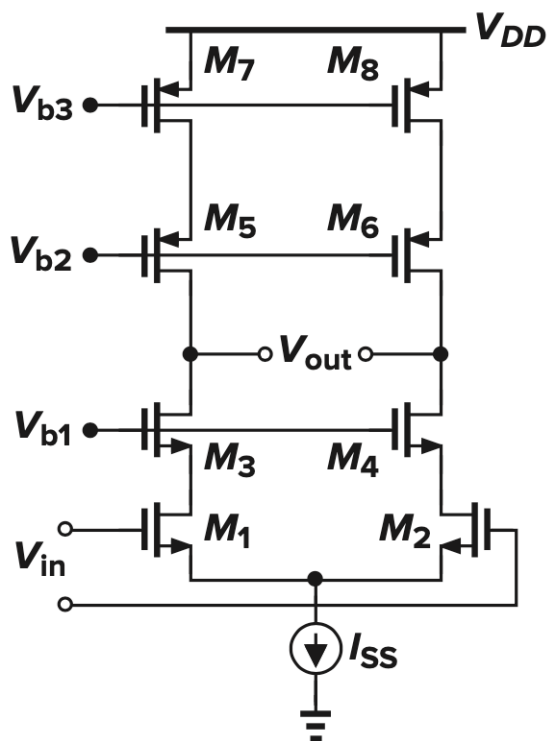
# Cascode differential pair

- The gain of the differential pair with current-source loads relatively low, in the range of 5 to 10 in nanometer technologies
  - increase the output impedance of both PMOS and NMOS by **cas coding**



# Cascode differential pair

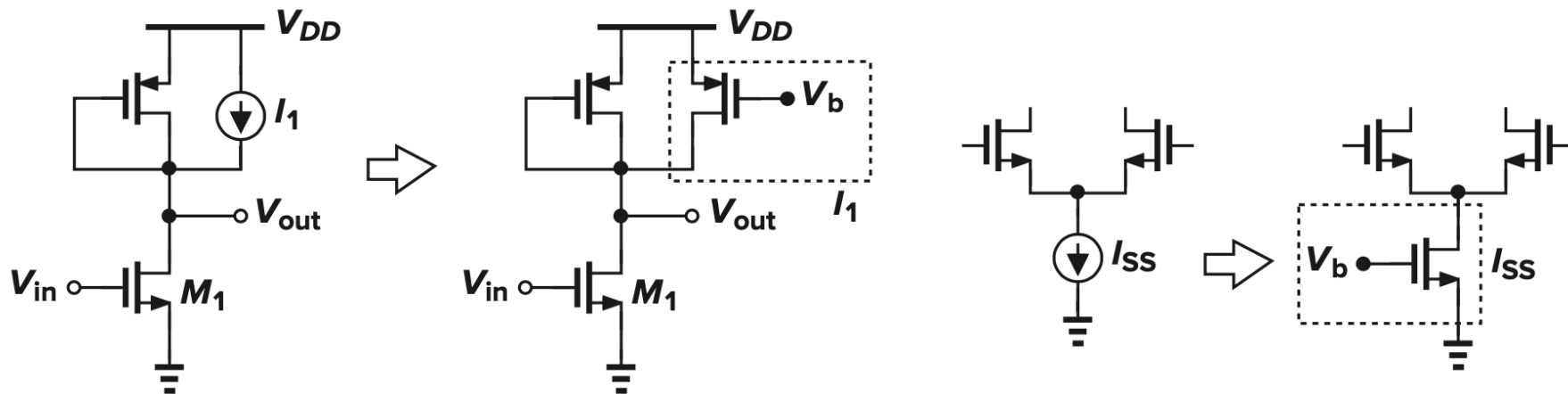
- The gain of the differential pair with current-source loads relatively low, in the range of 5 to 10 in nanometer technologies
  - increase the output impedance of both PMOS and NMOS by **cas coding**
  - increases the differential **gain** at the cost of more **headroom**



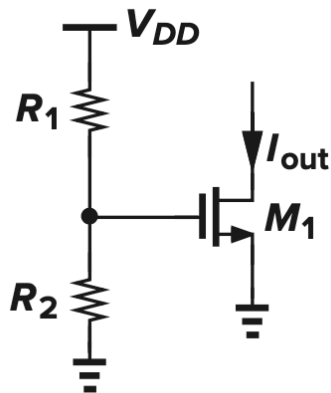
$$|A_v| \approx g_{m1} [(g_{m3} r_{o3} r_{o1}) \parallel (g_{m5} r_{o5} r_{o7})]$$

# Current Mirrors

- Current sources act as a **large resistor** without consuming excessive voltage headroom
- MOS devices operating in **saturation** can act as a current source
- In conjunction with “**current mirrors**” perform useful functions
- Important for **biasing** analog circuits



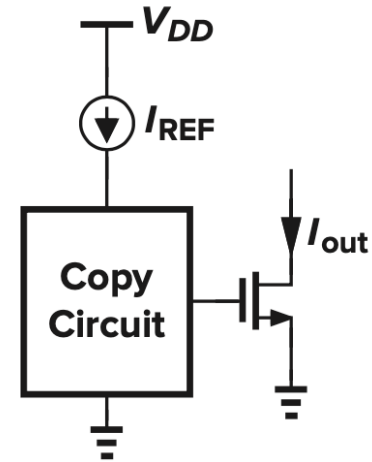
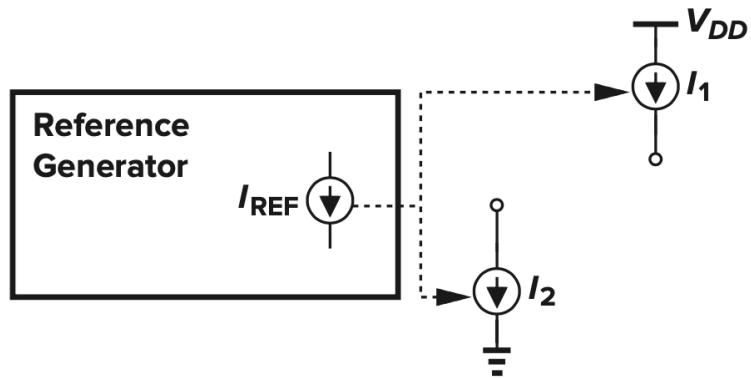
# Definition of current by resistive divider



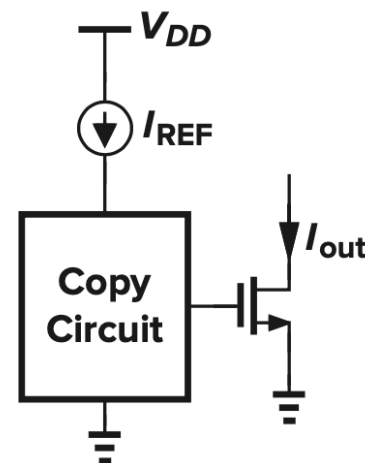
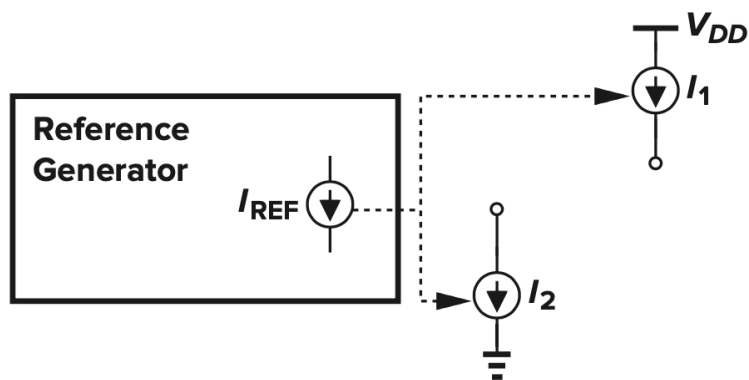
$$I_{out} \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( \frac{R_2}{R_1 + R_2} V_{DD} - V_{TH} \right)^2$$

- Various PVT dependencies of  $I_{out}$ , thus, it is poorly defined
  - the overdrive voltage is a function of  $V_{DD}$  and  $V_{TH}$
  - the threshold voltage may vary by 50 to 100 mV from wafer to wafer
  - both  $\mu_n$  and  $V_{TH}$  exhibit temperature dependence

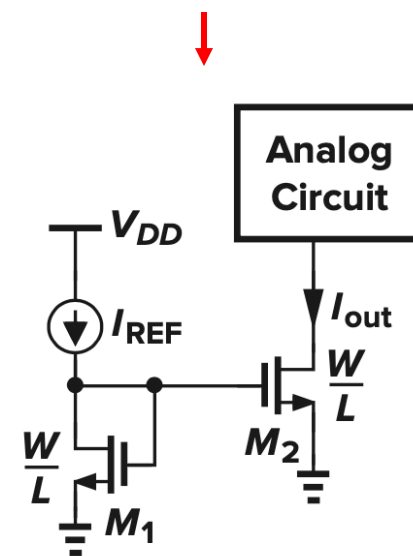
# Copying current from a reference



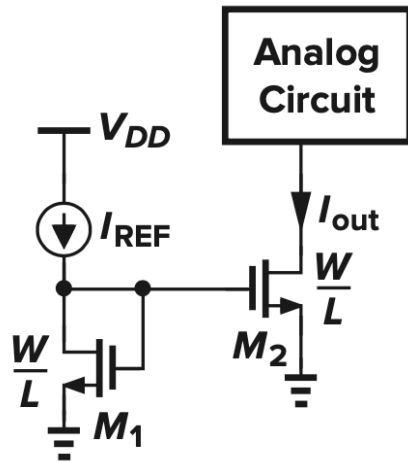
# Copying current from a reference



- *Diode-connected device in a basic current mirror*
- Two identical MOS devices that have equal gate-source voltages and operate in **saturation** carry equal currents (if  $\lambda = 0$ )



# Basic current mirror



(neglecting channel-length modulation)

$$I_{REF} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_1 (V_{GS} - V_{TH})^2$$

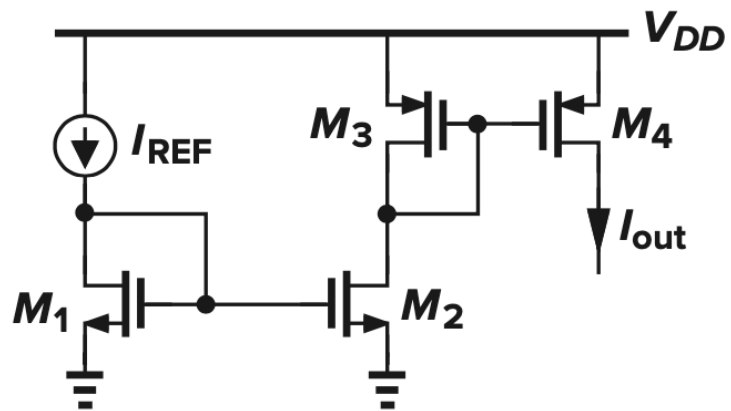
$$I_{out} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{TH})^2$$



$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

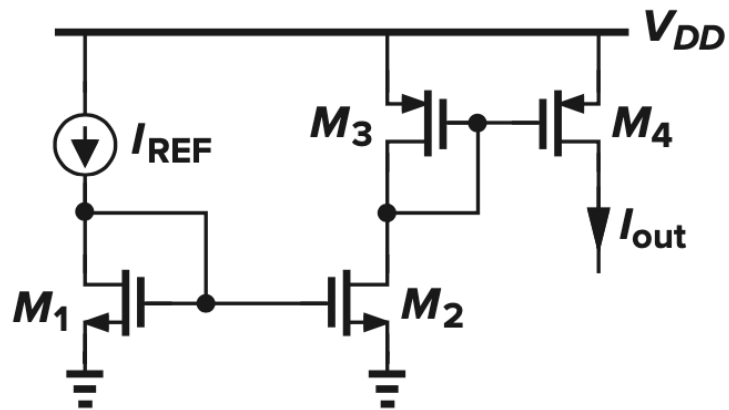
- ✓ it allows precise copying of the current with **no dependence on process and temperature**, based on the **ratio of device dimensions**, a quantity that can be controlled with reasonable accuracy

# Example: Calculate $I_{out}$



- ❖ the drain current of  $M_4$  if all transistors in saturation

# Example: Calculate $I_{out}$



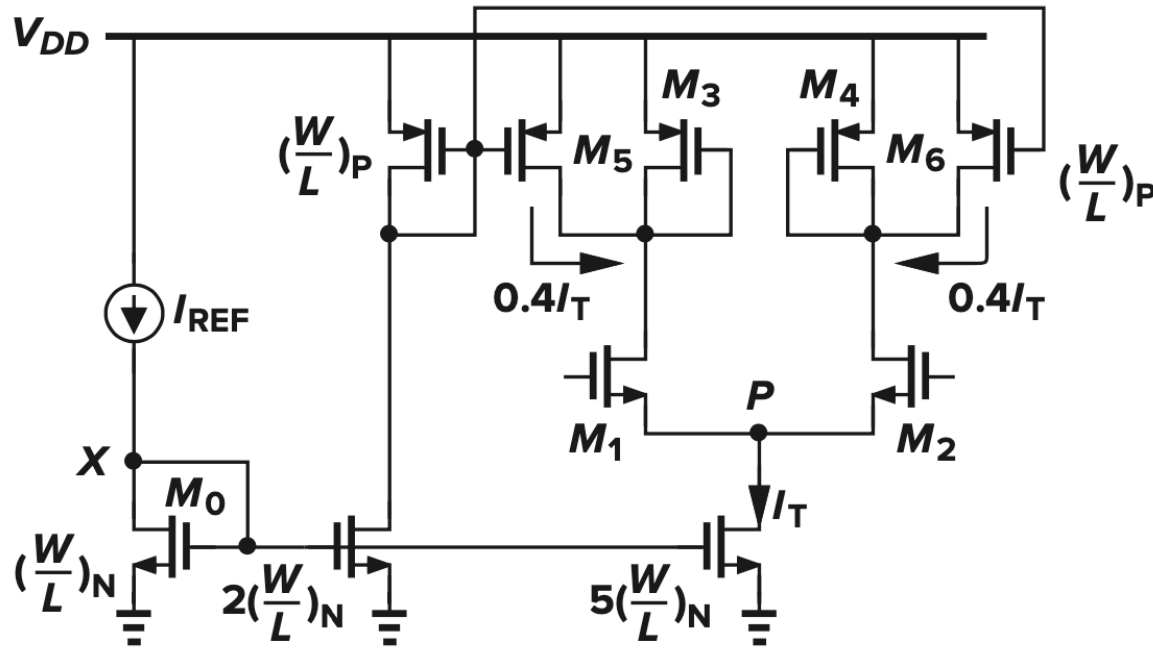
- ❖ the drain current of  $M_4$  if all transistors in saturation

$$I_{D2} = I_{REF} [(W/L)_2 / (W/L)_1]$$

$$I_{D4} = I_{D3} \times [(W/L)_4 / (W/L)_3]$$

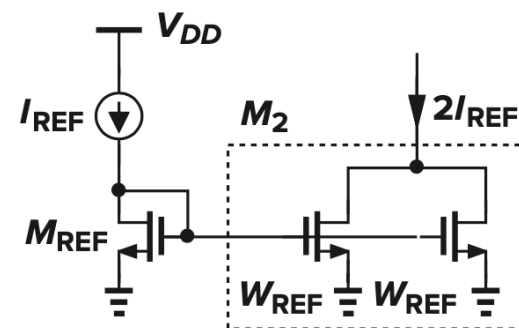
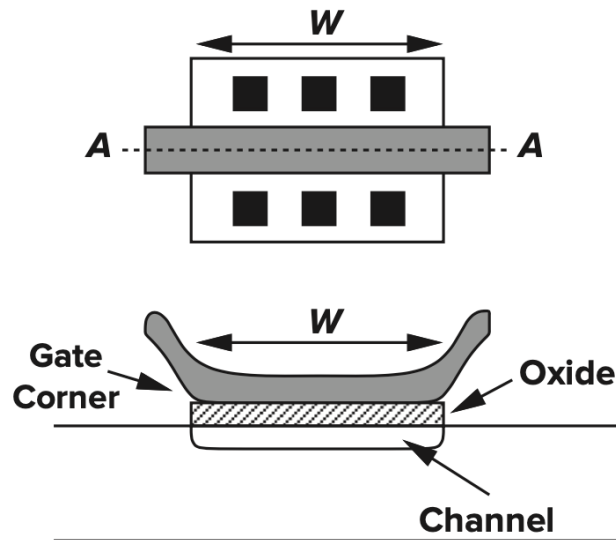
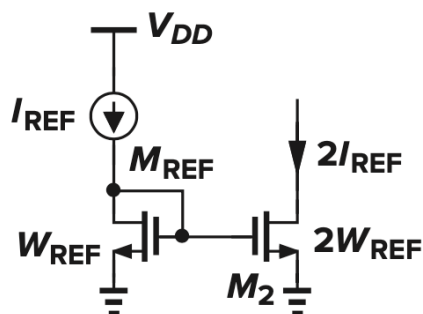
$$\alpha = \beta = 5 \quad \rightarrow \quad I_{REF} \times 25$$

# Current mirrors to bias a differential amplifier

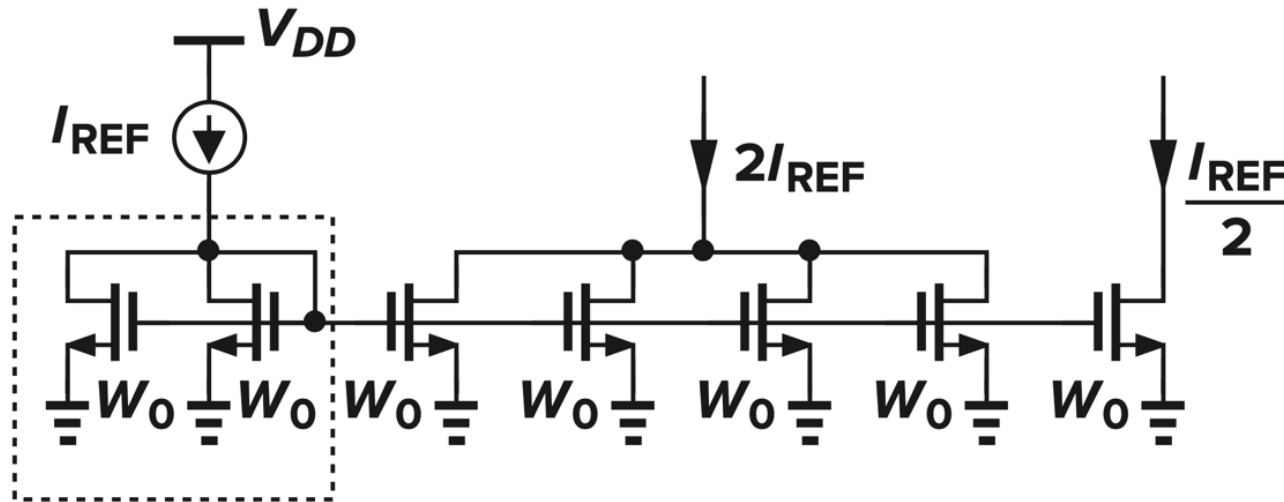


# Sizing issues

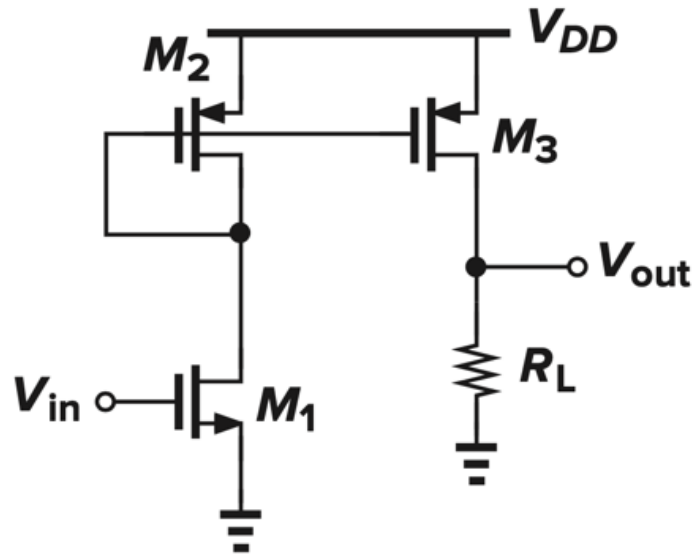
- Current mirrors usually employ the **same length** for all of transistors to minimize errors due to the side-diffusion of the source and drain areas ( $L_D$ )
- Direct scaling of the width faces difficulties
  - Since the “corners” of the gate are poorly defined, if the drawn  $W$  is doubled, the actual width does not exactly double
- “**unit**” transistors are used to create copies by *repeating* such a device



# Current mirror with unit transistors



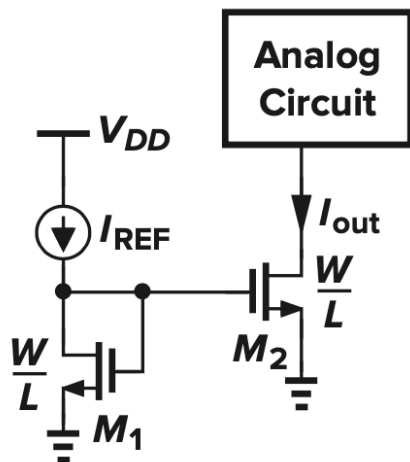
# Example: Calculate the gain



Voltage gain:

$$g_{m1} R_L (W/L)_3 / (W/L)_2$$

# Effect of channel length modulation



- **Channel-length modulation** produces significant error in copying currents, especially if **minimum-length transistors** are used to minimize the width (and the output **capacitance**)

$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_1 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

# Exam regulations

- Please check the document '***Final exam regulations***' that will be provided on Moodle
  - The final exam will be written on campus
  - The duration of the exam is 3 hours
  - You can bring one page with formulas on one or both sides
  - You need a calculator
- If you have questions, you can email myself or the TAs

**Thank you!**

