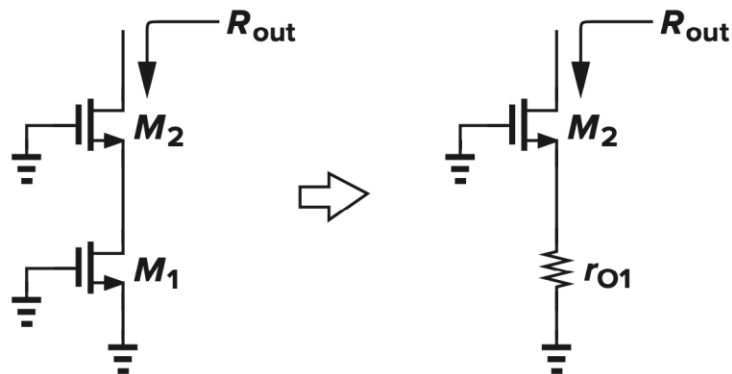


Analog IC design (EE-320), Lecture 8

Prof. Mahsa Shoaran

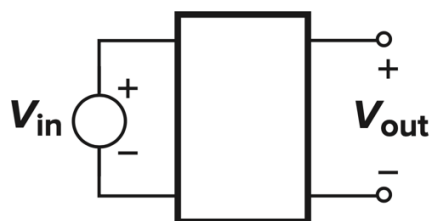
Institute of Electrical and Micro Engineering, School of Engineering, EPFL

Review: Cascode. Diff Pair



Cascode: high output impedance

$$R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$$

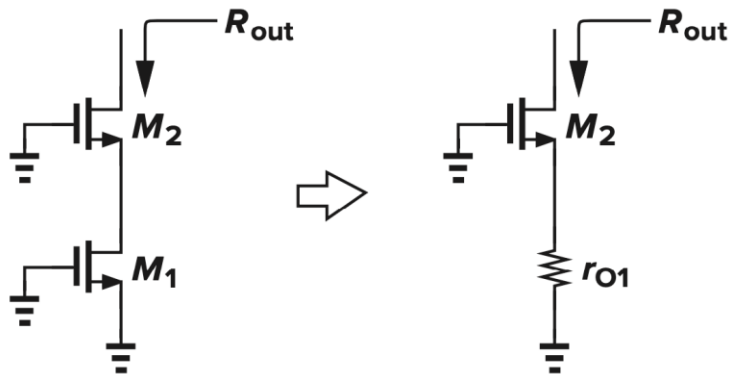


$$G_m \equiv I_{out} / V_{in}$$

$$A_v \equiv -G_m R_{out}$$

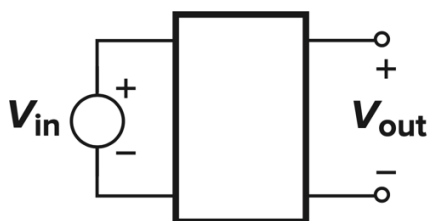
- For G_m calculation: the output is ac shorted
- For R_{out} calculation: the input voltage is set to zero

Review: Cascode. Diff Pair



Cascode: high output impedance

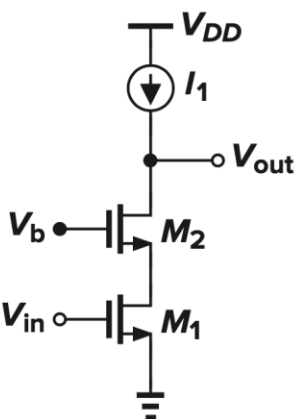
$$R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$$



$$G_m = I_{out} / V_{in}$$

$$A_v = -G_m R_{out}$$

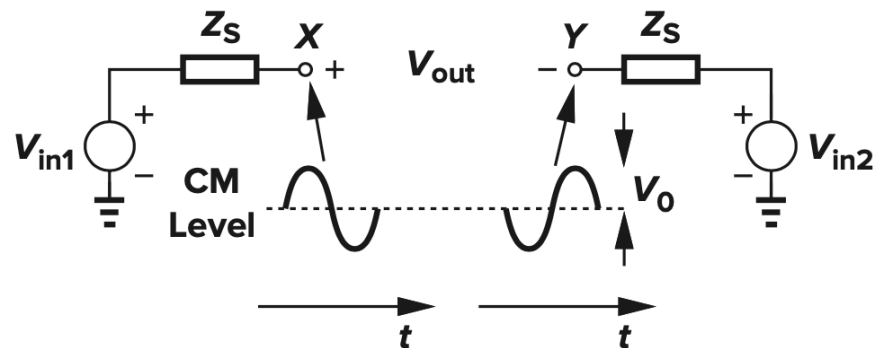
- For G_m calculation: the output is ac shorted
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$$G_m \approx g_{m1}$$

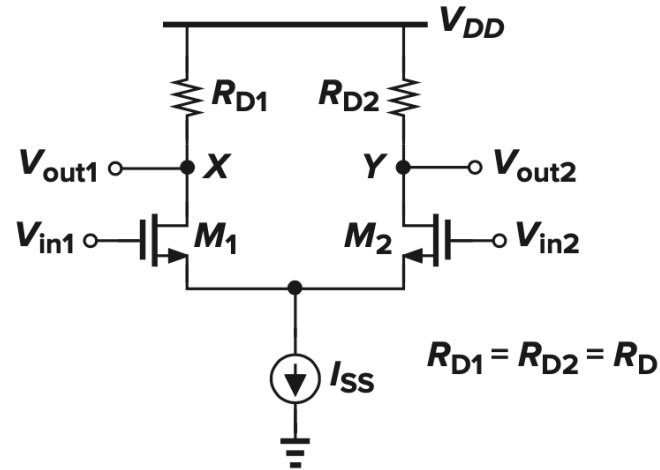
$$R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$$

$$|A_v| = (g_{m2} + g_{mb2})r_{o2}g_{m1}r_{o1}$$

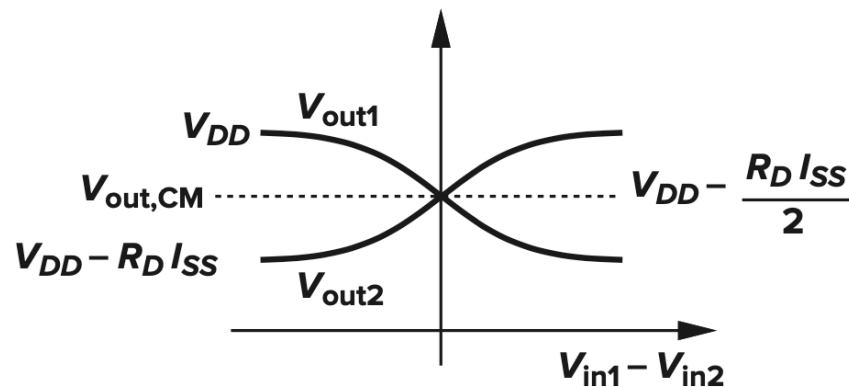


Differential input-output characteristics

(neglecting channel-length modulation and body effect):

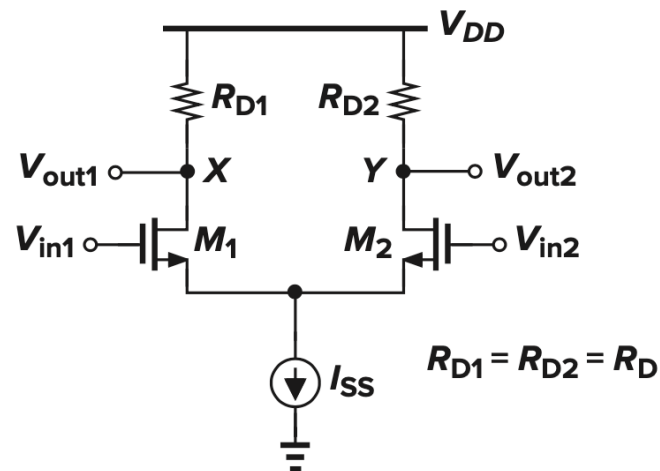


Differential input-output characteristics of a diff pair

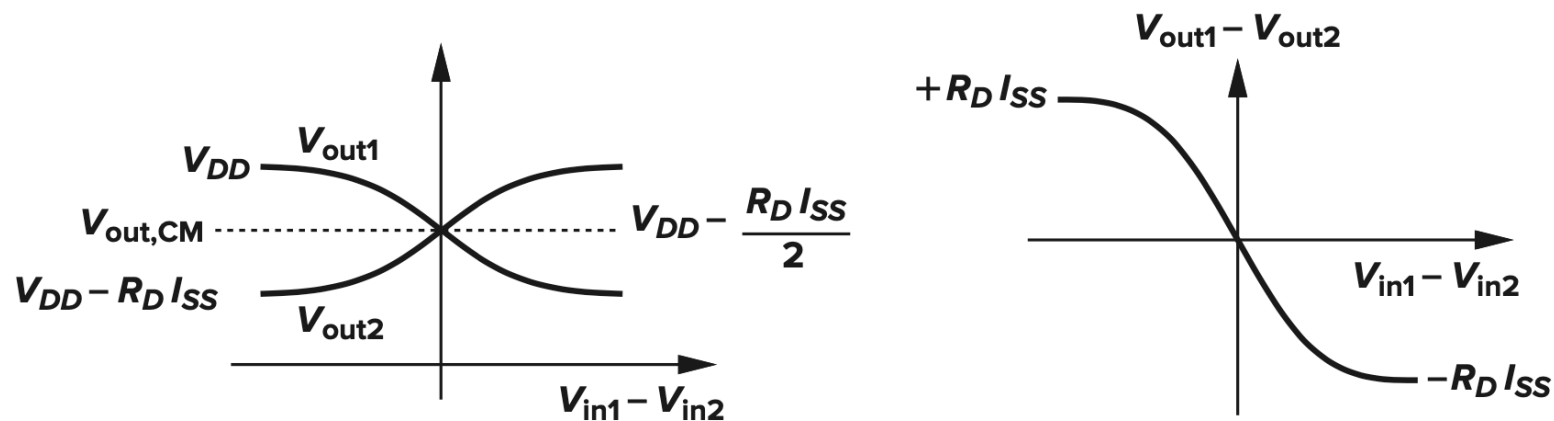


Differential input-output characteristics

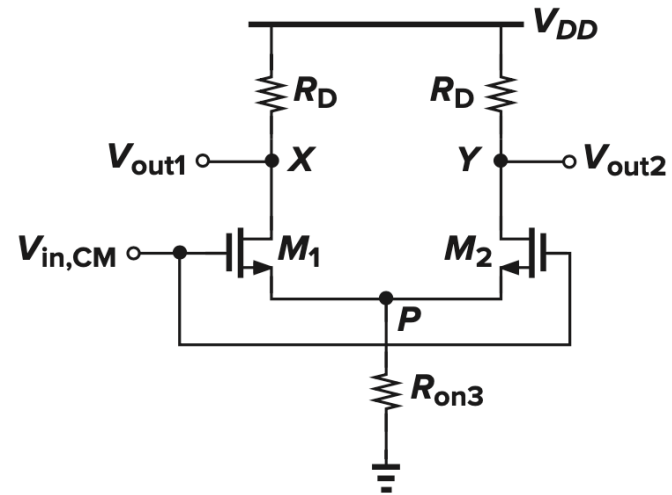
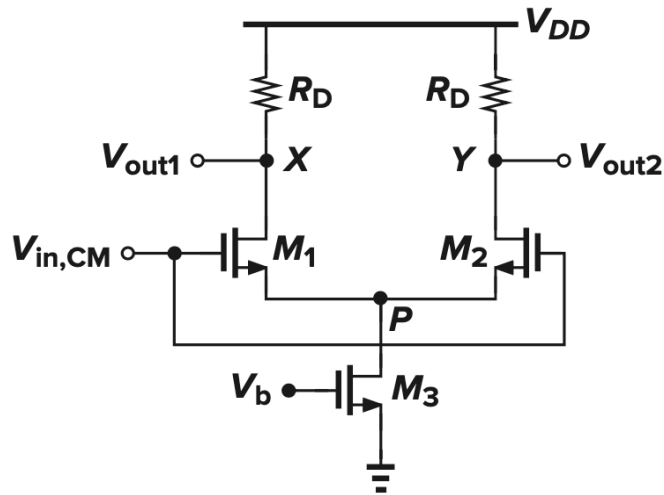
(neglecting channel-length modulation and body effect):



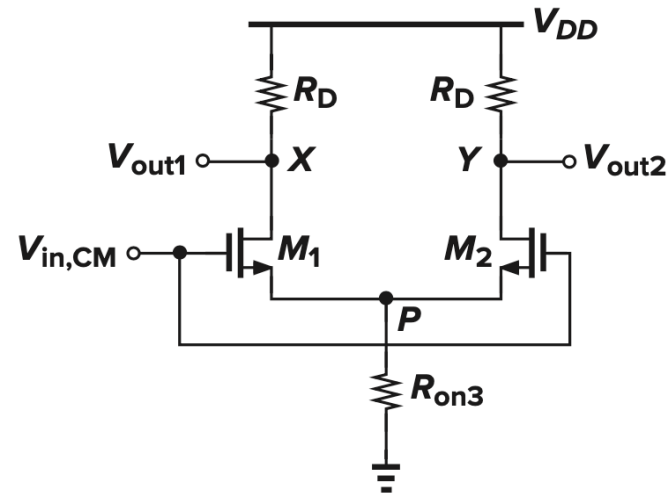
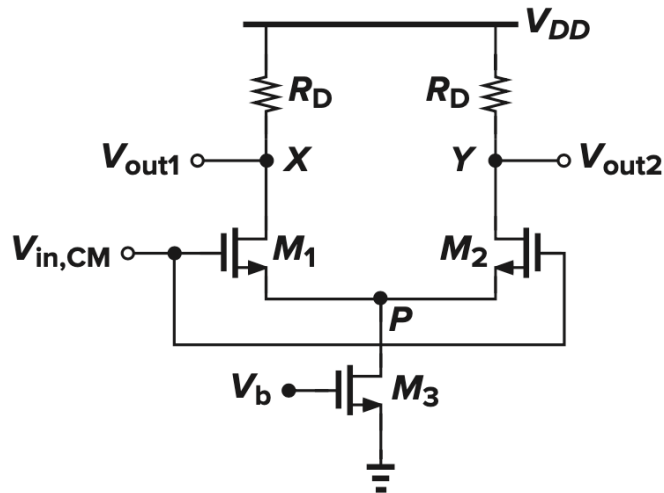
Differential input-output characteristics of a diff pair



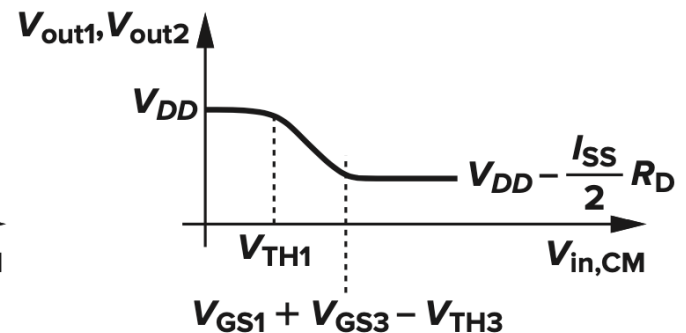
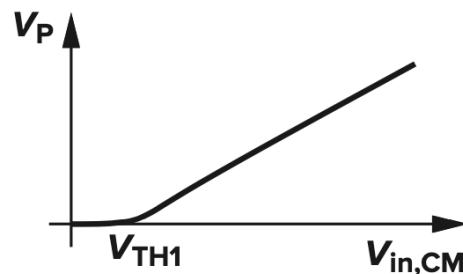
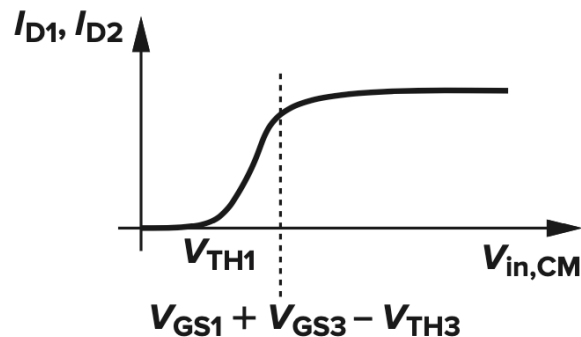
Common-mode input-output characteristics



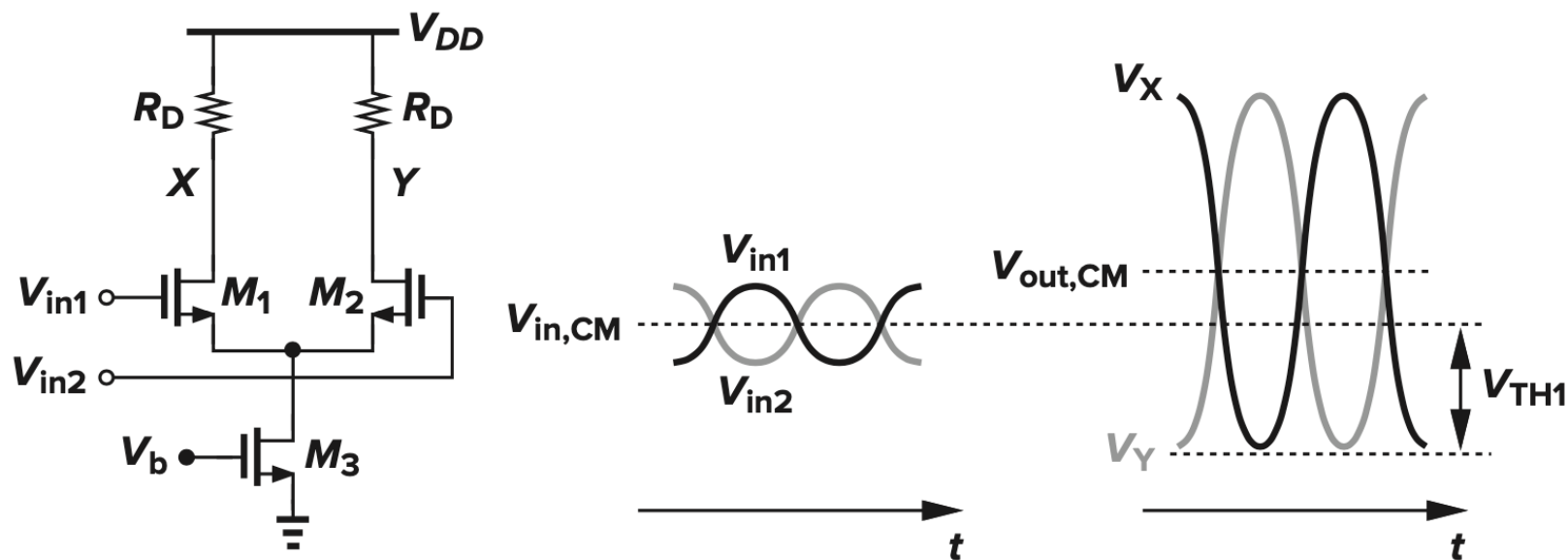
Common-mode input-output characteristics



$$V_{GS1} + (V_{GS3} - V_{TH3}) \leq V_{in,CM} \leq \min \left[V_{DD} - R_D \frac{I_{SS}}{2} + V_{TH}, V_{DD} \right]$$



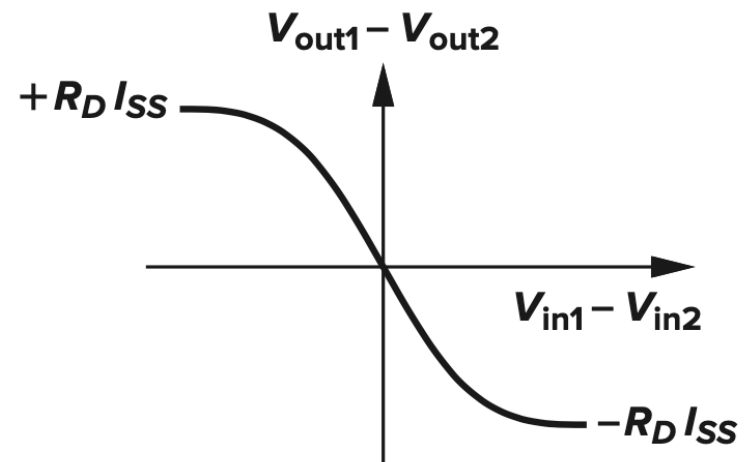
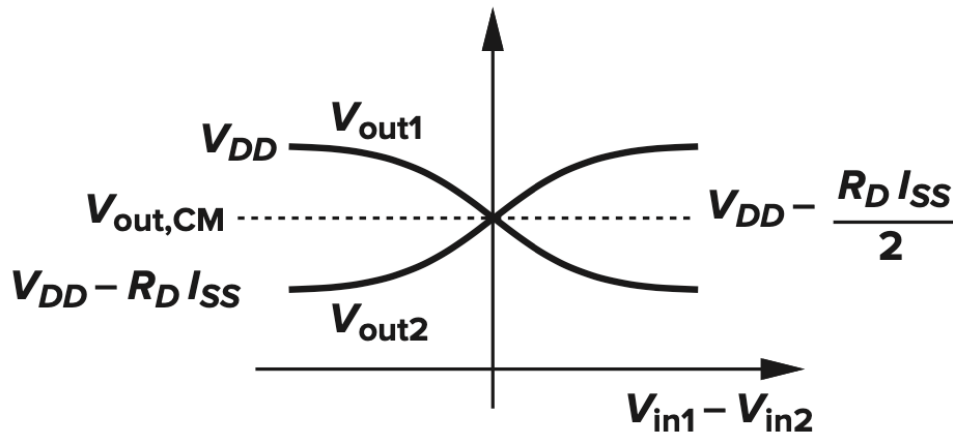
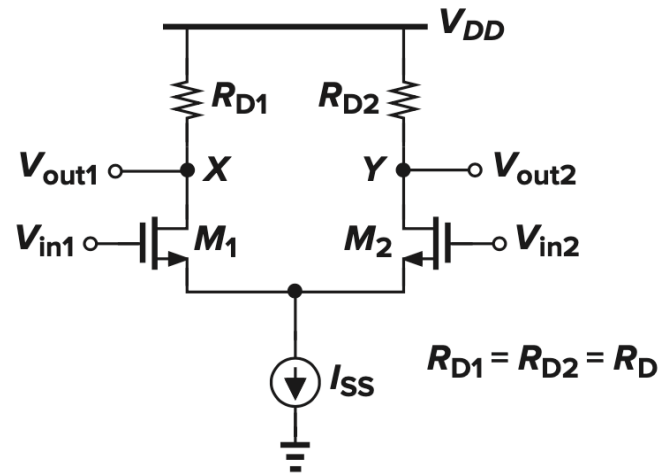
Maximum output swing



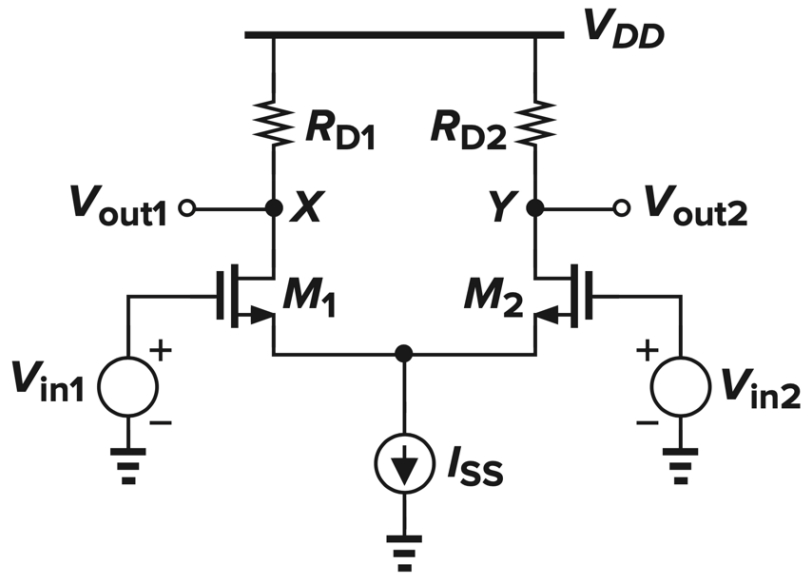
Single-ended peak-to-peak output swing:

$$V_{DD} - (V_{GS1} - V_{TH1}) - (V_{GS3} - V_{TH3})$$

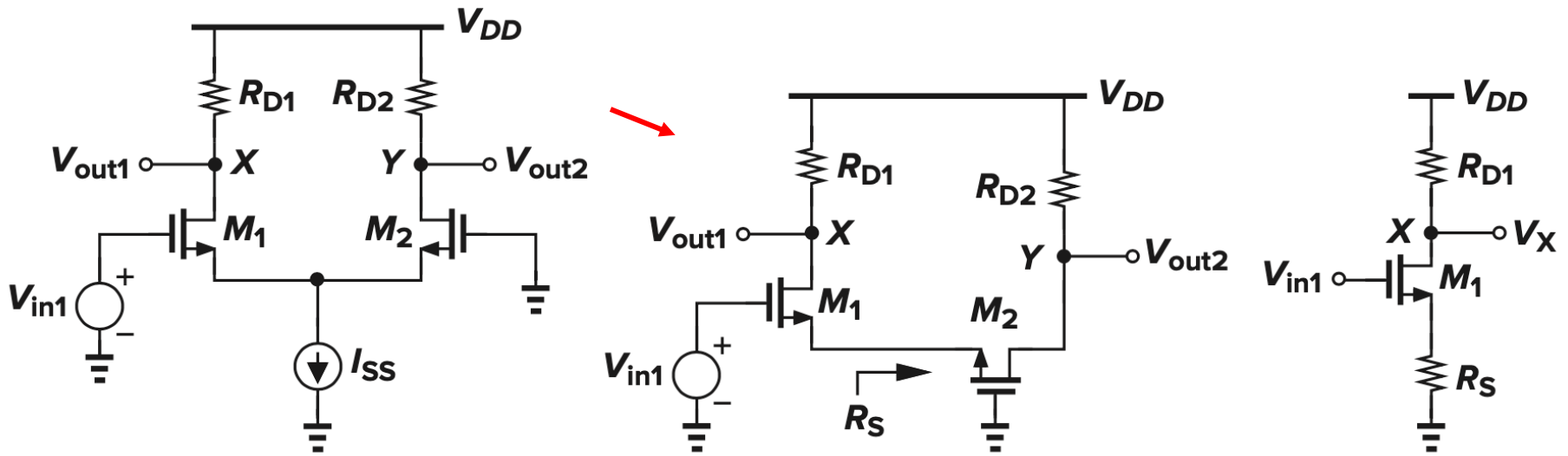
Large signal analysis



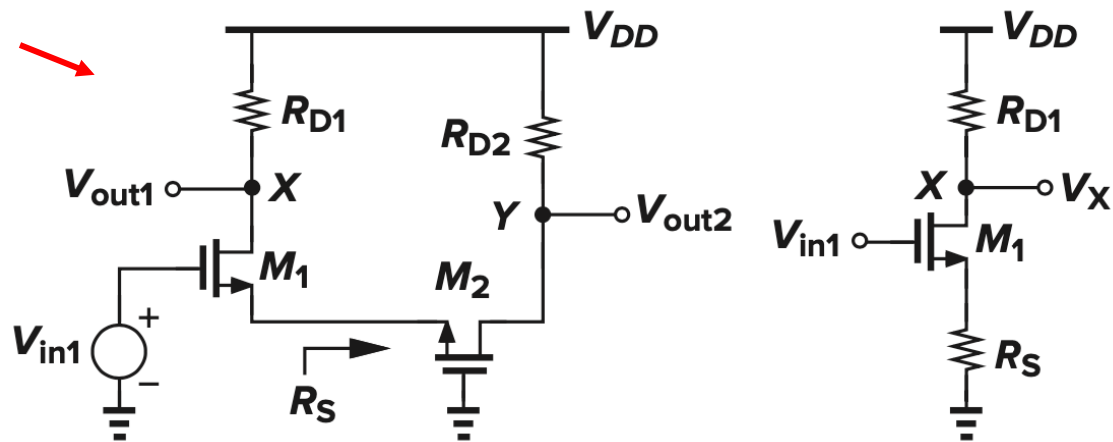
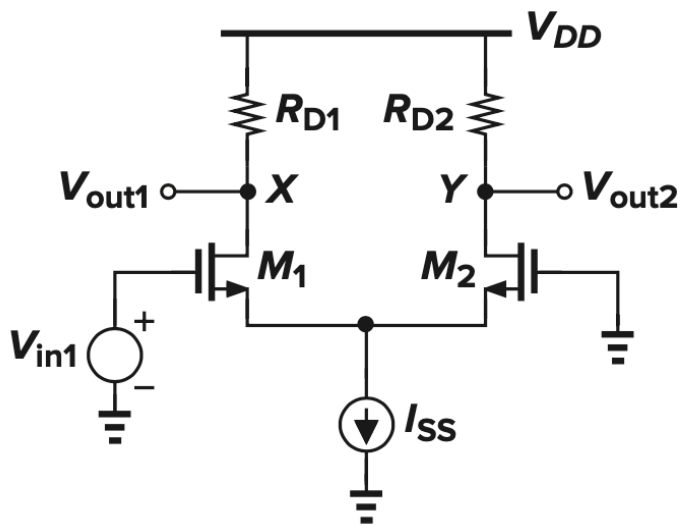
Small-signal analysis: gain



Small-signal analysis: gain (method 1)



Small-signal analysis: gain (method 1)

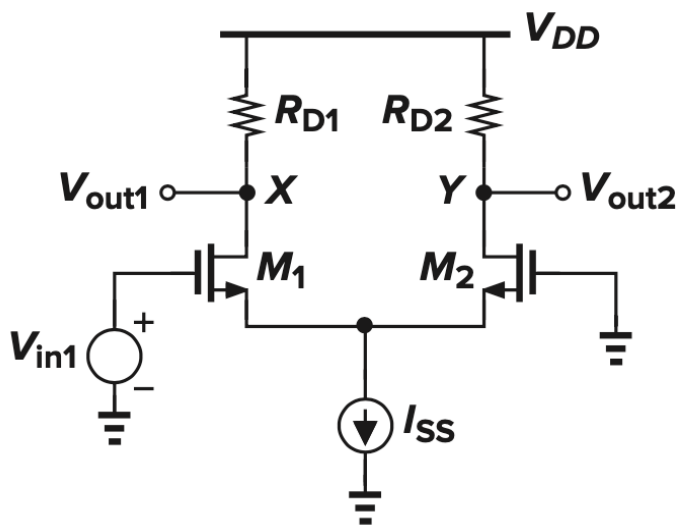


$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

$$\rightarrow (V_X - V_Y)|_{\text{Due to } V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

Small-signal analysis: gain (method 1)

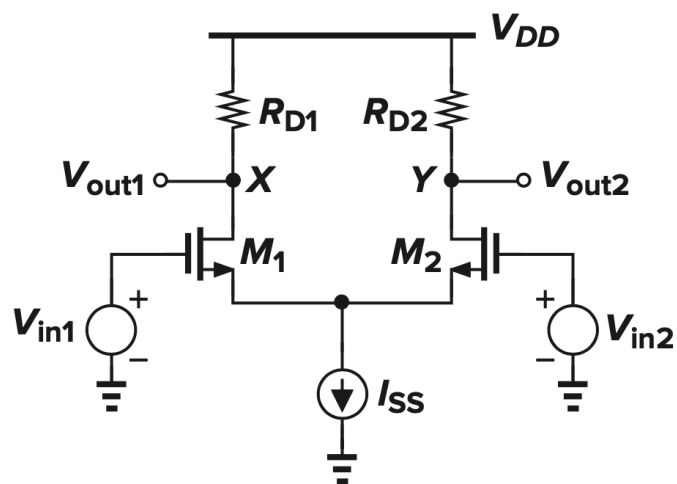


$$(V_X - V_Y)|_{\text{Due to } V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

$$g_{m1} = g_{m2} = g_m \quad \downarrow$$

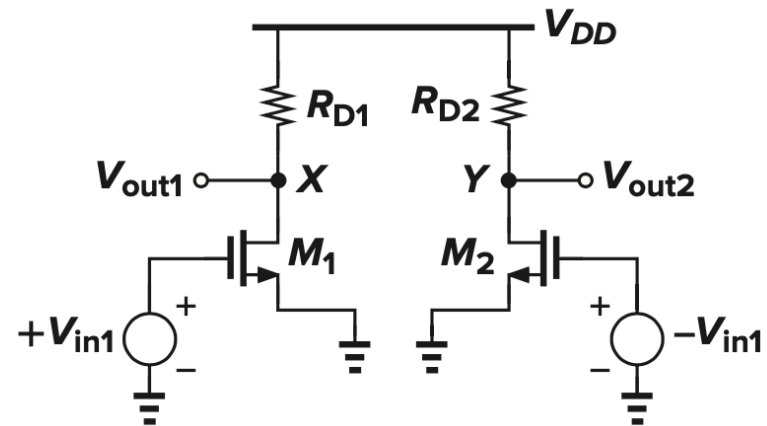
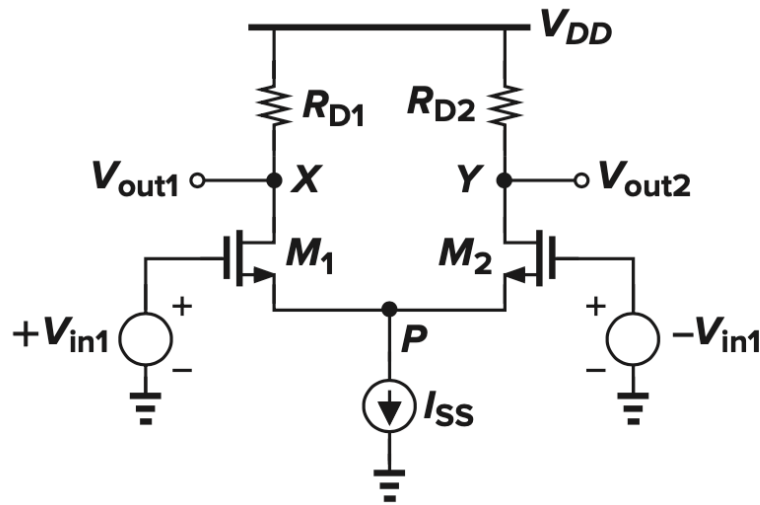
$$(V_X - V_Y)|_{\text{Due to } V_{in1}} = -g_m R_D V_{in1}$$

$$(V_X - V_Y)|_{\text{Due to } V_{in2}} = g_m R_D V_{in2}$$



$$\boxed{\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D}$$

Small-signal gain with half-circuit model (method 2)



- ✓ If a **fully-symmetric differential pair** senses **differential inputs** (i.e., the two inputs change by equal and opposite amounts from the equilibrium condition), then the concept of “**half circuit**” can be applied

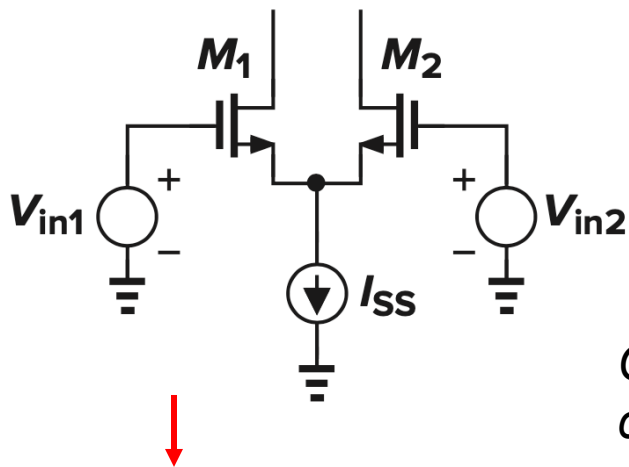
$$V_X / V_{in1} = -g_m R_D$$

$$V_Y / (-V_{in1}) = -g_m R_D$$

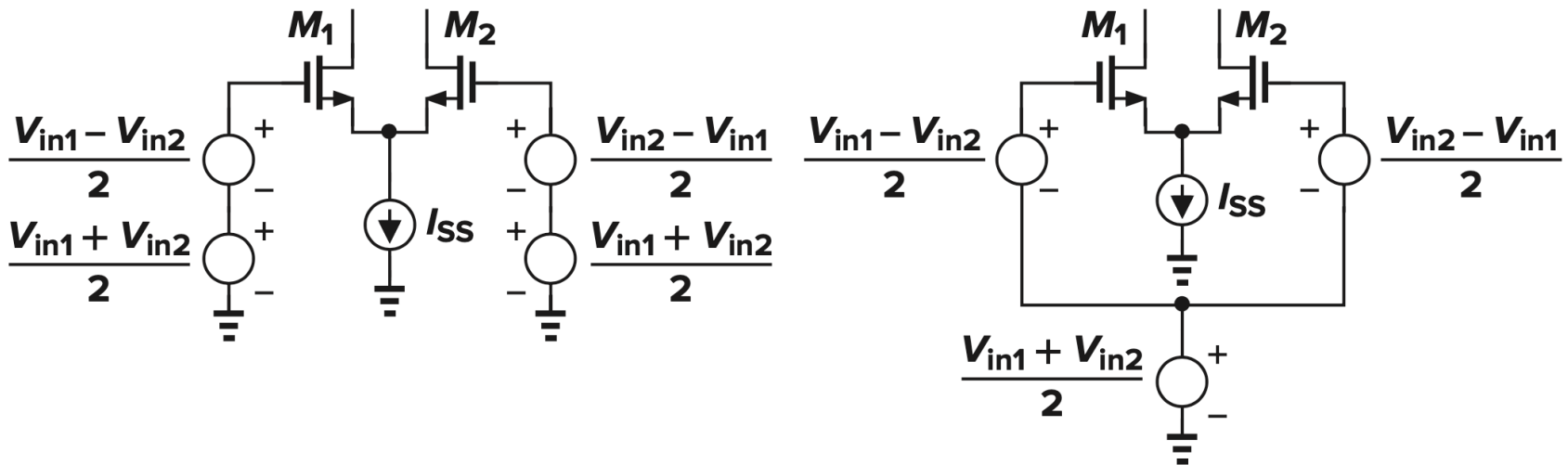


$$(V_X - V_Y) / (2V_{in1}) = -g_m R_D$$

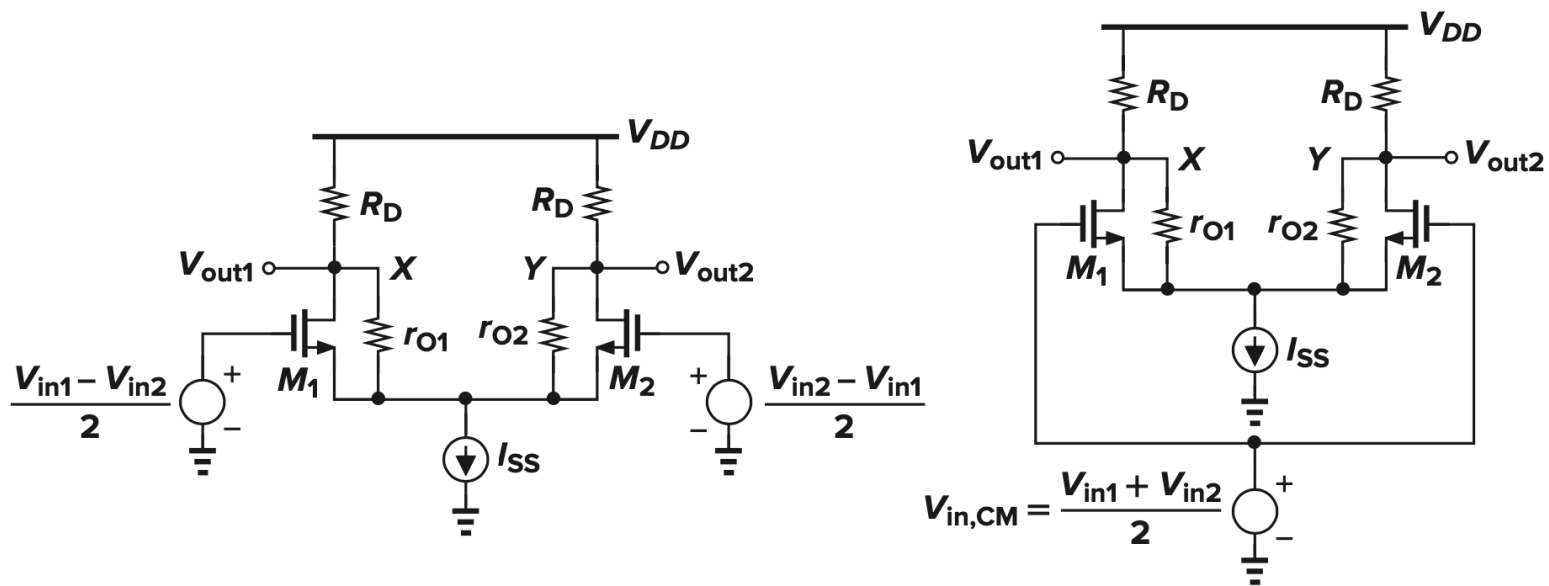
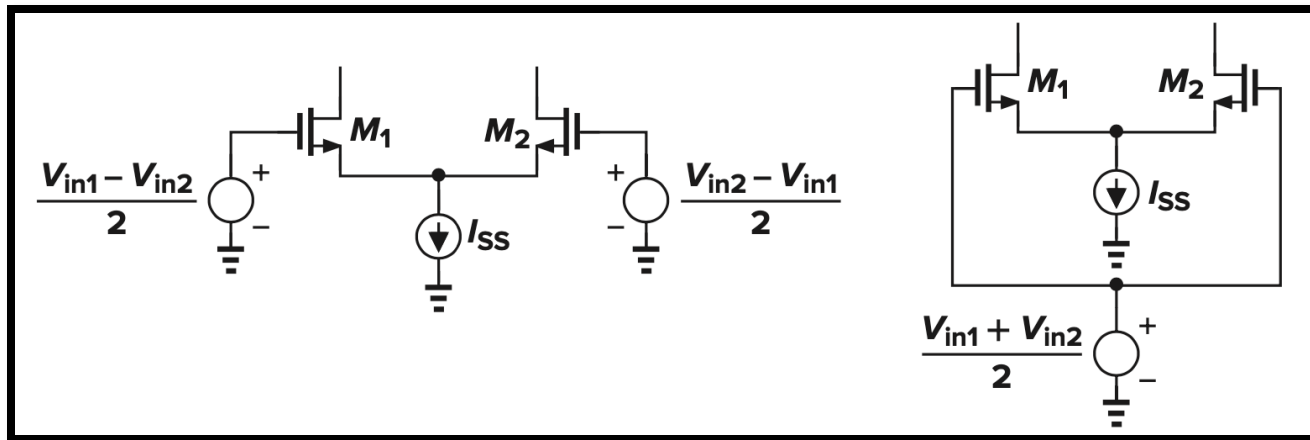
Half-circuit model for non-differential inputs



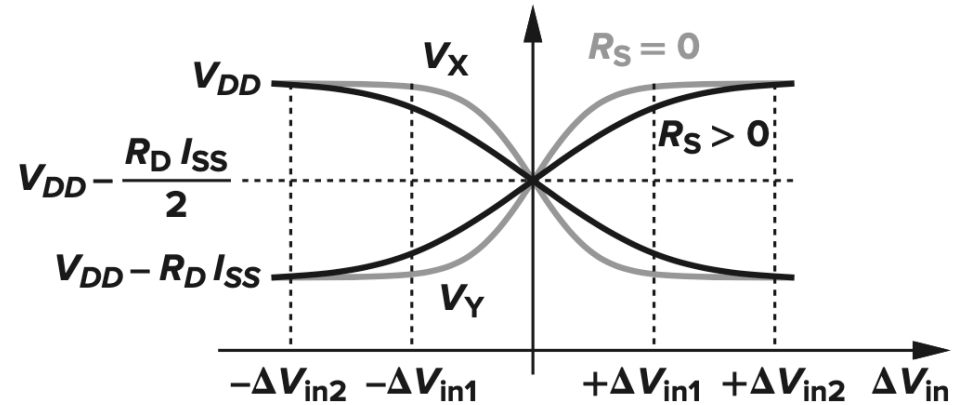
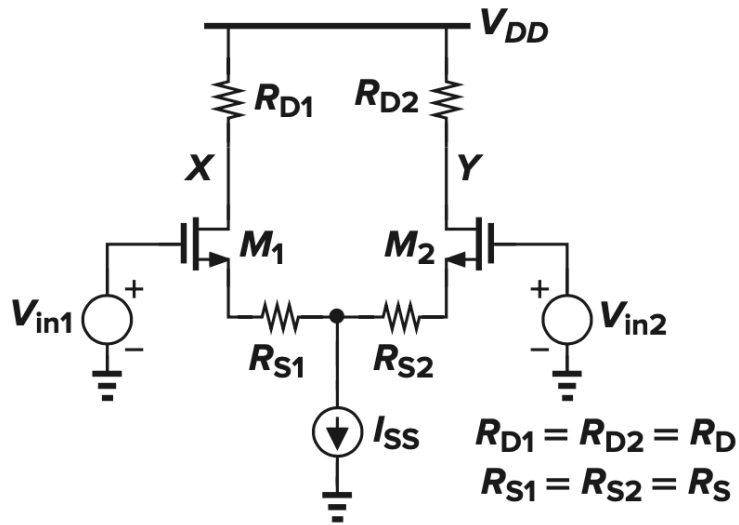
Conversion of arbitrary inputs to differential and common-mode components



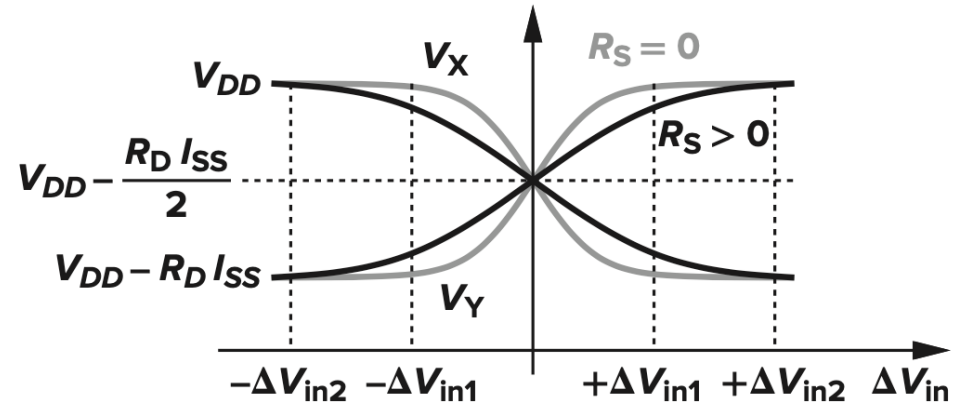
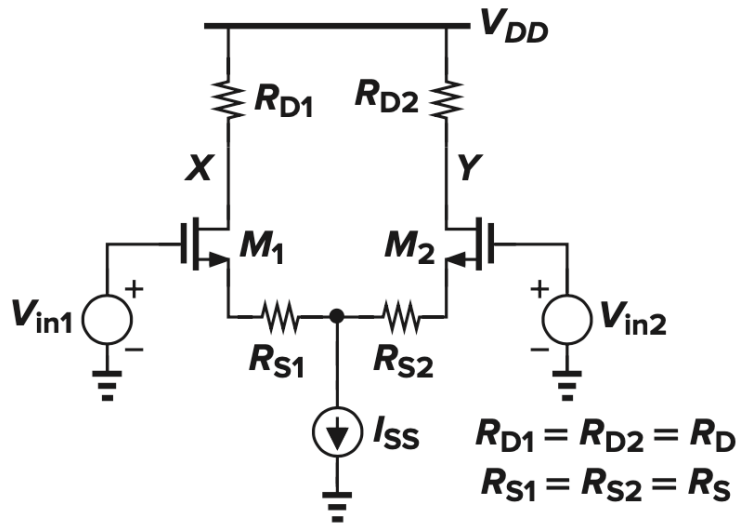
Half-circuit model for non-differential inputs



Degenerated differential pair for improved linearity



Degenerated differential pair for improved linearity



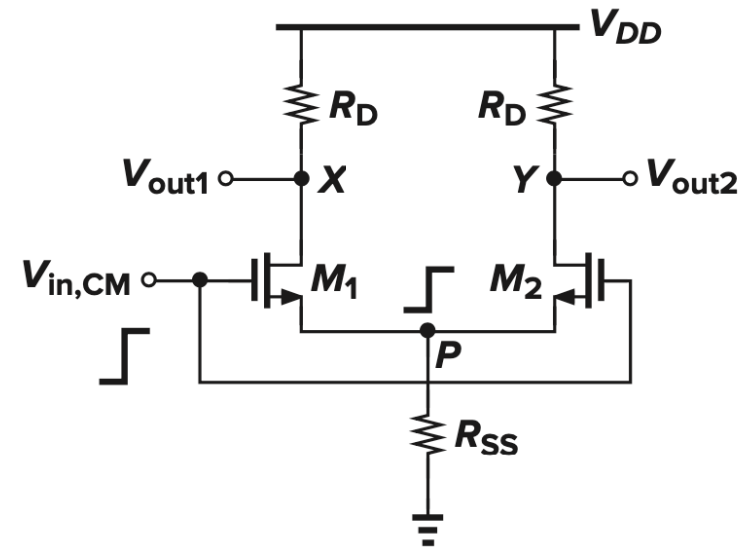
half-circuit:

$$|A_v| = \frac{R_D}{\frac{1}{g_m} + R_S}$$

✓ the circuit trades **gain** for **linearity**

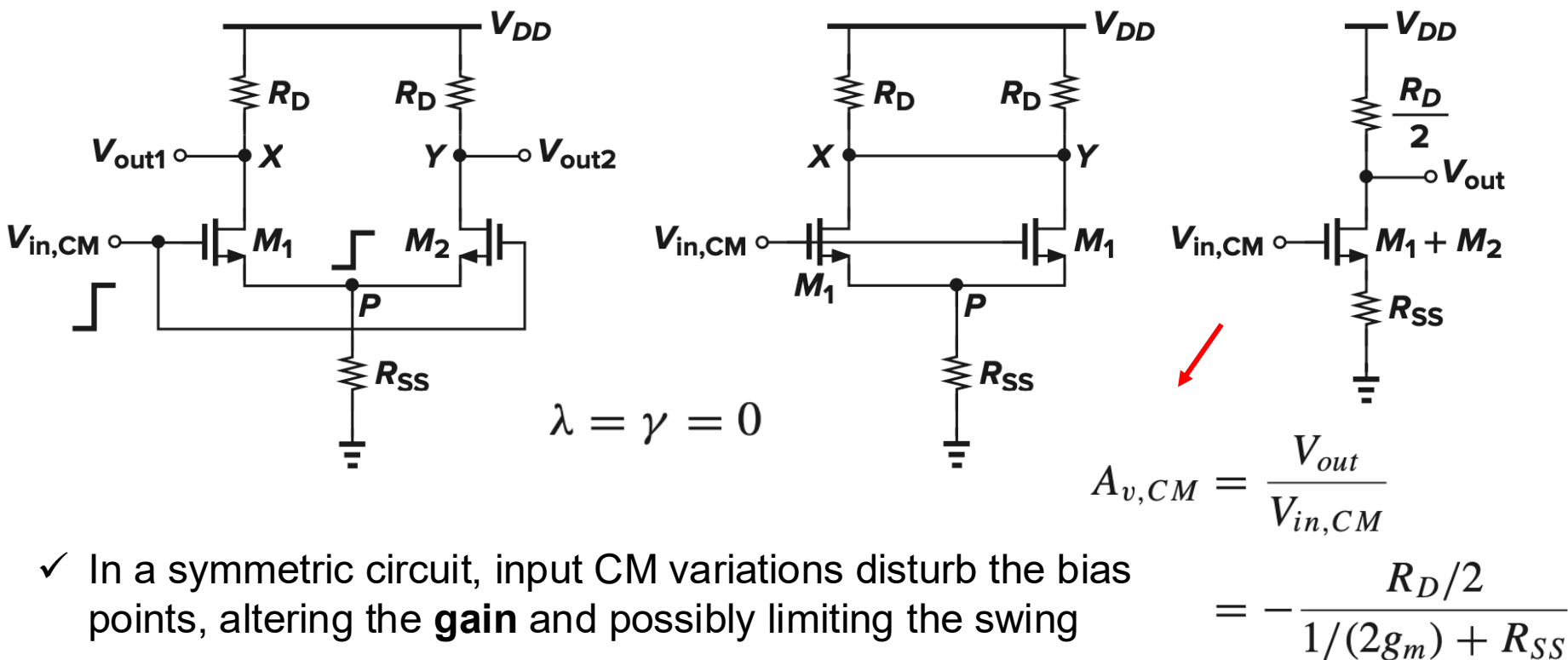
Common-mode response

- An important advantage of differential amplifiers is their ability to **suppress the effect of common-mode** perturbations
 - In reality, the circuit is not fully symmetric nor does the current source exhibit an infinite output impedance
 - As a result, a fraction of the input CM variation appears at the output



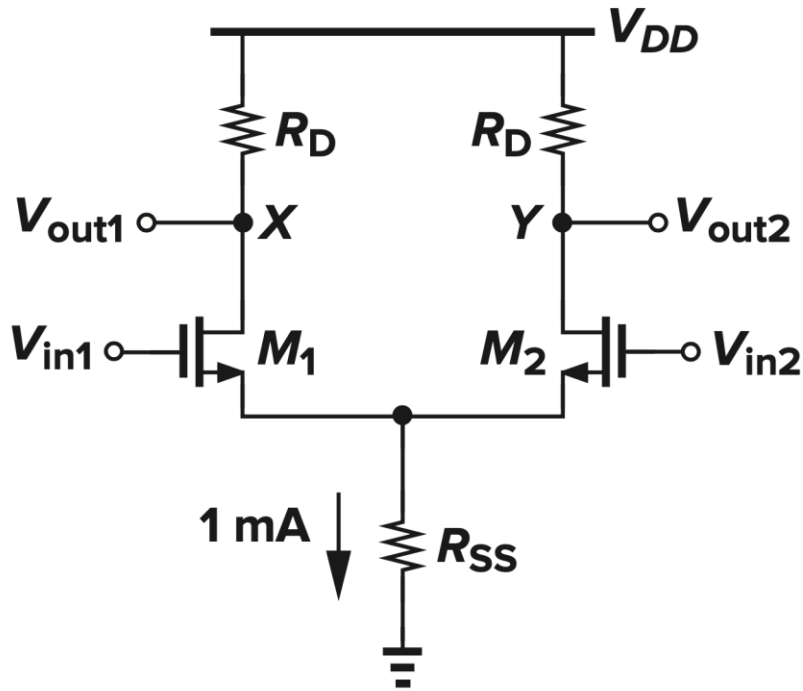
Common-mode response

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 - In reality, the circuit is not fully symmetric nor does the current source exhibit an infinite output impedance
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- ✓ In a symmetric circuit, input CM variations disturb the bias points, altering the **gain** and possibly limiting the swing

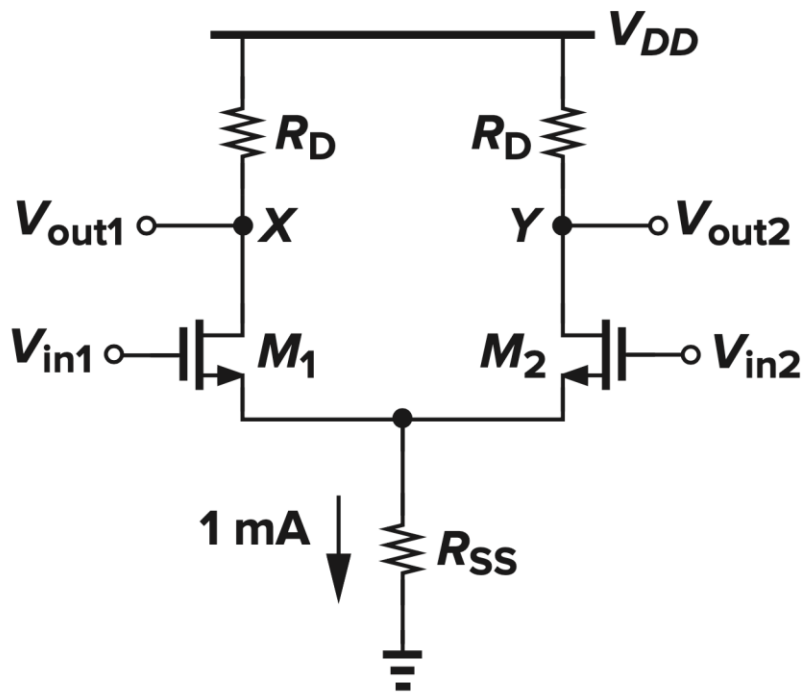
Example



Assume that $(W/L)_{1,2}=25/0.5$, $\mu_n C_{ox}=50\mu\text{A/V}^2$, $V_{TH}=0.6\text{V}$, $\lambda=\gamma=0$, and $V_{DD}=3\text{V}$.

- ❖ What is the required input CM voltage for which R_{SS} sustains 0.5V ?
- ❖ Calculate R_D for a differential gain of 5.
- ❖ What happens at the output if the input CM level is 50 mV higher than the value calculated above?

Example



$$I_{D1} = I_{D2} = 0.5 \text{ mA}$$



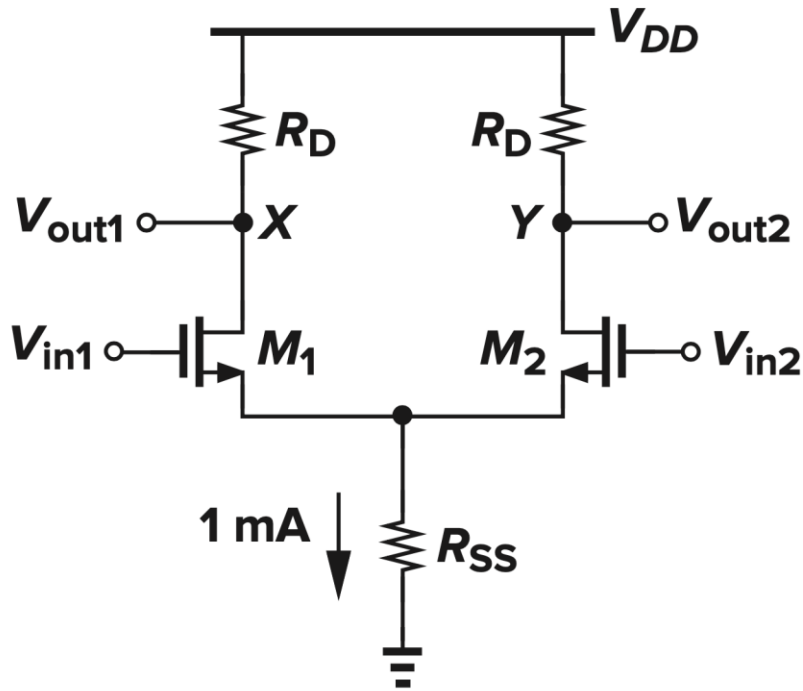
$$V_{GS1} = V_{GS2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} + V_{TH}$$
$$= 1.23 \text{ V}$$

$$V_{in,CM} = V_{GS1} + 0.5 \text{ V} = 1.73 \text{ V}$$

Assume that $(W/L)_{1,2}=25/0.5$, $\mu_n C_{ox}=50\mu\text{A/V}^2$, $V_{TH}=0.6\text{V}$, $\lambda=\gamma=0$, and $V_{DD}=3\text{V}$.

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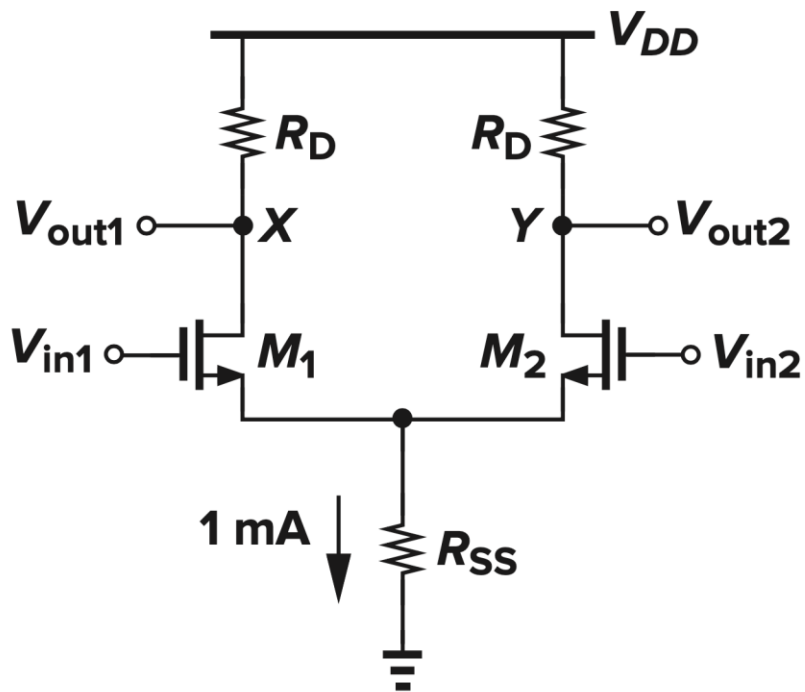


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$$g_m = \sqrt{2\mu_n C_{ox} (W/L) I_{D1}} = 1/(632 \Omega) \quad \rightarrow \quad R_D = 3.16 \text{ k}\Omega$$

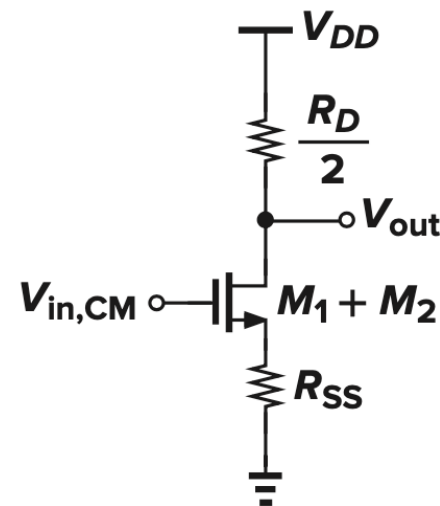
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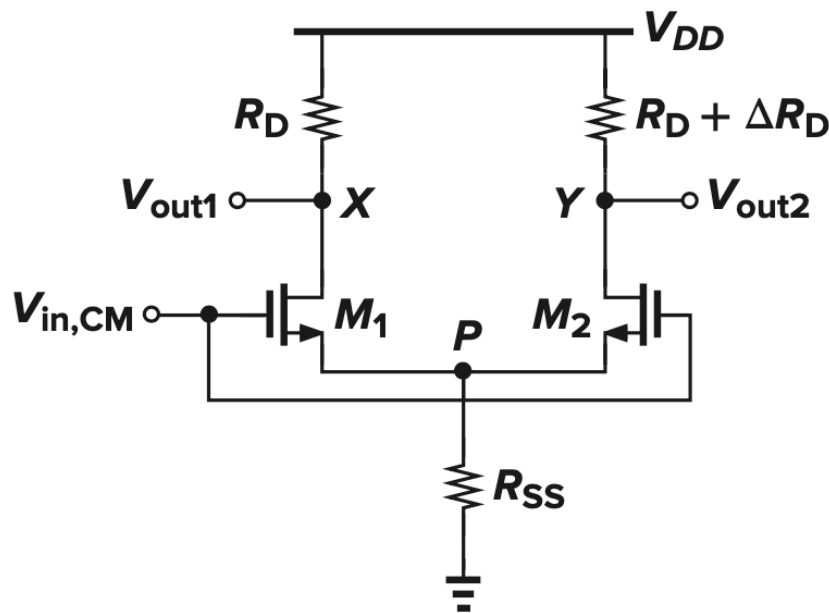
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- ❖ Calculate R_D for a differential gain of 5.
- ❖ What happens at the output if the input CM level is 50 mV higher than the value calculated above?

$$\begin{aligned}
 |\Delta V_{X,Y}| &= \Delta V_{in,CM} \frac{R_D/2}{R_{SS} + 1/(2g_m)} \\
 &= 50 \text{ mV} \times 1.94 \\
 &= 96.8 \text{ mV}
 \end{aligned}$$



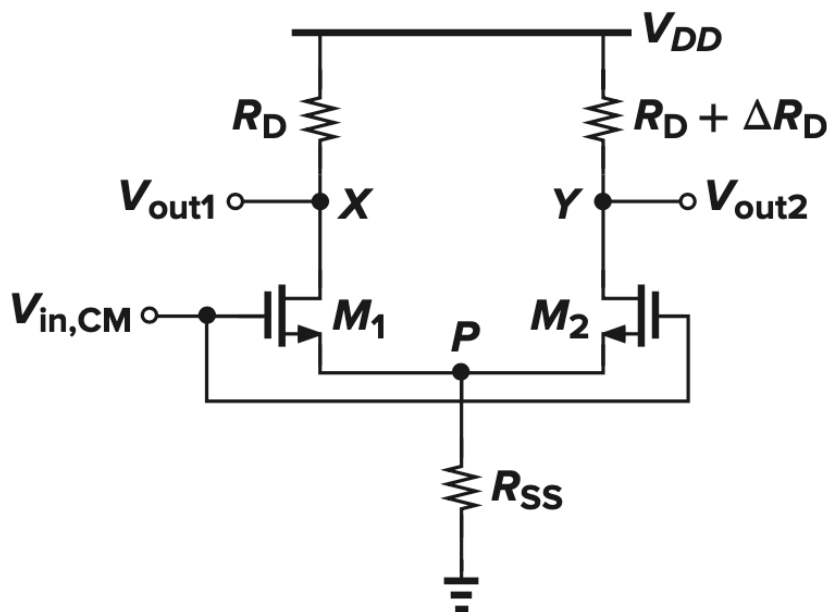
Common-mode response

- The **finite output impedance** of the tail current source results in some **CM gain** in a symmetric differential pair: usually a **minor** concern
- More troublesome: variation of **differential output** as a result of a change in **CM input**, due to **asymmetry (mismatches)** of two sides during manufacturing



Common-mode response

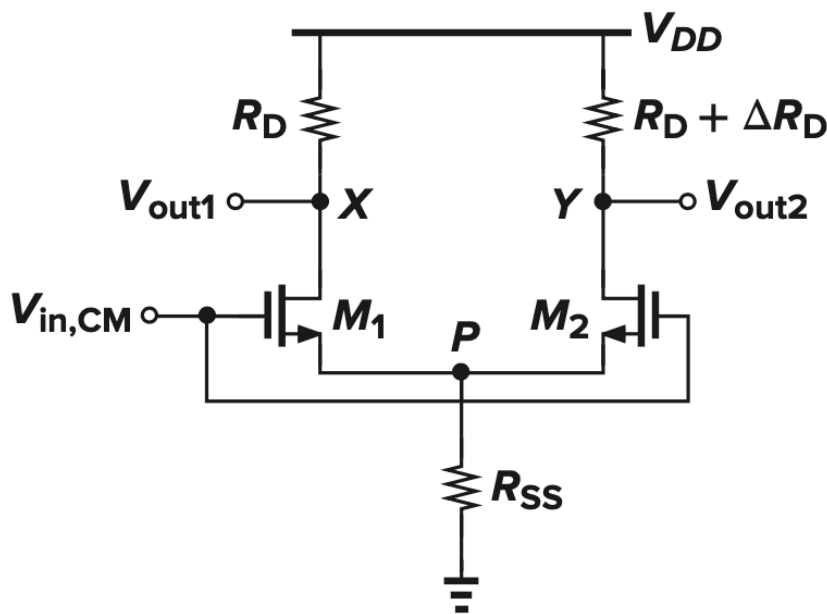
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$$\Delta V_P = \frac{R_{SS}}{R_{SS} + \frac{1}{2g_m}} \Delta V_{in,CM}$$

Common-mode response

- The **finite output impedance** of the tail current source results in some **CM gain** in a symmetric differential pair: usually a **minor** concern
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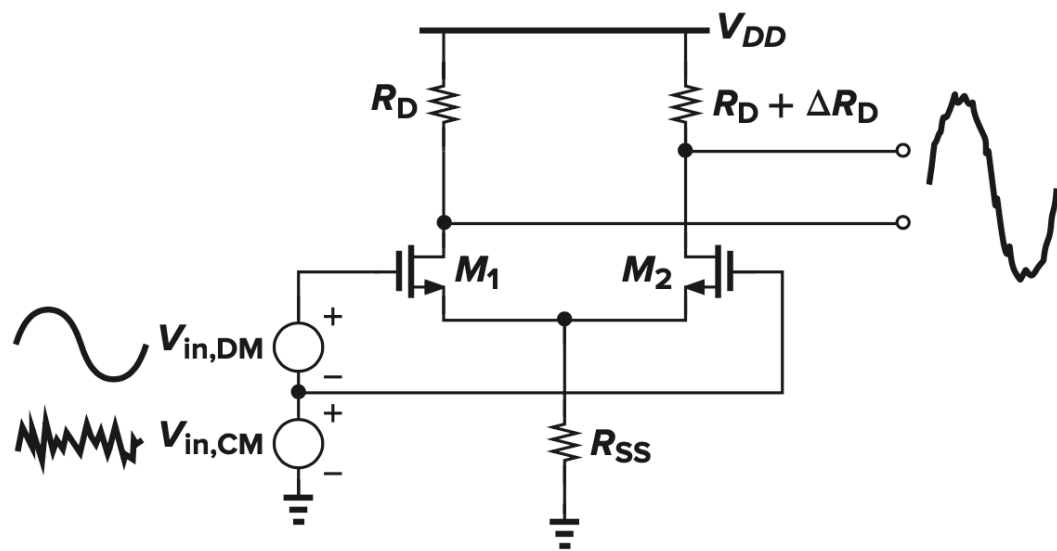


$$\Delta V_P = \frac{R_{SS}}{R_{SS} + \frac{1}{2g_m}} \Delta V_{in,CM}$$

$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D$$

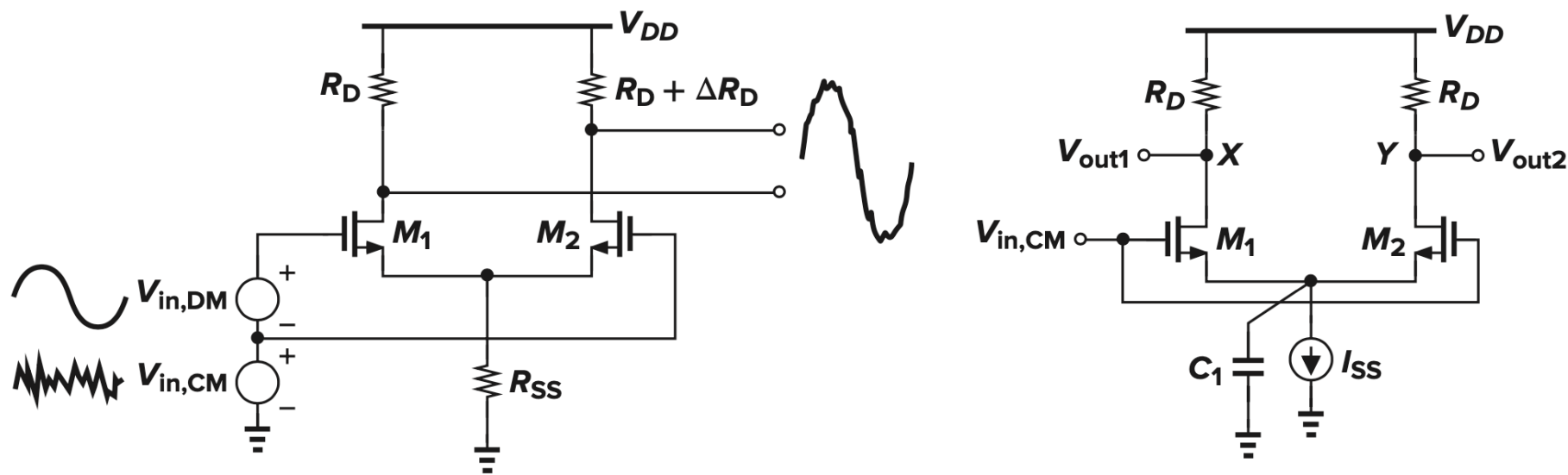
$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D)$$

CM noise in the presence of resistor mismatch



- The common-mode response of differential pairs depends on the **output impedance** of the tail current source and **asymmetries** in the circuit
- Two effects: variation of the **output CM** level (in the absence of mismatch) and **conversion** of input CM variations to **differential** components at the output
- The latter effect is much more severe, so the CM response should be studied with **mismatches** taken into account

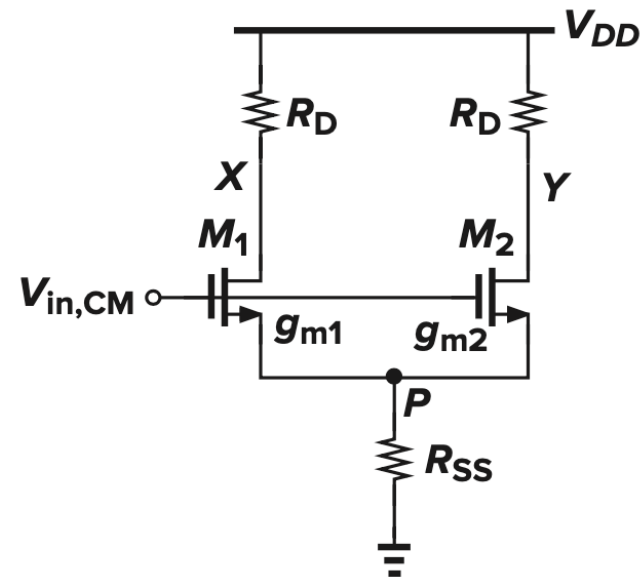
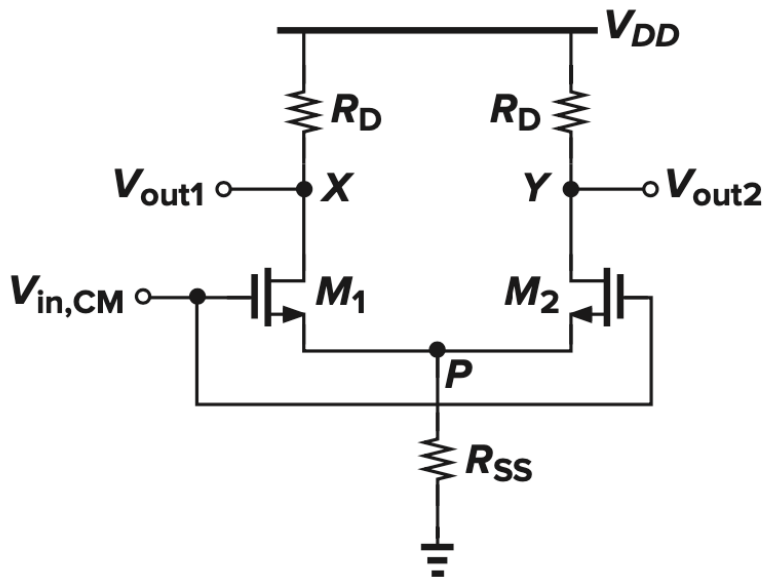
CM noise in the presence of resistor mismatch



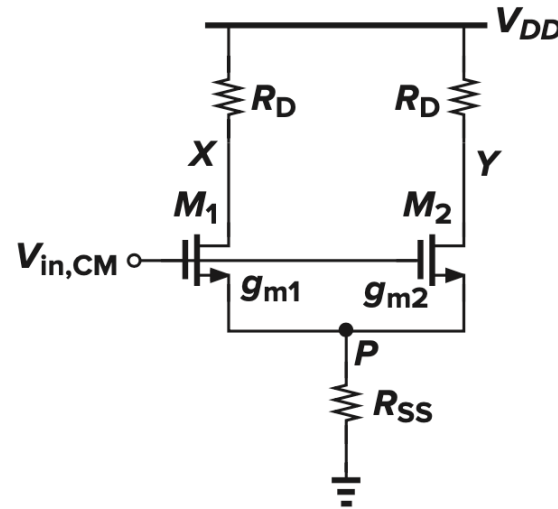
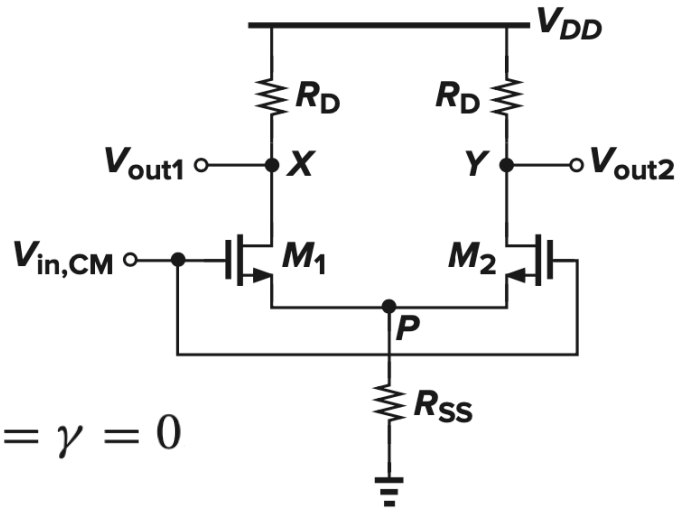
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Common-mode response with input pair mismatch

- The asymmetry in the circuit comes from both the **load resistors** and the **input transistors**, the latter contributing a typically **much greater mismatch**
- Due to **dimension** and **threshold** voltage mismatches, the two transistors carry slightly **different currents** and have **unequal g_m**



Common-mode response with input pair mismatch

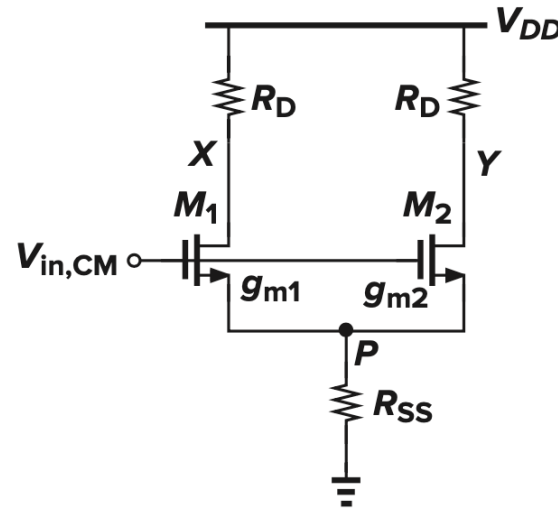
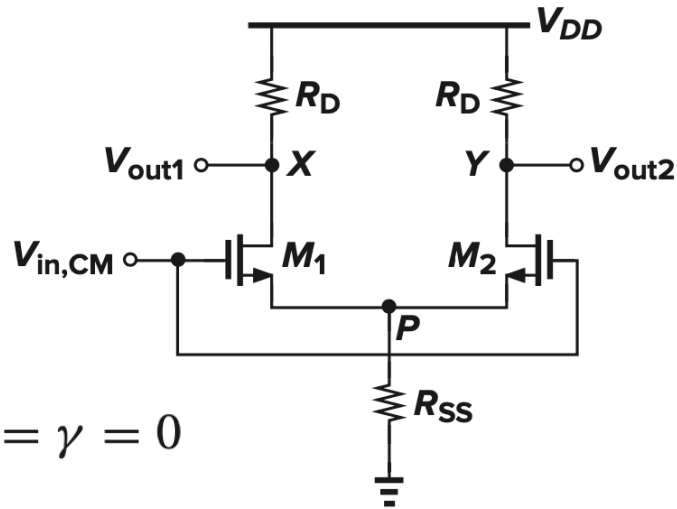


$$\lambda = \gamma = 0$$

$$(g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS} = V_P$$

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}$$

Common-mode response with input pair mismatch



$$(g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS} = V_P$$

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}$$



$$\begin{aligned} V_X &= -g_{m1}(V_{in,CM} - V_P)R_D \\ &= \frac{-g_{m1}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \end{aligned}$$

$$V_Y = -g_{m2}(V_{in,CM} - V_P)R_D$$

$$= \frac{-g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM}$$

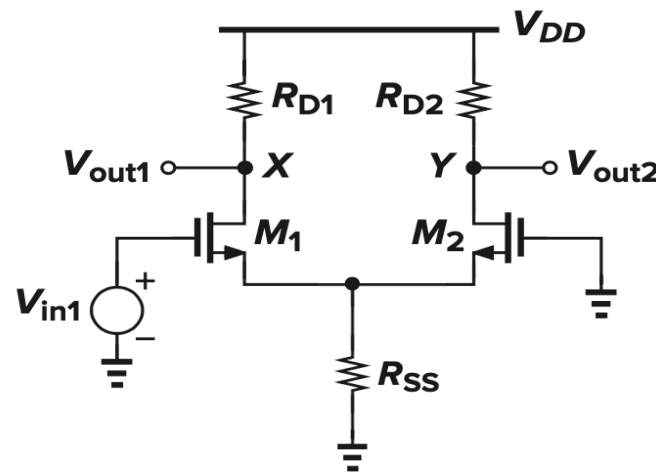
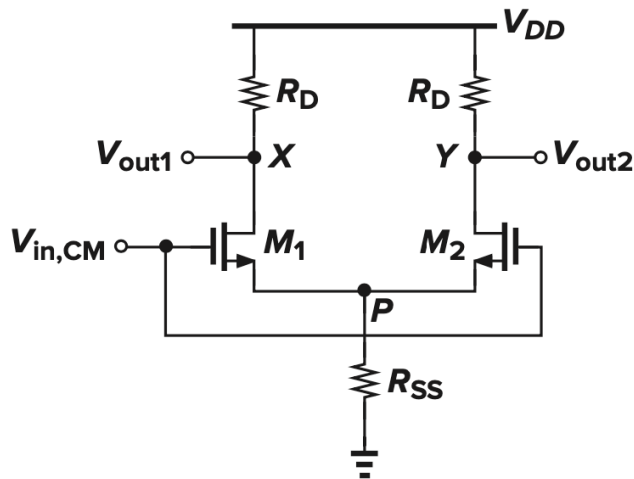
$$V_X - V_Y = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM}$$

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2})R_{SS} + 1}$$

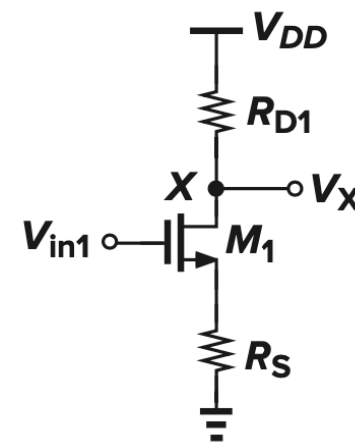
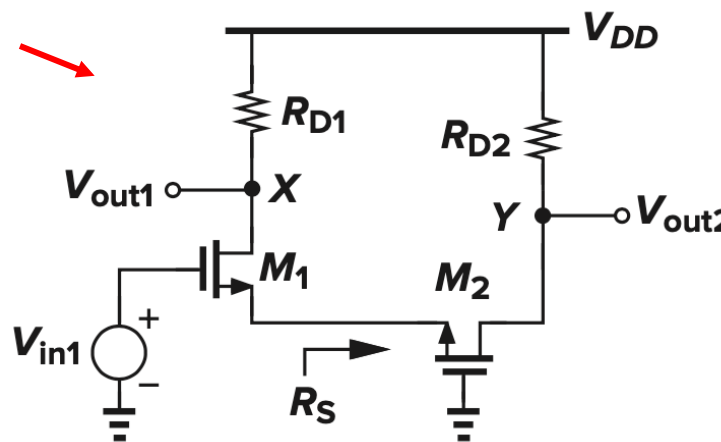
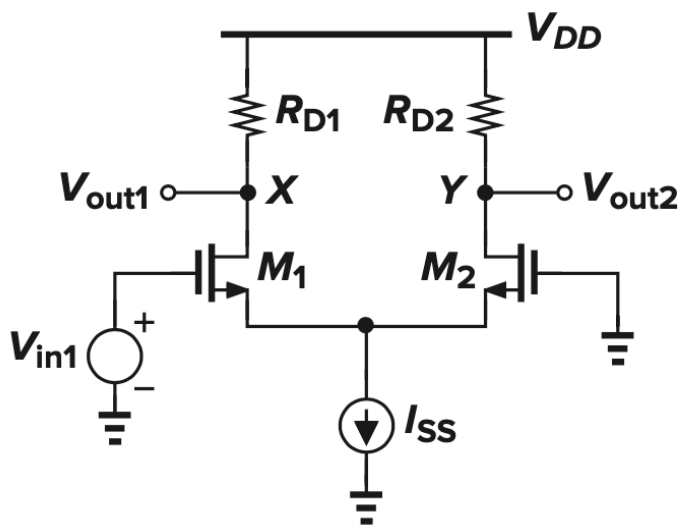
CMRR: common-mode rejection ratio

- For a meaningful comparison of differential circuits, the **undesirable differential component produced by CM variations** must be normalized to the **wanted differential output resulting from amplification**
 - “Common-mode rejection ratio” (**CMRR**) defined as the desired gain divided by the undesired gain

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$



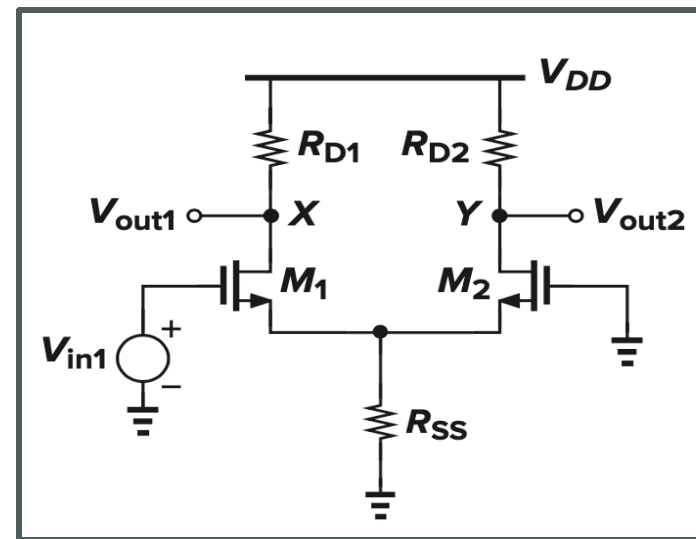
CMRR? Recall: differential gain



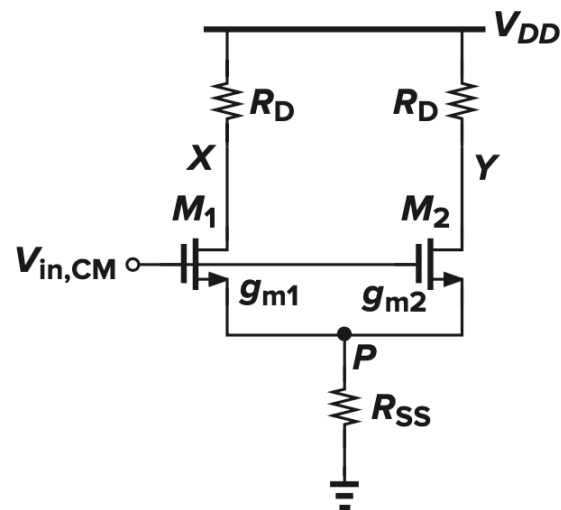
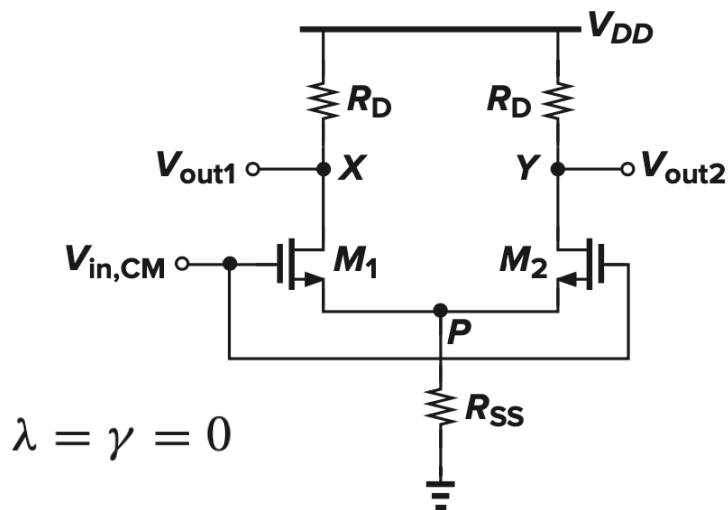
$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}$$



CMRR? Recall: common-mode gain



$$A_{CM-DM} = - \frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) R_{SS} + 1}$$

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

$$\begin{aligned} \text{CMRR} &= \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} \\ &\approx \frac{g_m}{\Delta g_m} (1 + 2g_m R_{SS}) \end{aligned}$$

$$g_m = (g_{m1} + g_{m2})/2 \quad \Delta g_m = g_{m1} - g_{m2}$$

$$2g_m R_{SS} \gg 1$$



$$\text{CMRR} \approx 2g_m^2 R_{SS} / \Delta g_m$$

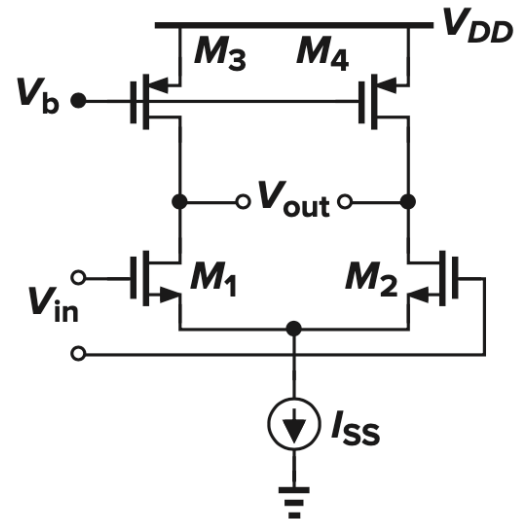
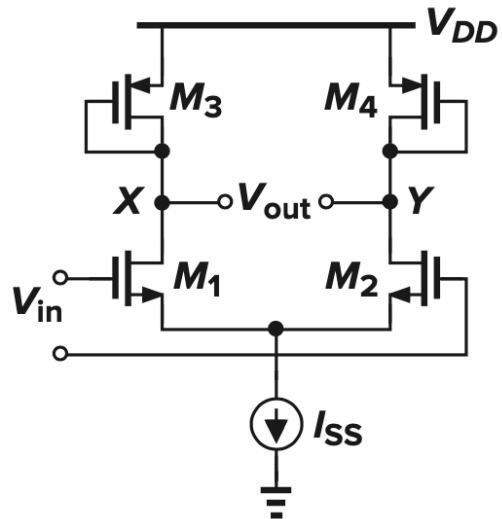
$$= \frac{2g_m R_{SS}}{\left(\frac{\Delta g_m}{g_m} \right)}$$

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

$$\text{in dB: } \text{CMRR}(dB) \equiv 20 \log \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

CMRR should be as large as possible

Differential Pair with MOS Loads



$$A_v = -g_{mN} (g_{mP}^{-1} \parallel r_{ON} \parallel r_{OP})$$

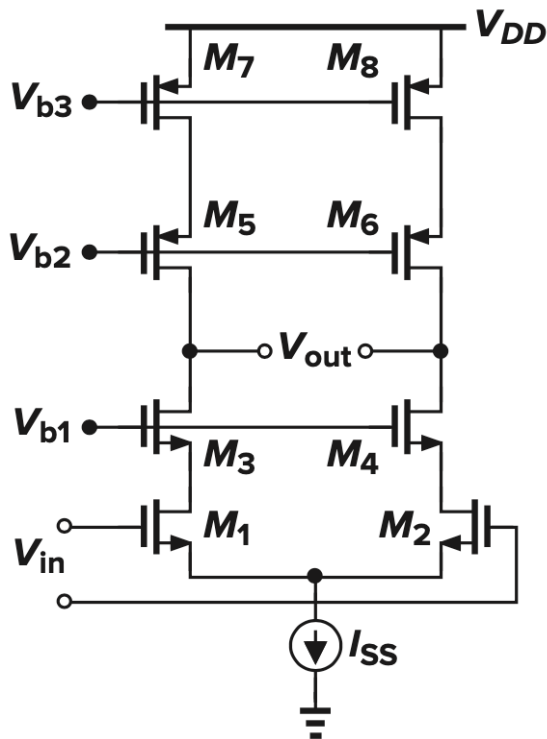
$$\approx -\frac{g_{mN}}{g_{mP}}$$

$$A_v = -g_{mN} (r_{ON} \parallel r_{OP})$$

$$A_v \approx -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$

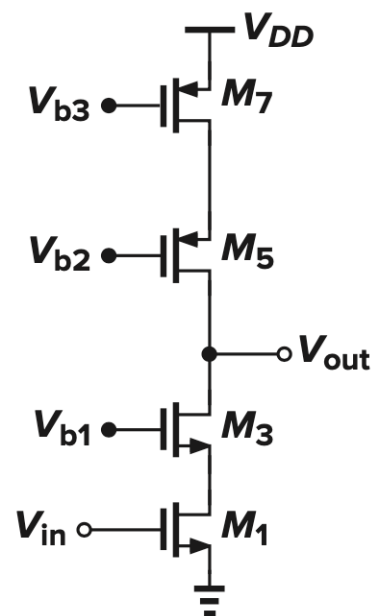
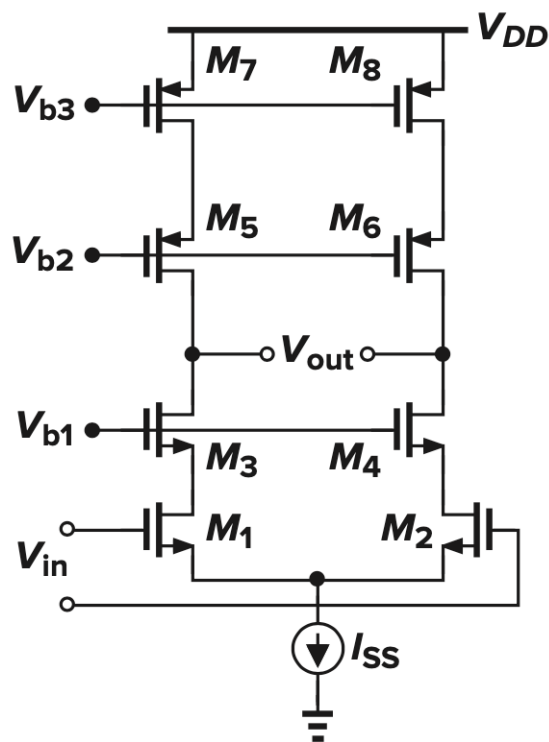
Cascode differential pair

- The gain of the differential pair with current-source loads relatively low, in the range of 5 to 10 in nanometer technologies
 - increase the output impedance of both PMOS and NMOS by **cas coding**



Cascode differential pair

- The gain of the differential pair with current-source loads relatively low, in the range of 5 to 10 in nanometer technologies
 - increase the output impedance of both PMOS and NMOS by **cas coding**
 - increases the differential **gain** at the cost of more **headroom**



$$|A_v| \approx g_{m1} [(g_{m3} r_{o3} r_{o1}) \parallel (g_{m5} r_{o5} r_{o7})]$$