

Analog IC design (EE-320), Lecture 7

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Institute of Electrical and Micro Engineering, School of Engineering, EPFL

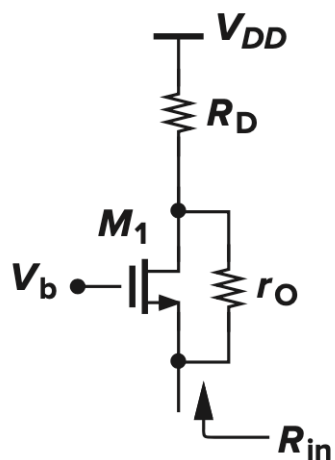
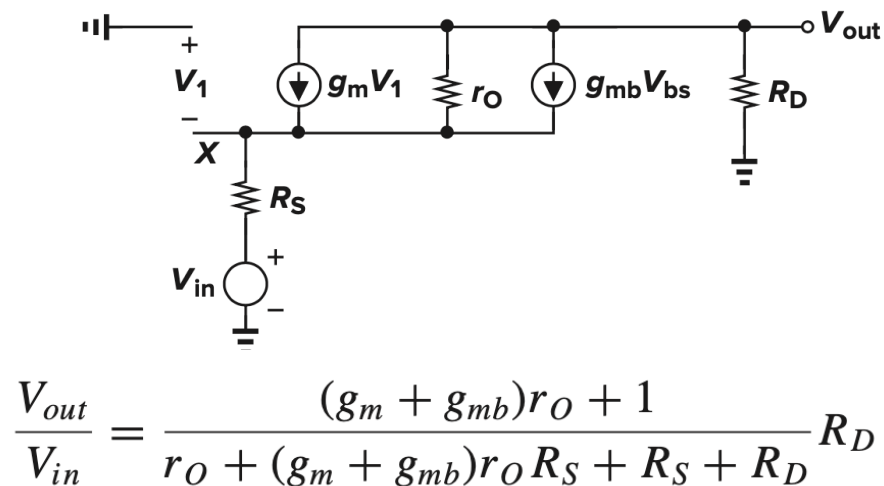
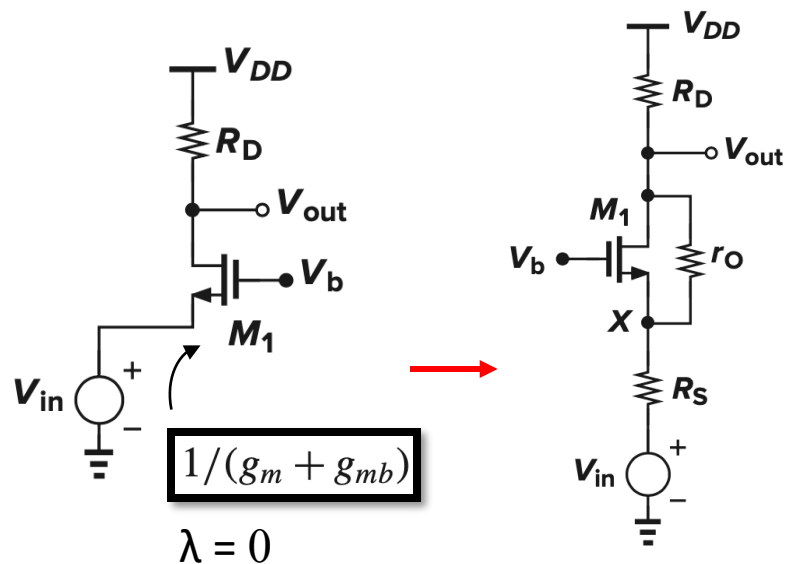
Homework 1, TP Schedule

- **Homework 1 assignment is due on Nov 12 at 20:00**
- **EDA statement assignment is due today**

- **The list of edauser IDs will be posted on moodle**
- **First TP session: Nov 10 in BC07-08 from 3:15pm to 6pm**

Week	Subject by week – EE-320: Analog IC design – Fall 2025	Suggested Chapters
Week 1: 08/09 – 14/09	Introduction, organization, review of MOS transistors + Exercise1	Ch 1, Ch 2.1-2.4, Slides on Moodle
Week 2: 15/09 – 21/09	MOS large and small-signal models, regimes of operations + Exercise2	Ch 2.1-2.4
Week 3: 22/09 – 28/09	Holiday – No class	
Week 4: 29/09 – 05/10	MOS parasitic effects, layout basic, single-stage amplifiers + Exercise3	Ch 2.1-2.4, Ch 3.1
Week 5: 06/10 – 12/10	Single-stage amplifiers + Exercise4	Ch 3.1-3.7
Week 6: 13/10 – 19/10	Single-stage amplifiers + Exercise5	Ch 3.1-3.7
Week 7: 20/10 – 26/10	Break – No class	
Week 8: 27/10 – 02/11	Single-stage amplifiers + Cascode + Exercise6 + Homework1	Ch 3.1-3.7
Week 9: 03/11 – 09/11	Differential amplifiers + Exercise7	Ch 4.1-4.4
Week 10: 10/11 – 16/11	TP1 Practical exercise session on Cadence	Tutorial on Moodle
Week 11: 17/11 – 23/11	TP2 Practical exercise session on Cadence	Tutorial on Moodle
Week 12: 24/11 – 30/12	TP3 Practical exercise session on Cadence + Homework2	Tutorial on Moodle
Week 13: 01/12 – 07/12	TP4 Practical exercise session on Cadence	Tutorial on Moodle
Week 14: 08/12 – 14/12	Differential amplifiers, current mirrors + Exercise8	Ch 4.1-4.4, Ch 5.1-5.3
Week 15: 15/12 – 22/12	Current mirrors + Exercise9	Ch 5.1-5.3

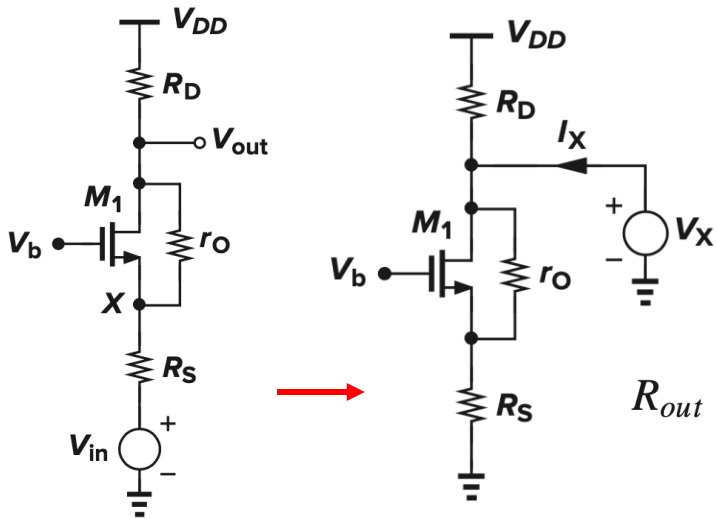
Review: Common-Gate



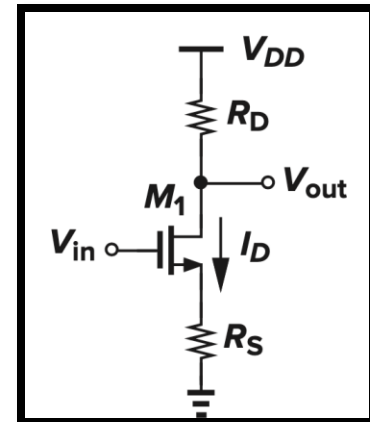
$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}$$

$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}$$

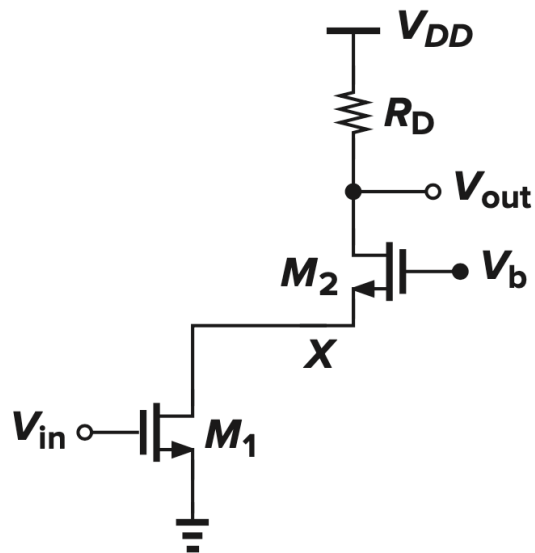
Review: Common-Gate, Cascode



$$R_{out} = \{[1 + (g_m + g_{mb})r_o]R_S + r_o\} \parallel R_D$$

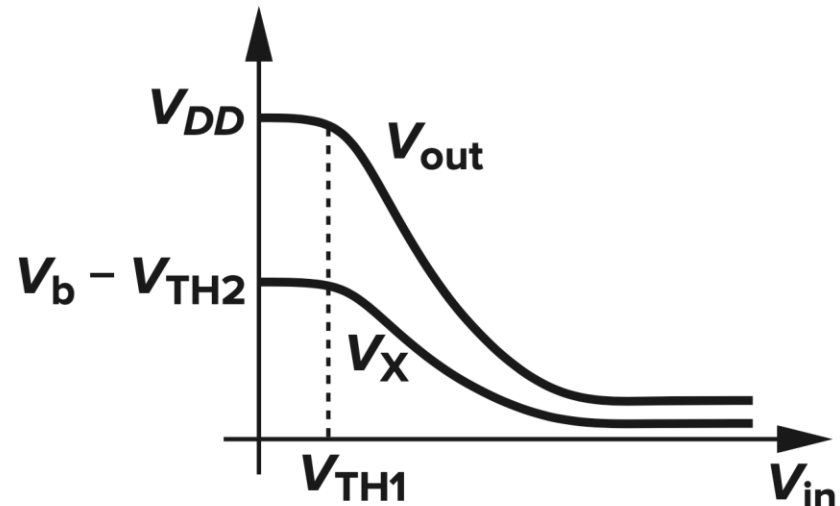
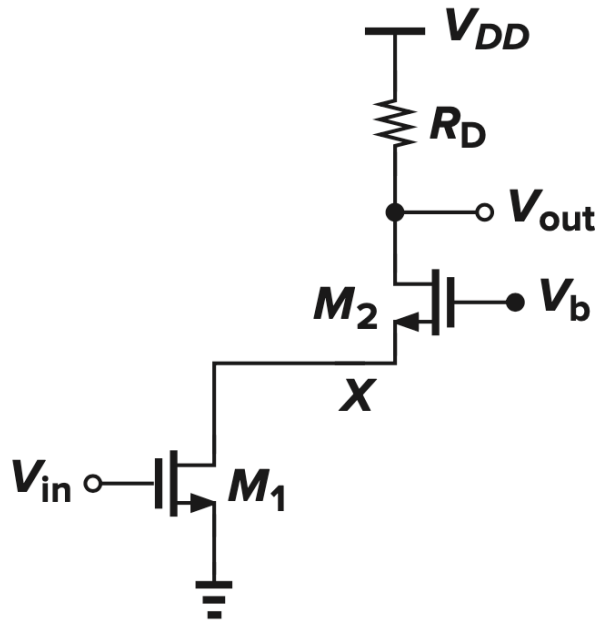


Cascode: cascade of a CS stage and a CG stage

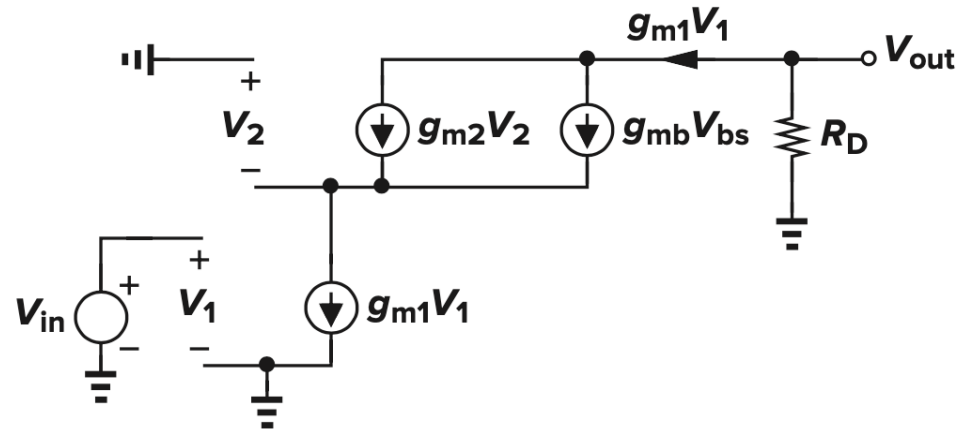
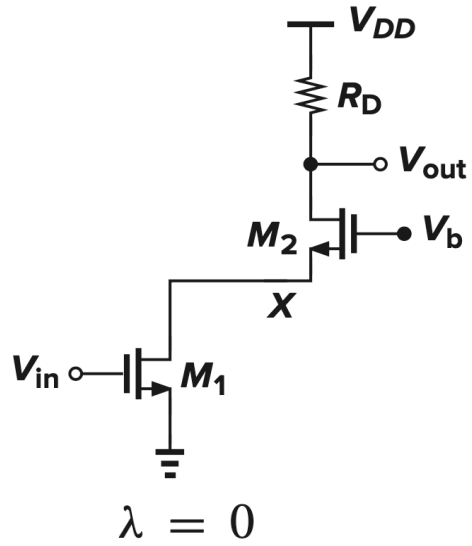


$$\begin{aligned} V_{out} &\geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2} \\ &= (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2}) \end{aligned}$$

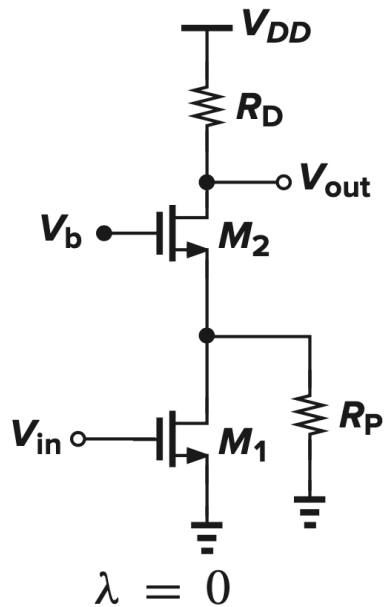
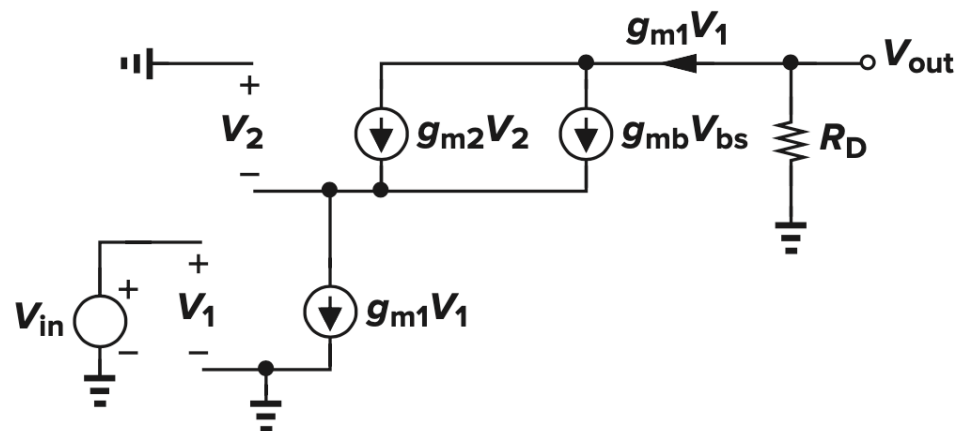
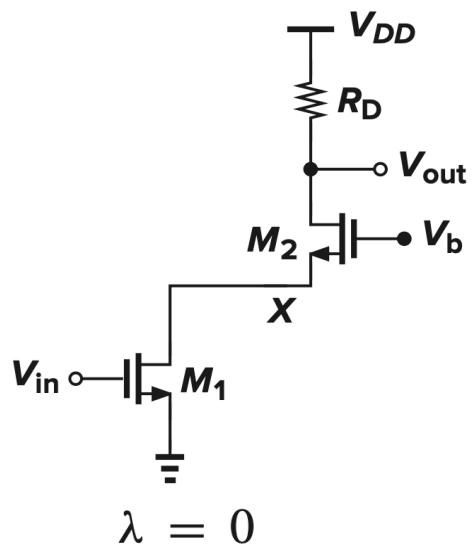
Cascode: large-signal behavior



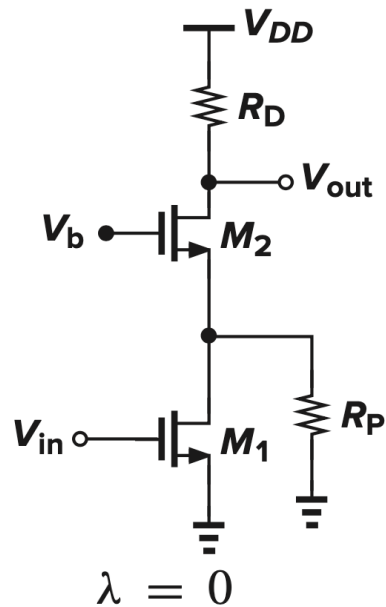
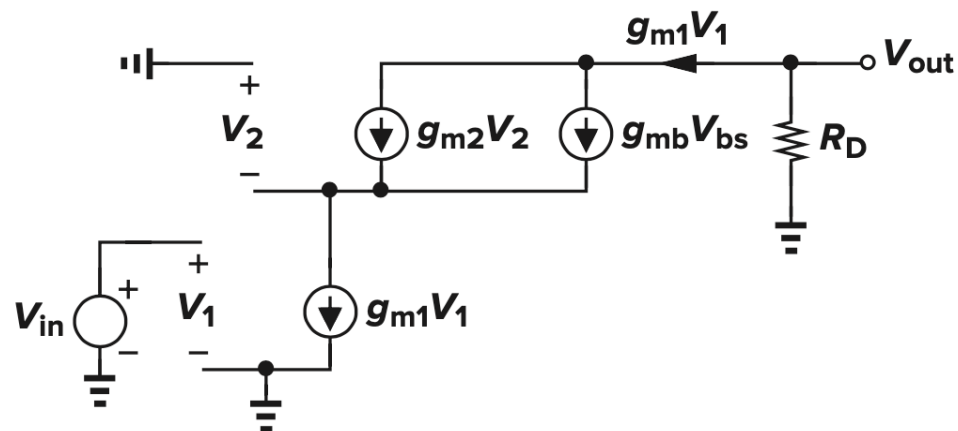
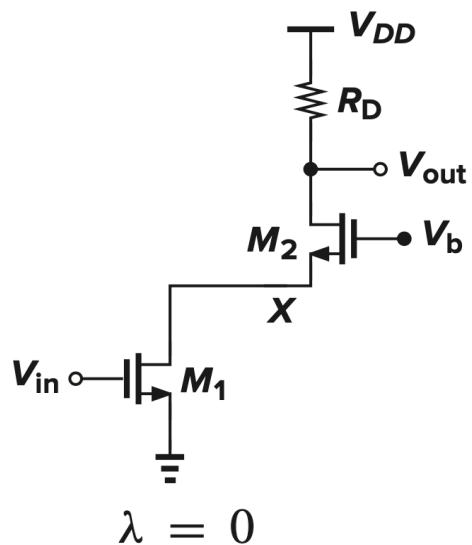
Cascode stage: Small-signal model



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Cascode stage: Small-signal model

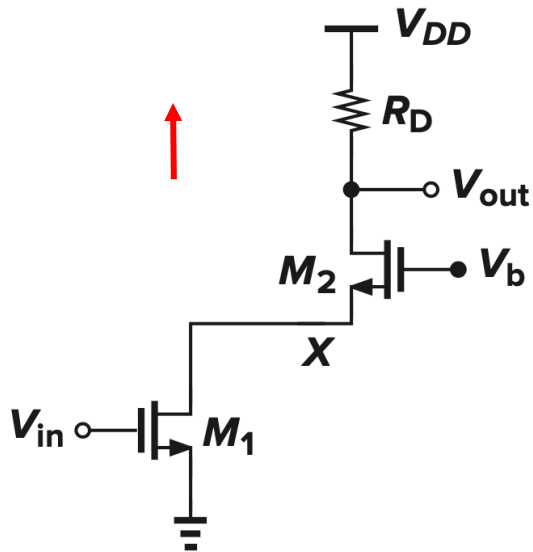
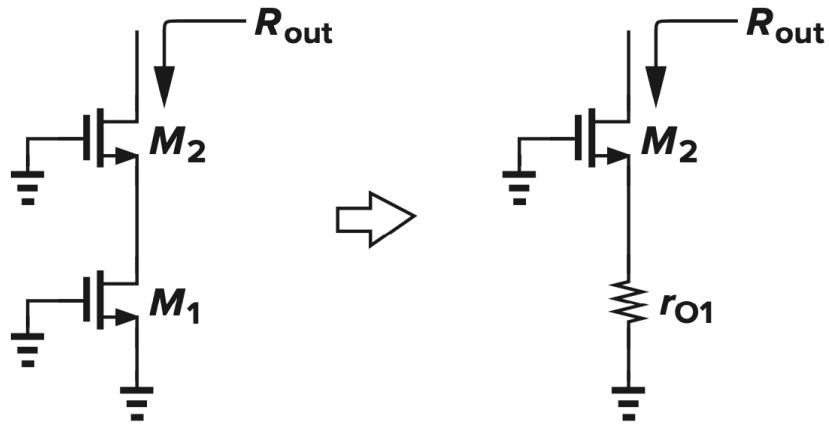


$$I_{D2} = g_{m1} V_{in} \frac{(g_{m2} + g_{mb2}) R_P}{1 + (g_{m2} + g_{mb2}) R_P}$$

$$A_v = - \frac{g_{m1} (g_{m2} + g_{mb2}) R_P R_D}{1 + (g_{m2} + g_{mb2}) R_P}$$

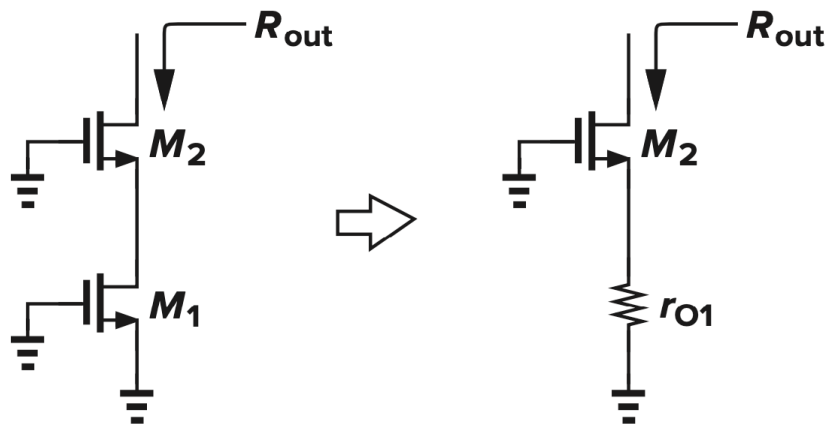
Cascode: output resistance

- ✓ An important property of the **cascode** structure is its **high output impedance**



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- ✓ An important property of the **cascode** structure is its **high output impedance**



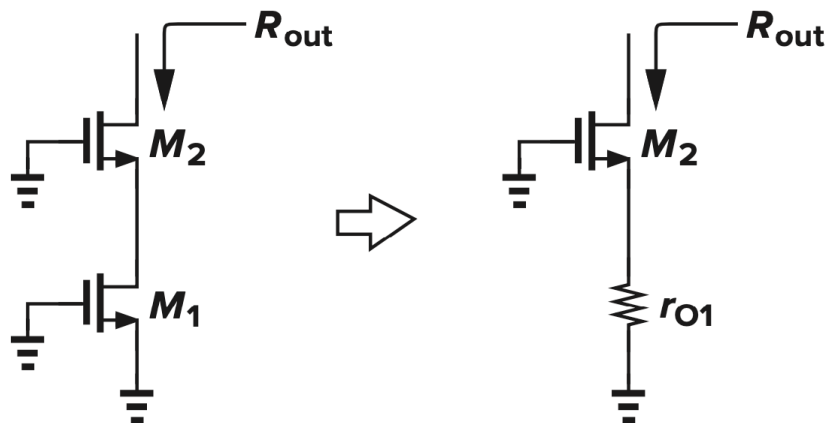
$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}$$
$$\approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$



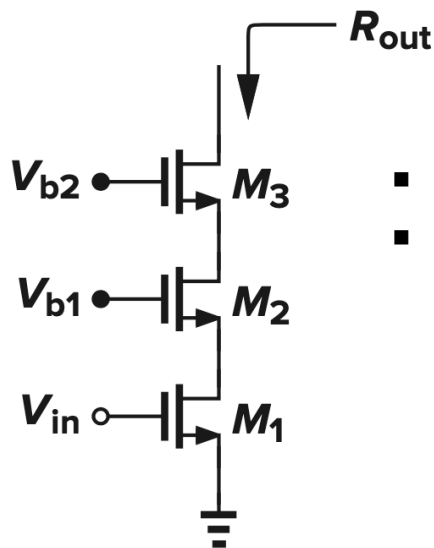
$$R_{out} = [1 + (g_m + g_{mb})R_S]r_O + R_S$$
$$= [1 + (g_m + g_{mb})r_O]R_S + r_O$$

Cascode: output resistance

- ✓ An important property of the **cascode** structure is its **high output impedance**

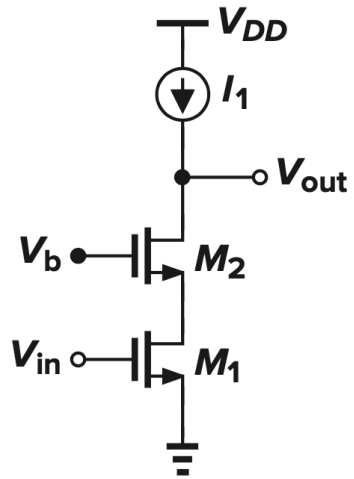


$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}$$
$$\approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$

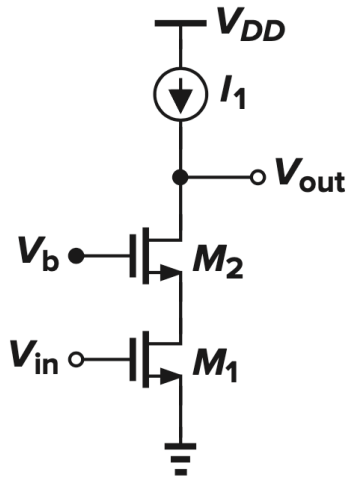


- A higher output impedance, but a limited headroom
- Minimum output voltage: sum of three overdrives

Cascode stage: gain



Cascode stage: gain



$$A_v = -G_m R_{out}$$

$$G_m \approx g_{m1}$$

$$R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$$

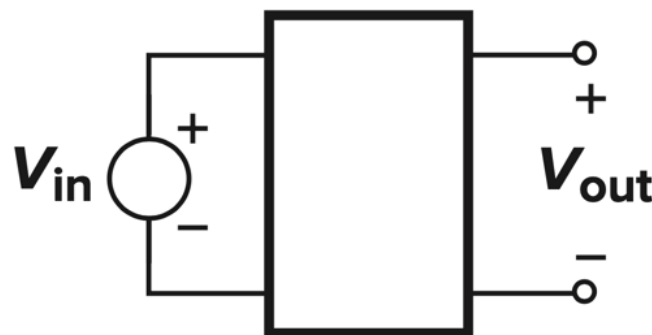
$$|A_v| = (g_{m2} + g_{mb2})r_{o2}g_{m1}r_{o1}$$

A method for voltage gain calculation

- In a linear circuit, the voltage gain is equal to $-\mathbf{G}_m \mathbf{R}_{out}$ where
 - \mathbf{G}_m is the transconductance of the circuit when the **output is ac shorted**
 - \mathbf{R}_{out} represents the output resistance of the circuit when the **input voltage is set to zero**

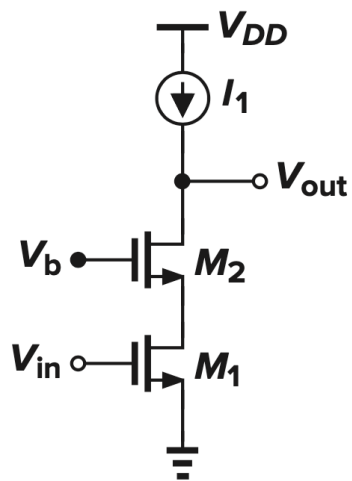
$$G_m = I_{out} / V_{in}$$

$$A_v = -G_m R_{out}$$



$$V_{out} = -G_m V_{in} R_{out}$$

Cascode stage: exact gain

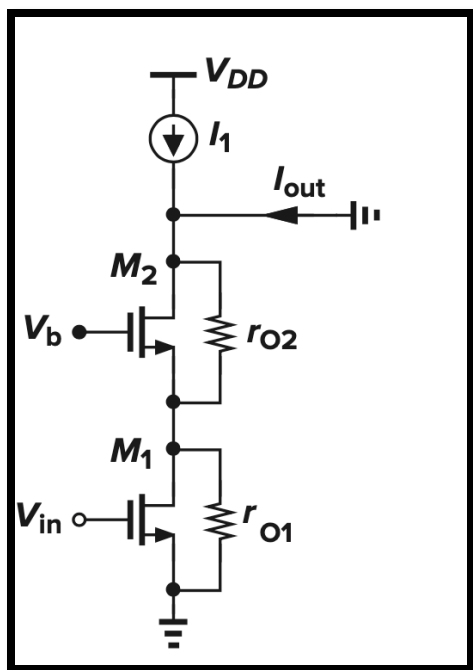


$$A_v = -G_m R_{out}$$

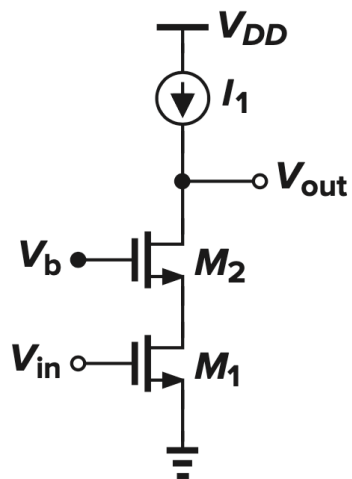
$$G_m \approx g_{m1}$$

$$R_{out} \approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$

$$|A_v| = (g_{m2} + g_{mb2})r_{O2}g_{m1}r_{O1}$$



Cascode stage: exact gain

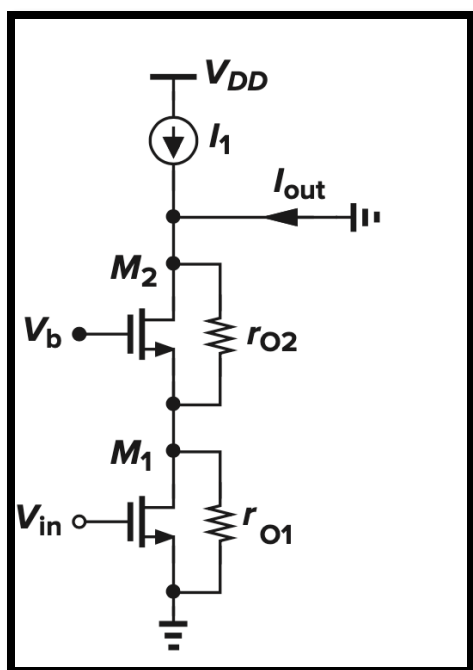


$$A_v = -G_m R_{out}$$

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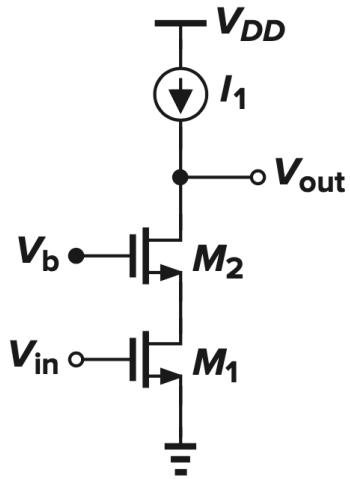
$$R_{out} \approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$

$$|A_v| = (g_{m2} + g_{mb2})r_{O2}g_{m1}r_{O1}$$



$$I_{out} = g_{m1} V_{in} \frac{r_{O1}}{r_{O1} + \frac{1}{g_{m2} + g_{mb2}} \parallel r_{O2}}$$

Cascode stage: exact gain

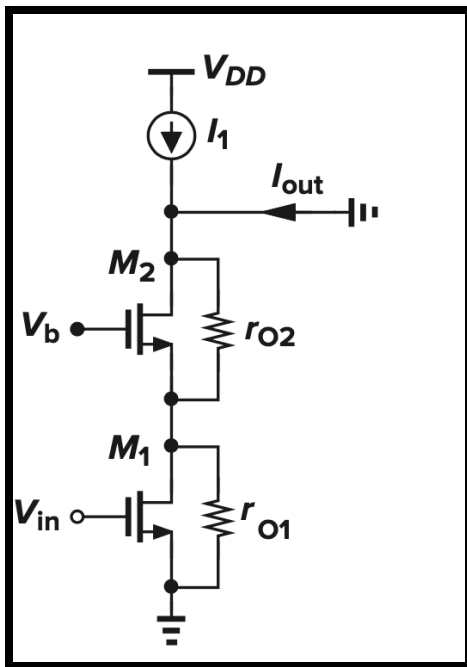


$$A_v = -G_m R_{out}$$

$$G_m \approx g_{m1}$$

$$R_{out} \approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$

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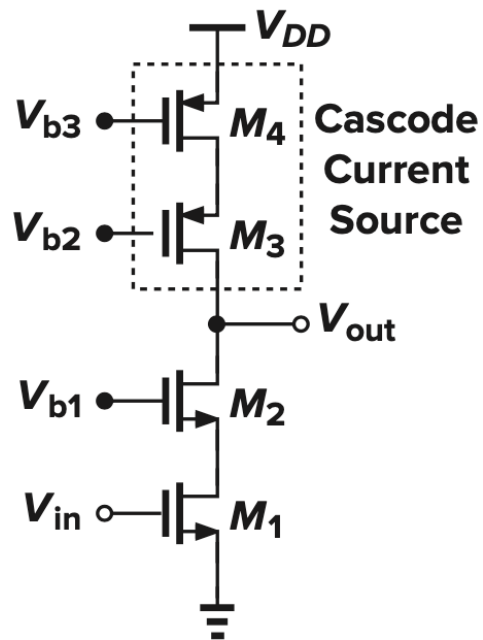
$$I_{out} = g_{m1} V_{in} \frac{r_{O1}}{r_{O1} + \frac{1}{g_{m2} + g_{mb2}} \parallel r_{O2}}$$

$$G_m = \frac{g_{m1} r_{O1} [r_{O2} (g_{m2} + g_{mb2}) + 1]}{r_{O1} r_{O2} (g_{m2} + g_{mb2}) + r_{O1} + r_{O2}}$$

$$|A_v| = G_m R_{out}$$

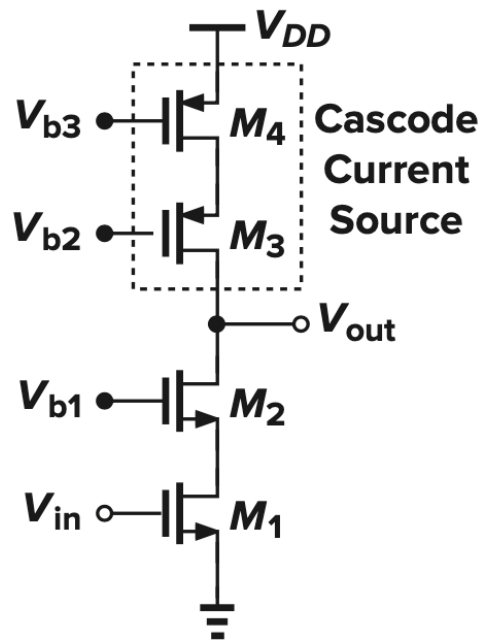
$$= g_{m1} r_{O1} [(g_{m2} + g_{mb2}) r_{O2} + 1]$$

Cascode as a constant current source



$$\uparrow [1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}$$

Cascode as a constant current source



$$\uparrow [1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}$$

$$A_v = -G_m R_{out}$$

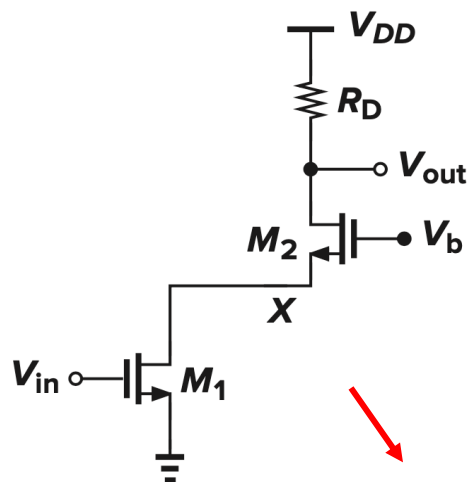
$$R_{out} = \{[1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}\} \parallel \{[1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}\}$$

$$|A_v| \approx g_{m1} R_{out}$$

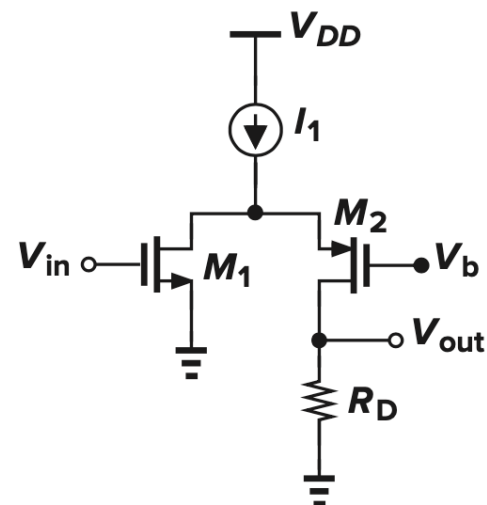
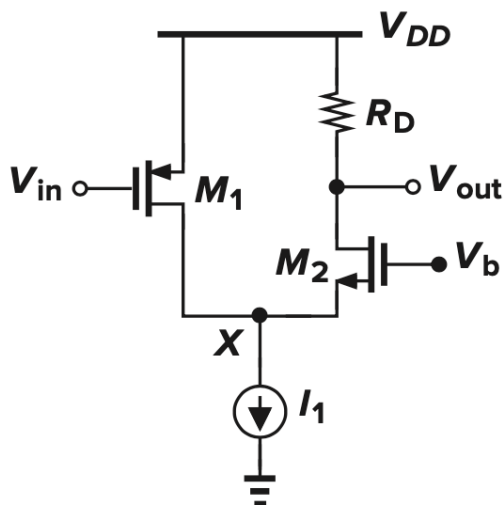
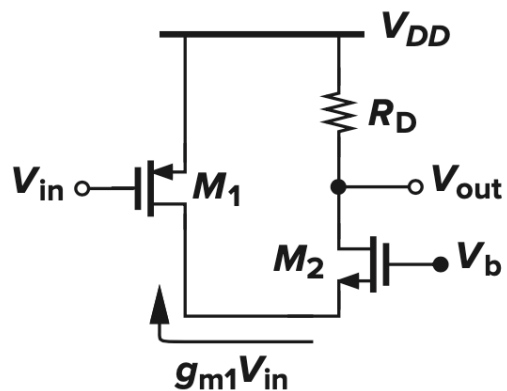
$$|A_v| \approx g_{m1} [(g_{m2}r_{O2}r_{O1}) \parallel (g_{m3}r_{O3}r_{O4})]$$

$$V_{out,max} - V_{out,min} = V_{DD} - (V_{GS1} - V_{TH1}) - (V_{GS2} - V_{TH2}) - |V_{GS3} - V_{TH3}| - |V_{GS4} - V_{TH4}|$$

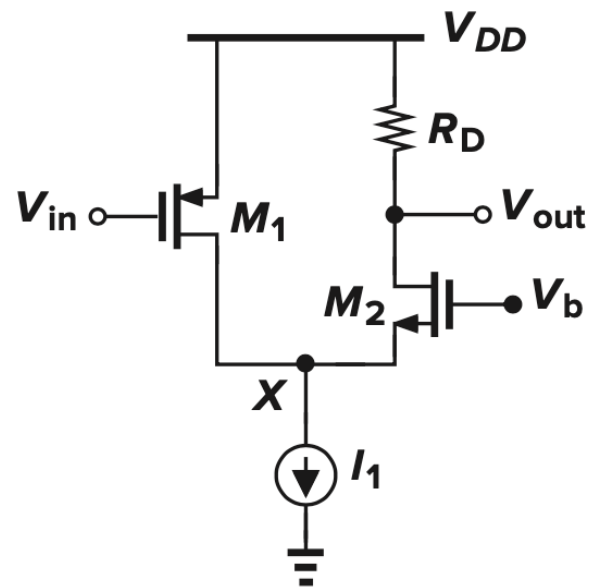
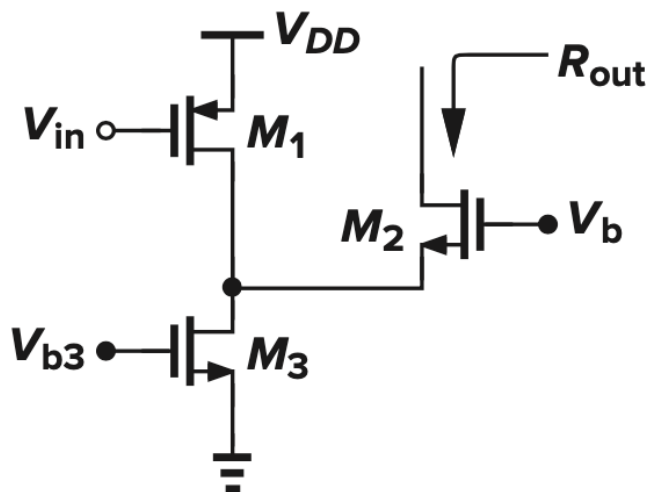
Folded Cascode



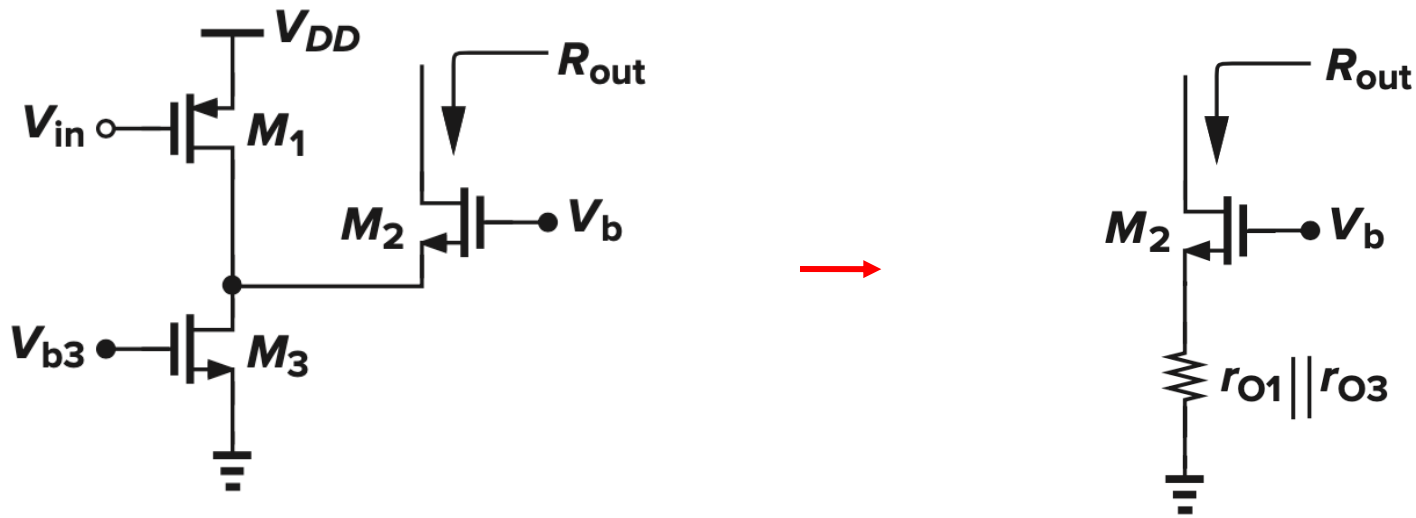
- ✓ Cascode: to convert the input voltage to a current and apply the result to a common-gate stage
- ✓ The input and cascode devices need not be of the same type



Example: Calculate the output impedance

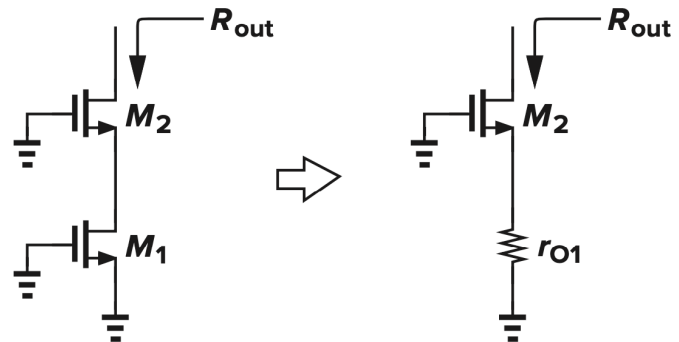


Example: Calculate the output impedance

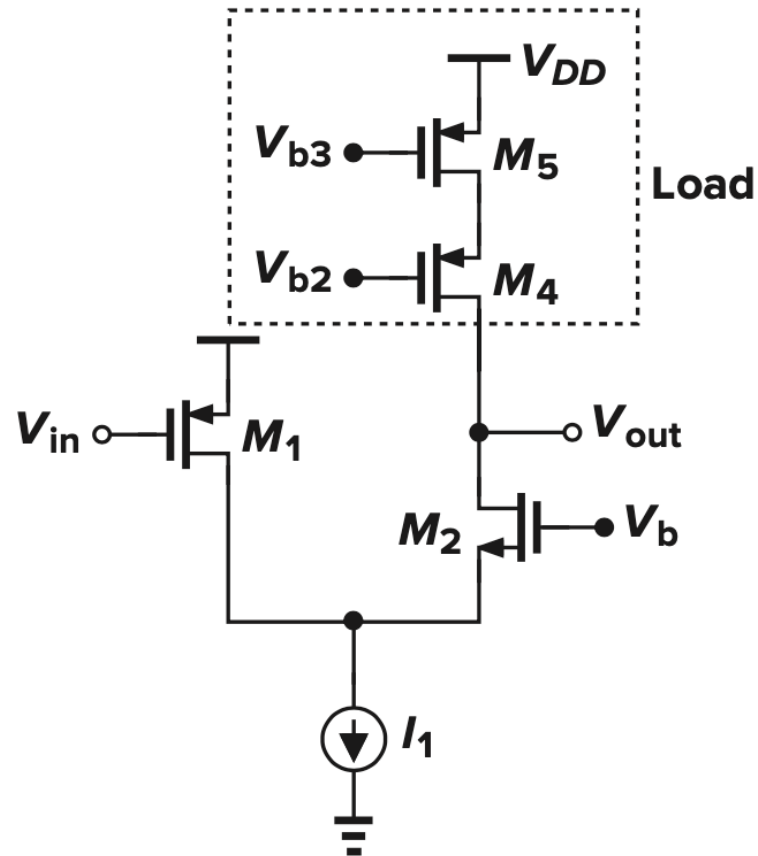


$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}](r_{O1} \parallel r_{O3}) + r_{O2}$$

✓ The output impedance is lower than a nonfolded “telescopic” cascode



Folded cascode with a cascode load

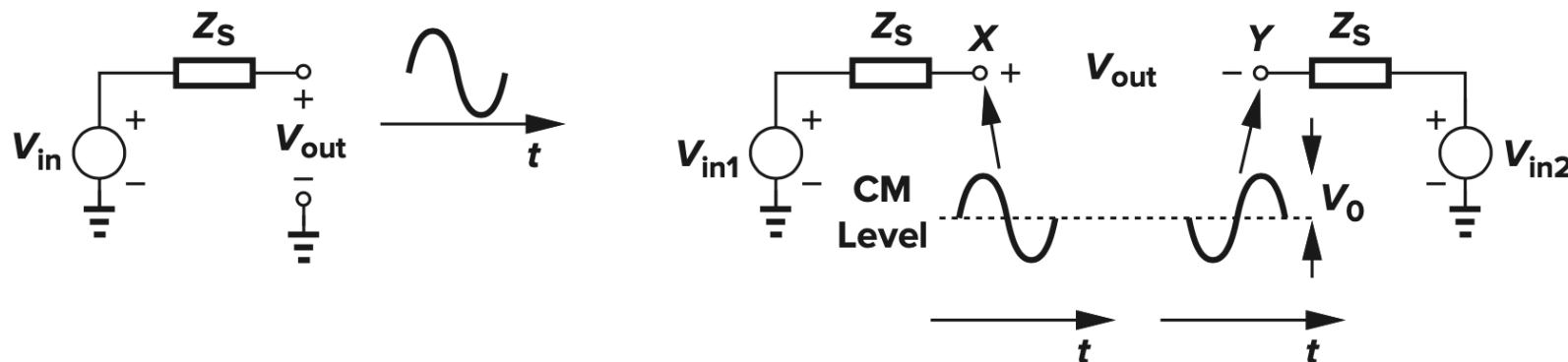


Differential Operation

- Differential operation
 - An important circuit invention
 - Used in high-performance analog and mixed-signal circuits

Differential Operation

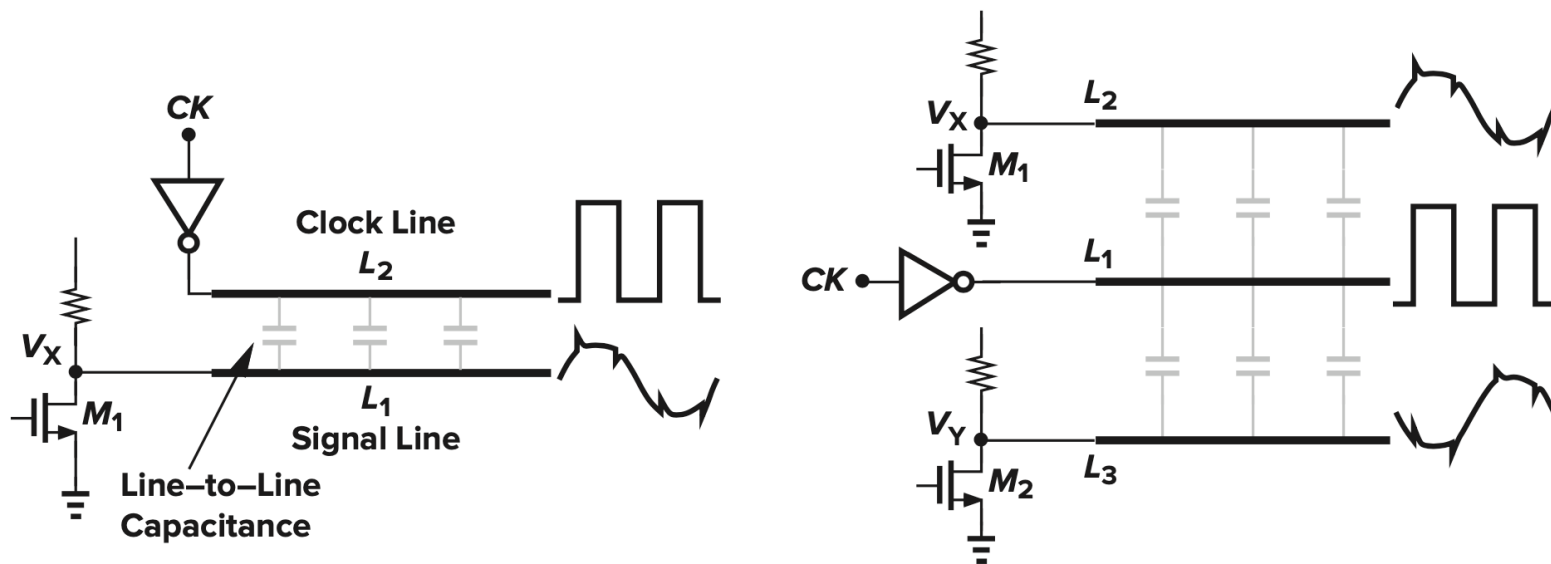
- Differential operation
 - An important circuit invention
 - Used in high-performance analog and mixed-signal circuits
- **Single-Ended and Differential Operation:**



- A **single-ended** signal is measured wrt a fixed potential, usually the ground
- A **differential** signal is measured between two nodes that have **equal and opposite** signal excursions around a fixed potential
- The “center” potential in differential signaling is the “common-mode” (CM) level

Differential Operation: immune to CM noise

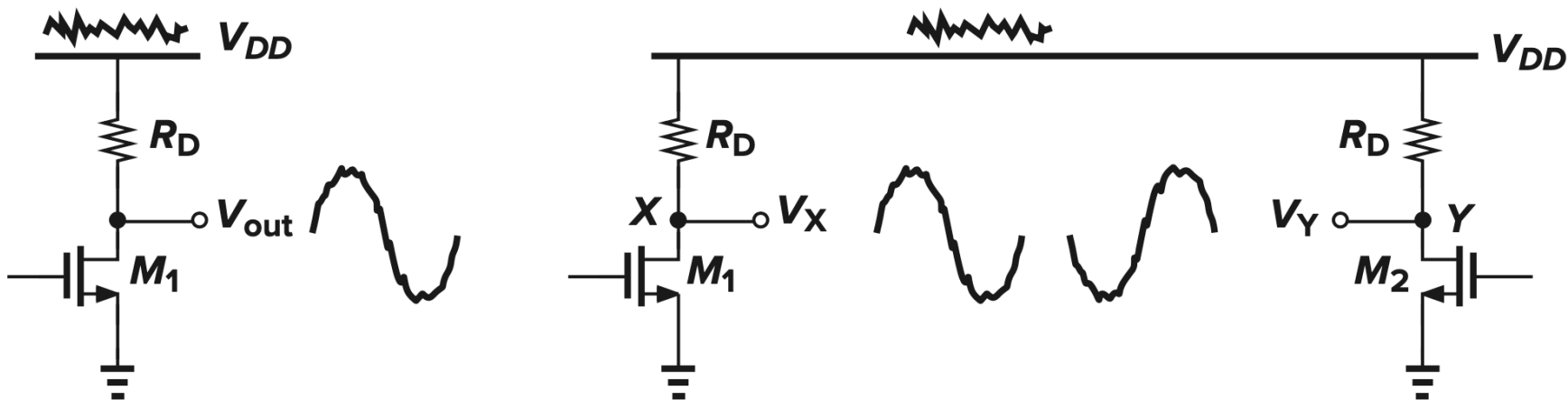
- Higher immunity to “environmental” noise



- The CM level of the two phases is disturbed, but the differential output is not corrupted, so it “rejects” common-mode noise

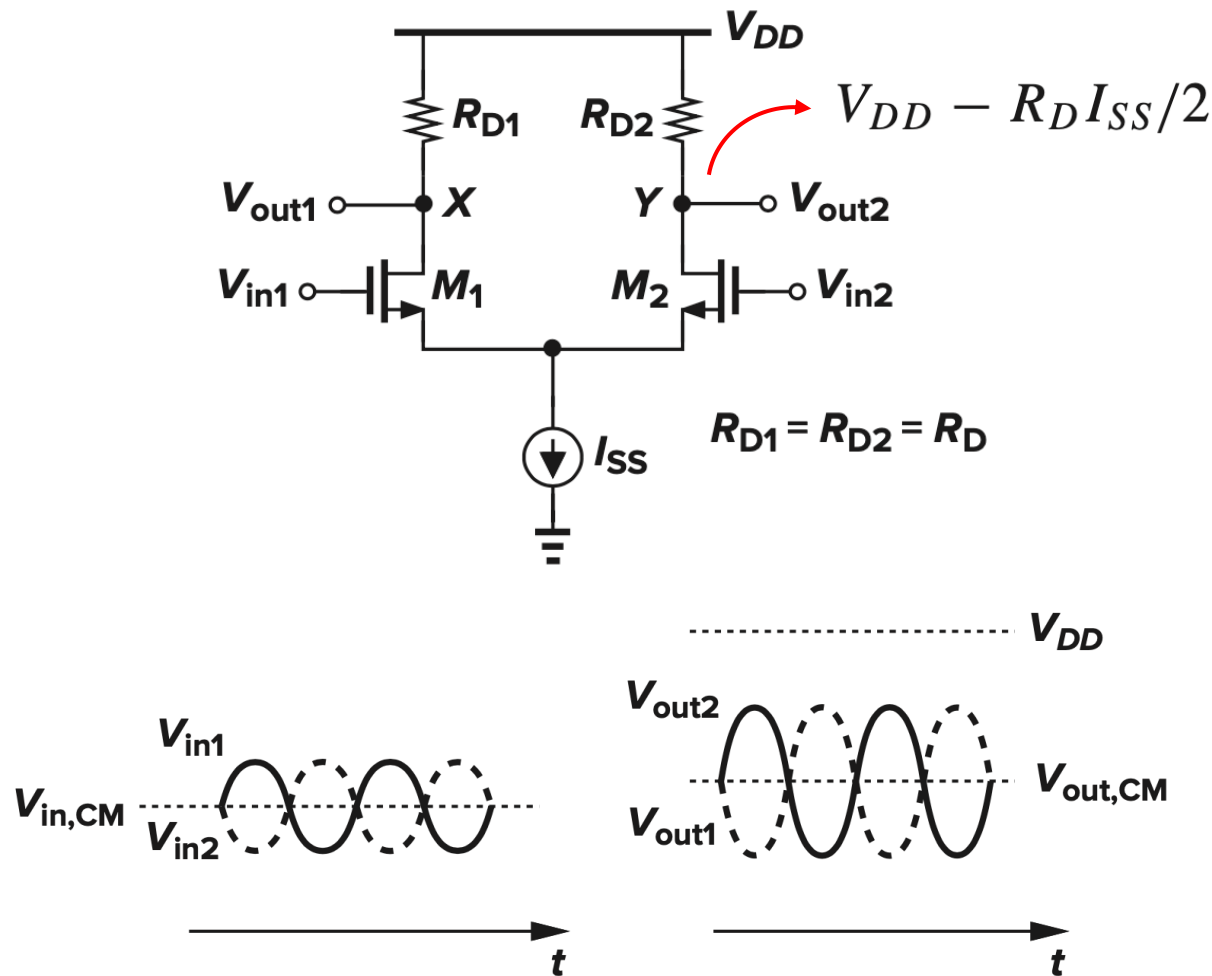
Differential Operation: immune to supply noise

- Higher immunity to “environmental” noise



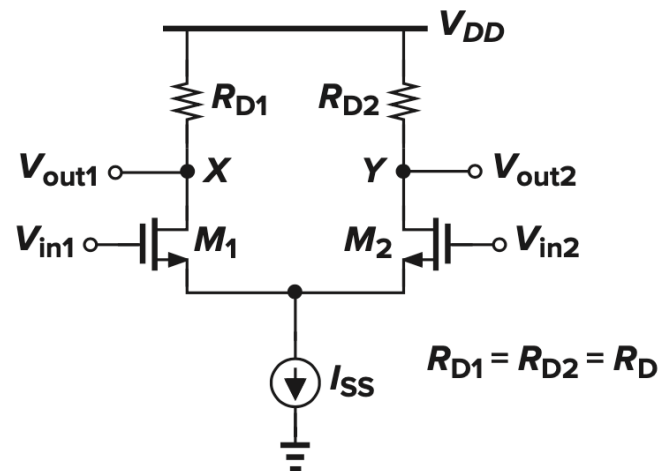
Basic Differential Pair

- Bias currents should have minimal dependence on the input CM level

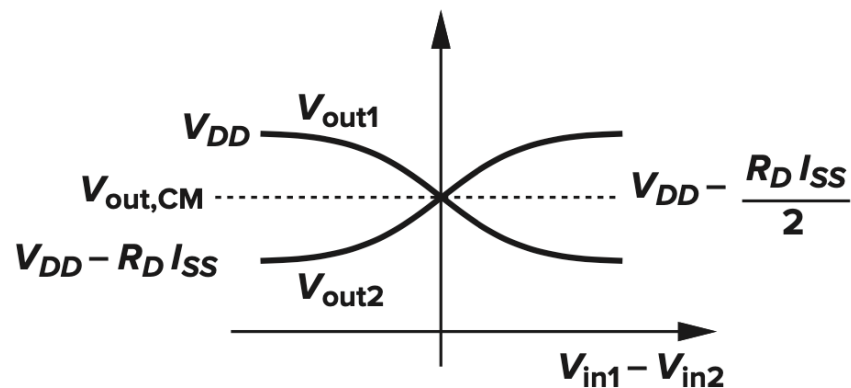


Differential input-output characteristics

(neglecting channel-length modulation and body effect):

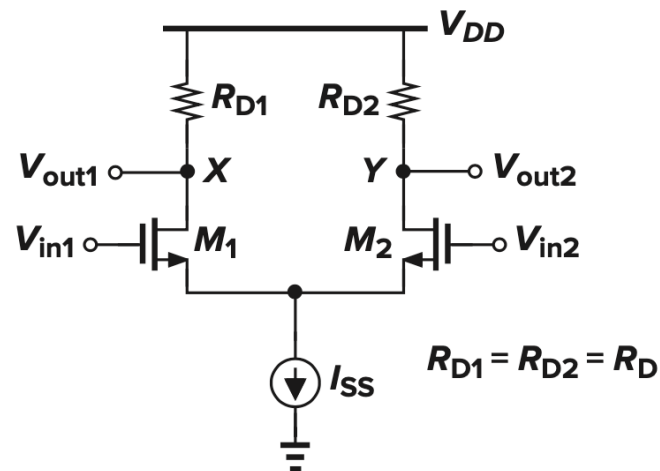


Differential input-output characteristics of a diff pair



Differential input-output characteristics

(neglecting channel-length modulation and body effect):



Differential input-output characteristics of a diff pair

