Integrated Neurotechnologies Laboratory

EPFL

Analog IC design (EE-320), Lecture 6

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Institute of Electrical and Micro Engineering, School of Engineering, EPFL

Homework 1, TP Schedule

Week	**Subject by week – EE-320: Analog IC design – Fall 2025**	**Suggested Chapters**
Week 1: **08/09** – 14/09	**Introduction, organization, review of MOS transistors** + Exercise1	Ch 1, Ch 2.1-2.4, Slides on Moodle
Week 2: **15/09** – 21/09	**MOS large and small-signal models, regimes of operations** + Exercise2	Ch 2.1-2.4
Week 3: **22/09** – 28/09	**Holiday – No class**	
Week 4: **29/09** – 05/10	**MOS parasitic effects, layout basic, single-stage amplifiers** + Exercise3	Ch 2.1-2.4, Ch 3.1
Week 5: **06/10** – 12/10	**Single-stage amplifiers** + Exercise4	Ch 3.1-3.7
Week 6: **13/10** – 19/10	**Single-stage amplifiers** + Exercise5	Ch 3.1-3.7
Week 7: **20/10** – 26/10	**Break – No class**	
Week 8: **27/10** – 02/11	**Single-stage amplifiers + Cascode** + Exercise6 + **Homework1**	Ch 3.1-3.7
Week 9: **03/11** – 09/11	**Differential amplifiers** + Exercise7	Ch 4.1-4.4
Week 10: **10/11** – 16/11	**TP1** Practical exercise session on Cadence	Tutorial on Moodle
Week 11: **17/11** – 23/11	**TP2** Practical exercise session on Cadence	Tutorial on Moodle
Week 12: **24/11** – 30/12	**TP3** Practical exercise session on Cadence + **Homework2**	Tutorial on Moodle
Week 13: **01/12** – 07/12	**TP4** Practical exercise session on Cadence	Tutorial on Moodle
Week 14: **08/12** – 14/12	**Differential amplifiers, current mirrors** + Exercise8	Ch 4.1-4.4, Ch 5.1-5.3
Week 15: **15/12** – 22/12	**Current mirrors** + Exercise9	Ch 5.1-5.3

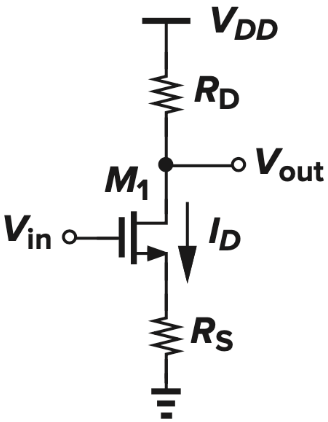
Assessment:

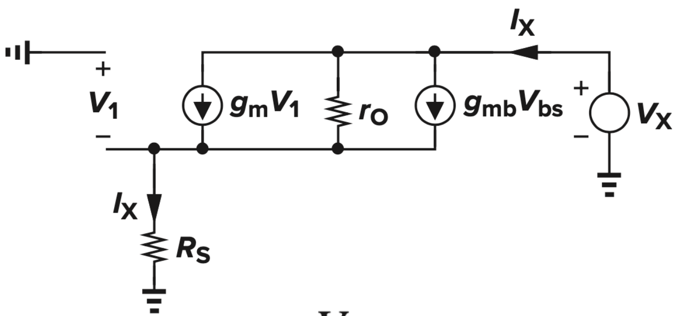
- **Written final exam**: 70% of the final grade
- **Homework (2 in total)**: 30% of the final grade

EDA Statement

- **Assignment for EDA document**, to be signed and uploaded via moodle, please complete the assignment **by Nov 3**
- **First TP session on Nov 10 in BC07-08** from **3:15pm to 6pm**
- **Homework 1 assignment** will be posted later this week
- **Homework 2 assignment** will be posted after TP3

Review: Common-Source

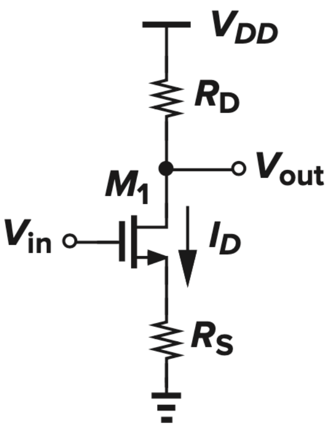


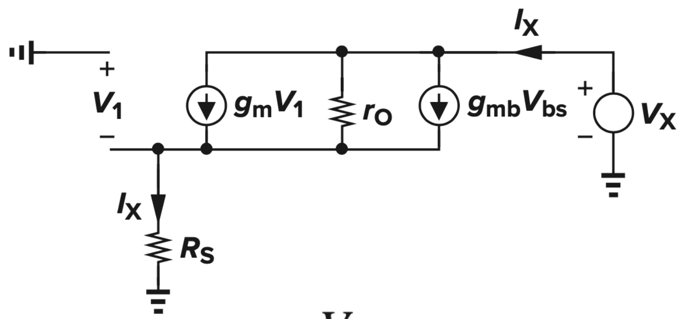


$$R_{out} = [1 + (g_m + g_{mb})R_S]r_O + R_S$$
$$= [1 + (g_m + g_{mb})r_O]R_S + r_O$$

$$\frac{V_{out}}{V_{in}} = \frac{-g_m r_O R_D}{R_D + R_S + r_O + (g_m + g_{mb})R_S r_O}$$

Review: Common-Source, Source-Follower





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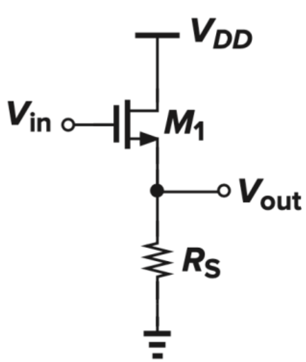
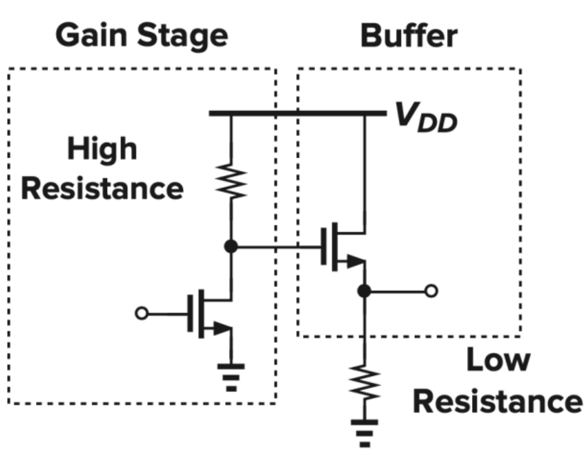
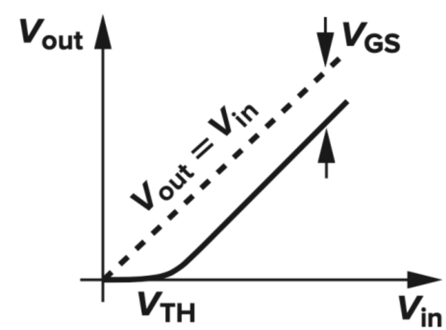
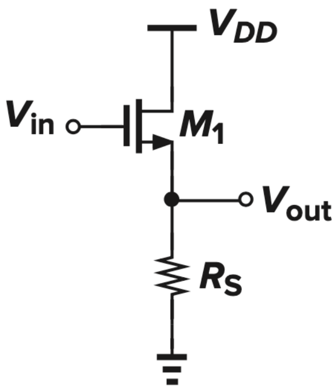
Source follower: common-drain or **voltage buffer**

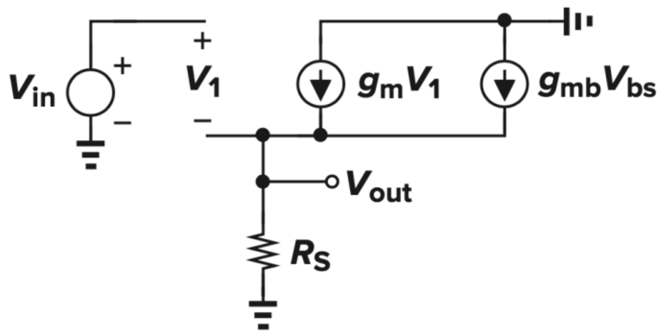




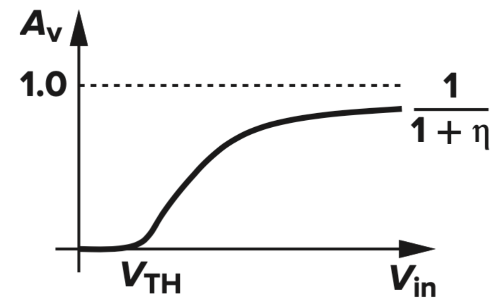


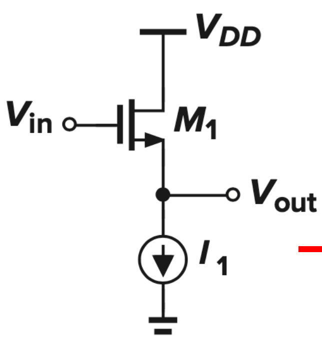
Review: Source-Follower

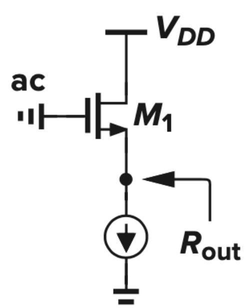


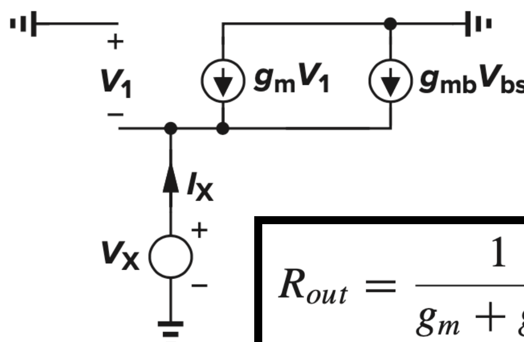


$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S}$$

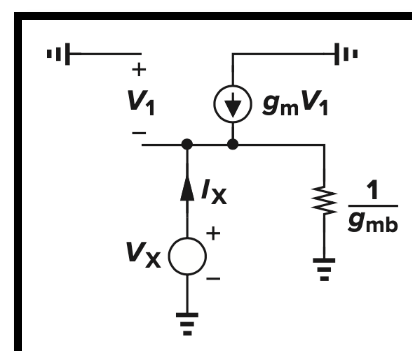




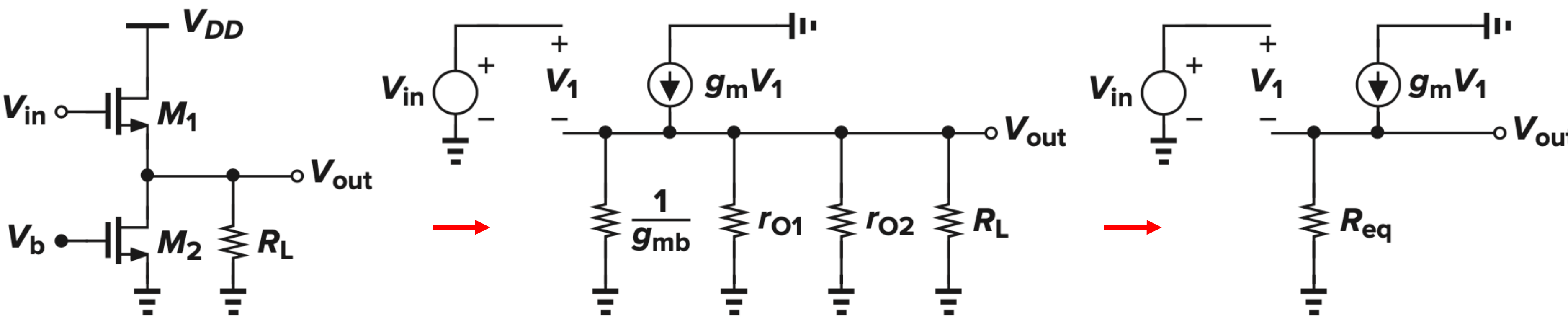




$$R_{out} = \frac{1}{g_m + g_{mb}}$$



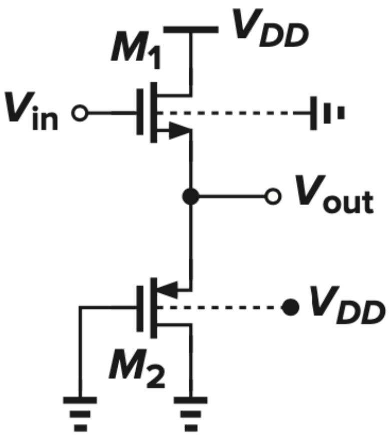
Review: Source Follower with a finite load resistance



$$A_v = \frac{R_{eq}}{R_{eq} + \dfrac{1}{g_m}}$$

$$R_{eq} = (1/g_{mb})||r_{O1}||r_{O2}||R_L$$

Example: Calculate the voltage gain



$$A_v = \frac{\frac{1}{g_{m2}+g_{mb2}} \| r_{O2} \| r_{O1} \| \frac{1}{g_{mb1}}}{\frac{1}{g_{m2}+g_{mb2}} \| r_{O2} \| r_{O1} \| \frac{1}{g_{mb1}} + \frac{1}{g_{m1}}}$$

PMOS Source Follower with no body effect

- Source follower drawbacks:
  - **nonlinearity**
  - **voltage headroom limitation**

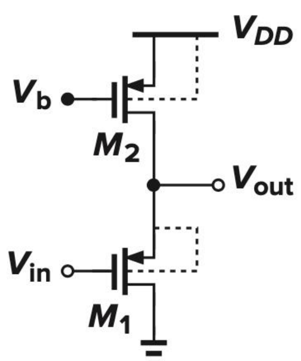
- Even if biased by an ideal current source, some nonlinearity exists due to the **nonlinear** dependence of $\boldsymbol{V_{TH}}$ upon the **source** potential

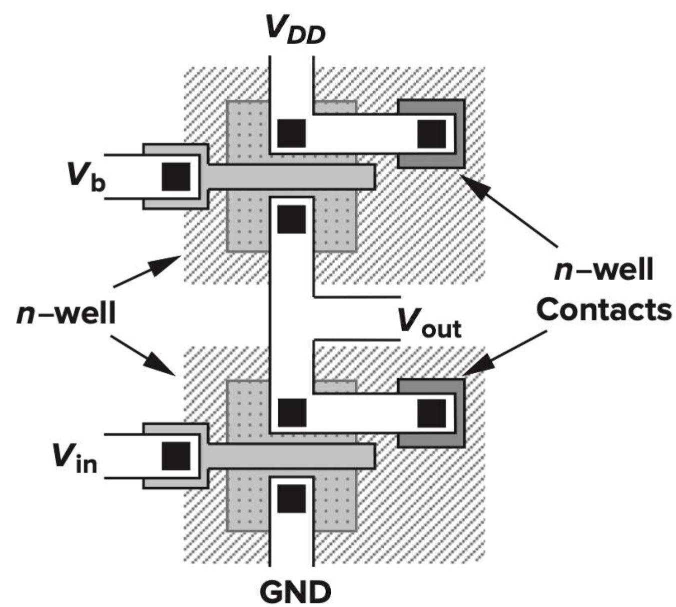
PMOS Source Follower with no body effect

- Source follower drawbacks:
  - **nonlinearity**
  - **voltage headroom limitation**

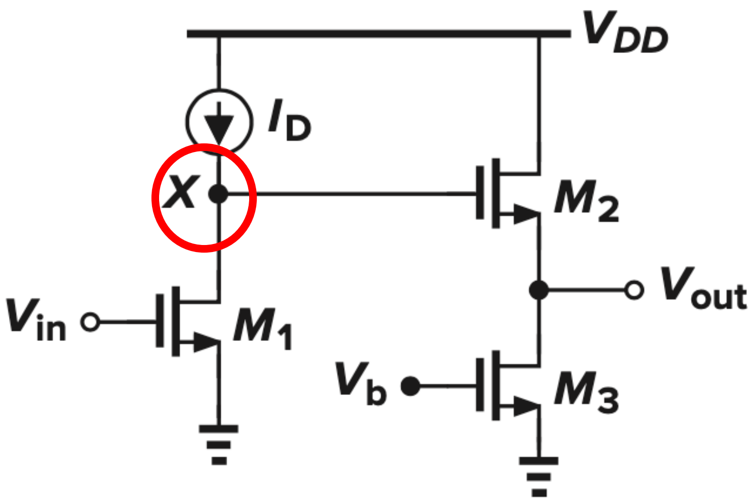
- Even if biased by an ideal current source, some nonlinearity exists due to the **nonlinear** dependence of $\boldsymbol{V_{TH}}$ upon the **source** potential

- The nonlinearity due to body effect can be eliminated if the bulk is tied to source





Source Follower: a level shifter

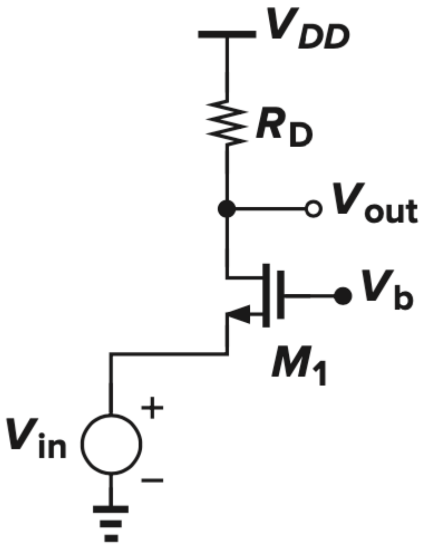


$$V_{GS1} - V_{TH1} \rightarrow V_{GS2} + (V_{GS3} - V_{TH3})$$

- Source followers shift the dc level by V_{GS}, thereby consuming voltage headroom and limiting the swings
- One application of source followers is in performing **voltage-level shift**

Common-Gate Stage

- A common-gate (CG) stage senses the input at the **source** and produces the output at the **drain**



Common-Gate Stage

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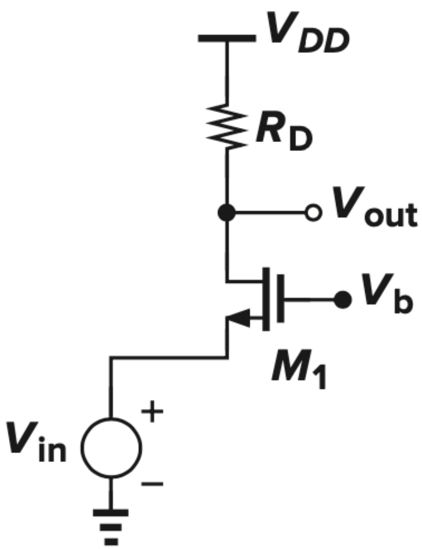
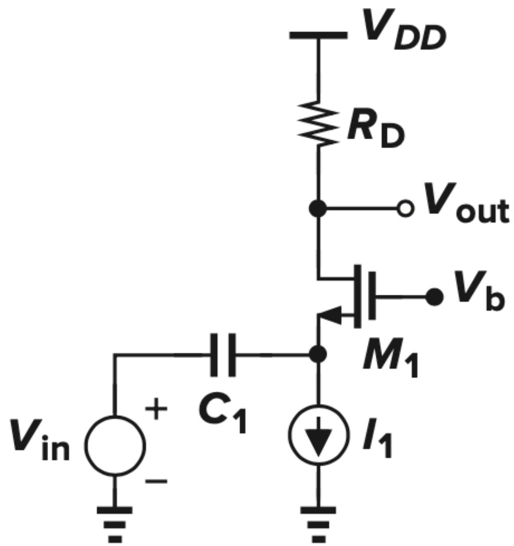
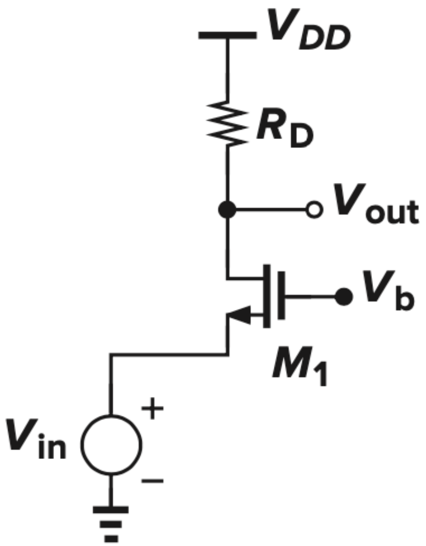




Common-Gate Stage: large signal analysis



in saturation

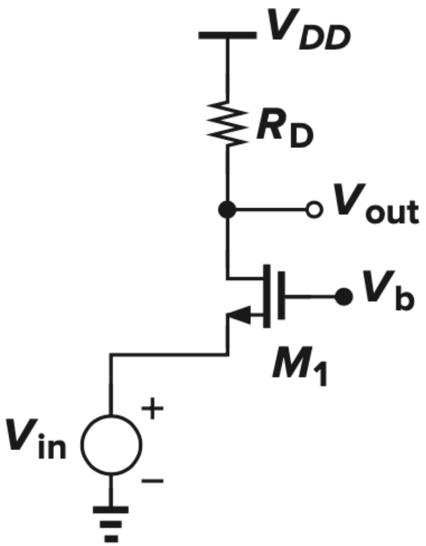
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2$$

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$$

driving M_1 into the triode region if:

$$V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$$

Common-Gate Stage: large signal analysis



in saturation

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$$

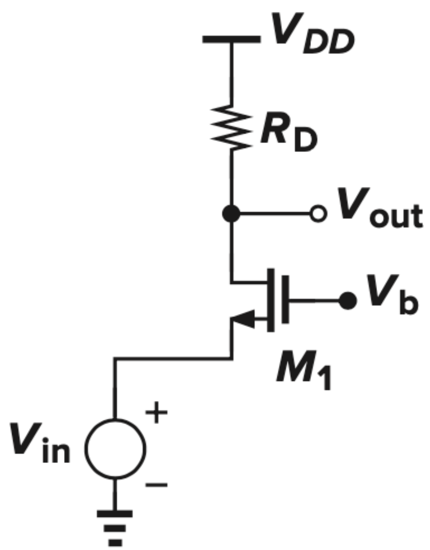
$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right) R_D$$

$$\partial V_{TH}/\partial V_{in} = \partial V_{TH}/\partial V_{SB} = \eta$$

$$= \mu_n C_{ox}\frac{W}{L} R_D(V_b - V_{in} - V_{TH})(1+\eta)$$

$$= g_m(1+\eta)R_D$$

Common-Gate Stage: large signal analysis



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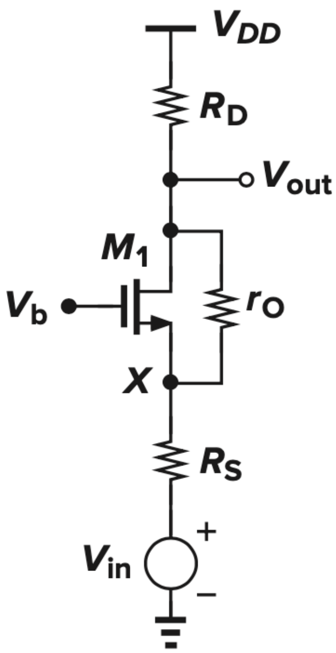
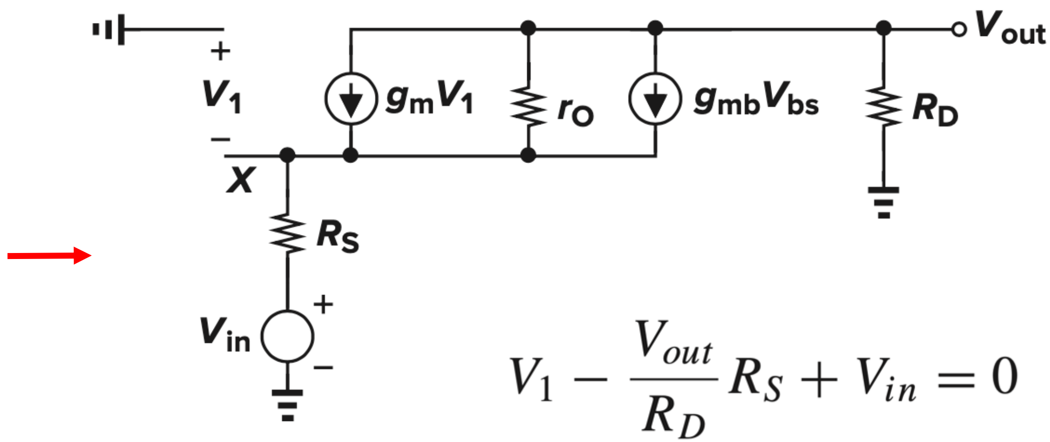
$$= g_m(1+\eta)R_D$$

- for $\lambda = 0$, the **input impedance** (seen at the source of M_1): $1/(g_m + g_{mb})$

$$1/[g_m(1+\eta)]$$

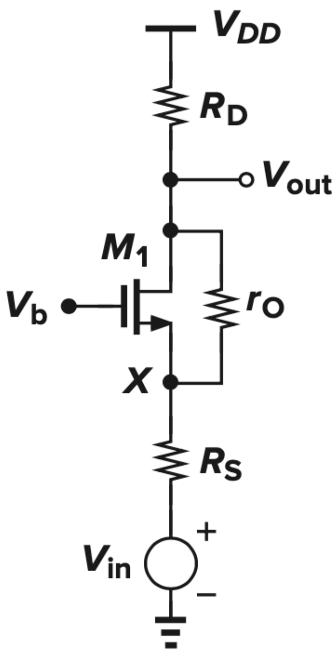
Common-Gate Stage: general case

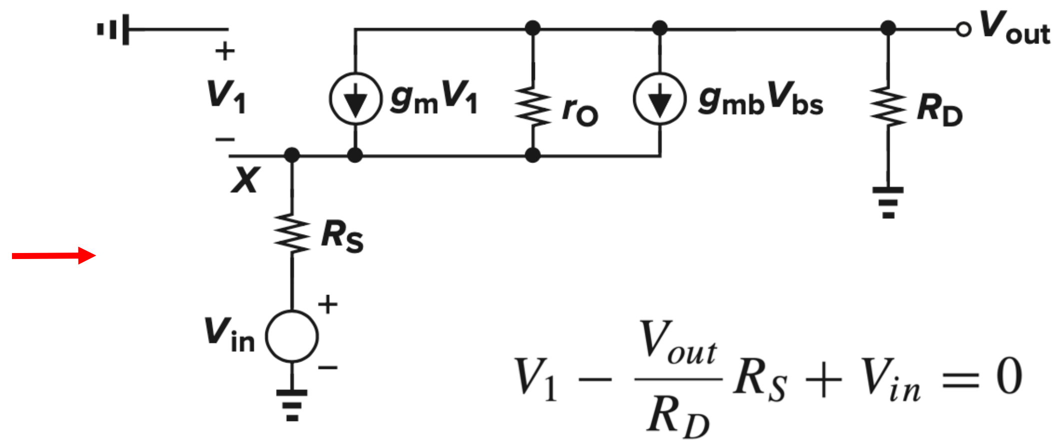




$$V_1 - \frac{V_{out}}{R_D} R_S + V_{in} = 0$$

Common-Gate Stage: general case

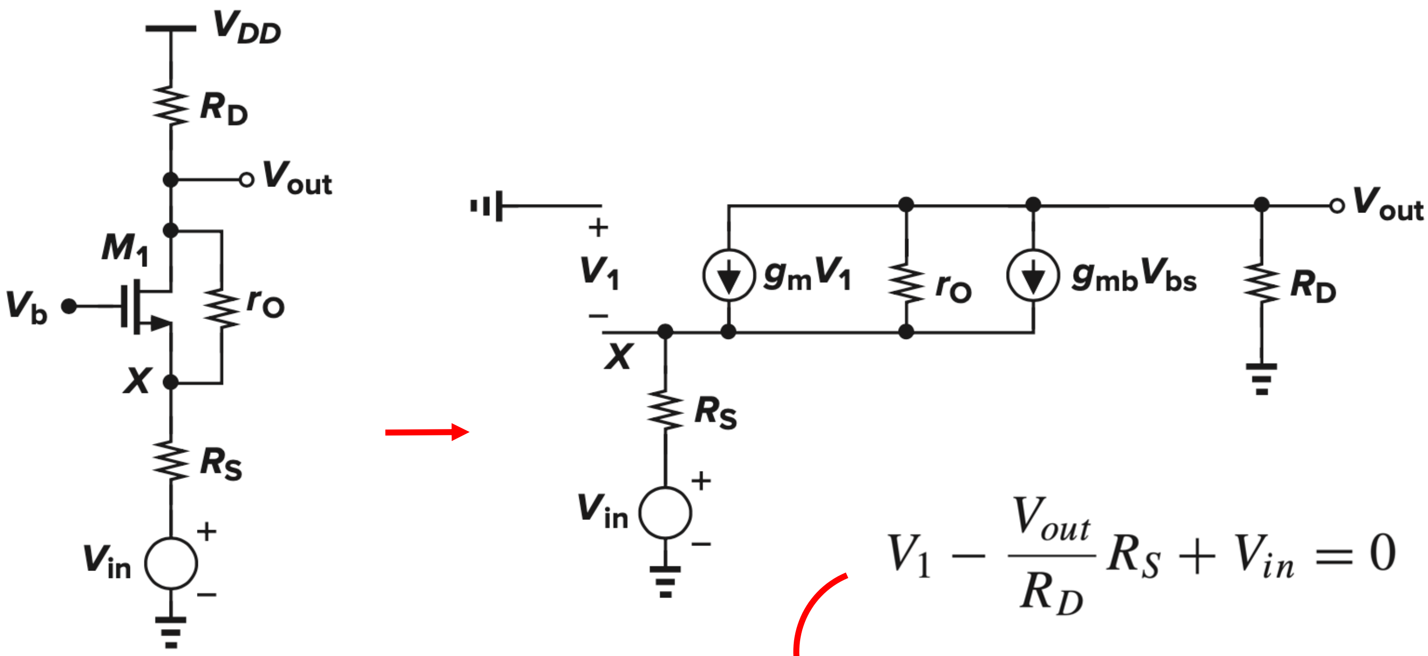




$$V_1 - \frac{V_{out}}{R_D} R_S + V_{in} = 0$$

$$r_O \left(\frac{-V_{out}}{R_D} - g_m V_1 - g_{mb} V_1 \right) - \frac{V_{out}}{R_D} R_S + V_{in} = V_{out}$$

Common-Gate Stage: general case



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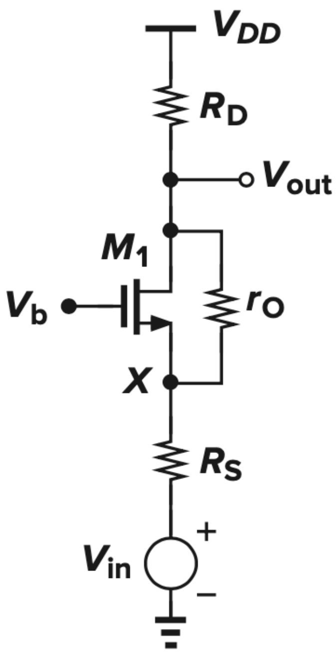
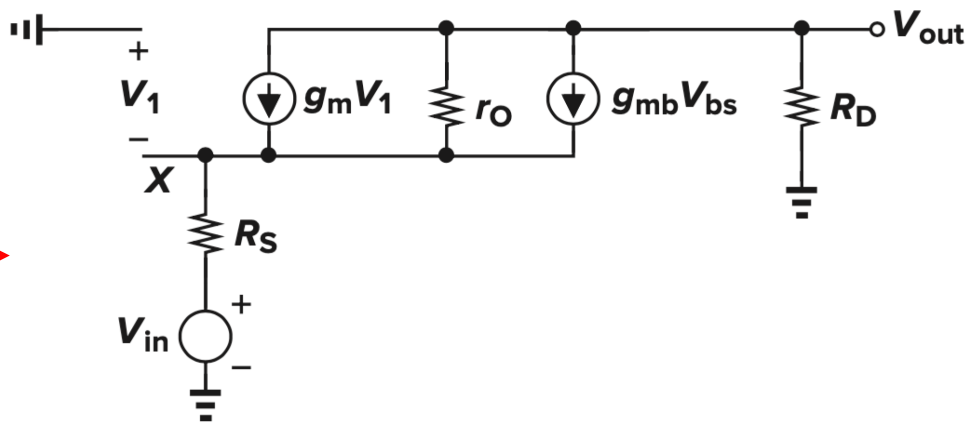
$$r_O \left[\frac{-V_{out}}{R_D} - (g_m + g_{mb}) \left(V_{out} \frac{R_S}{R_D} - V_{in} \right) \right] - \frac{V_{out} R_S}{R_D} + V_{in} = V_{out}$$

Common-Gate Stage: general case



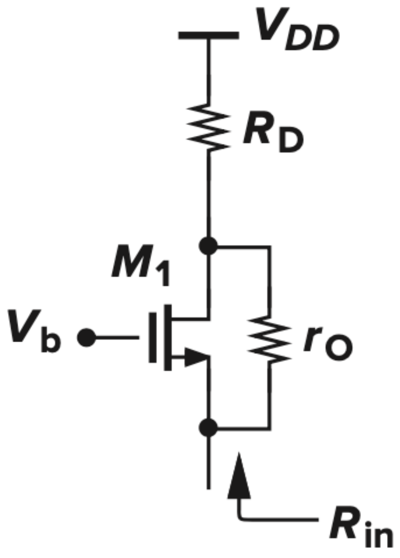


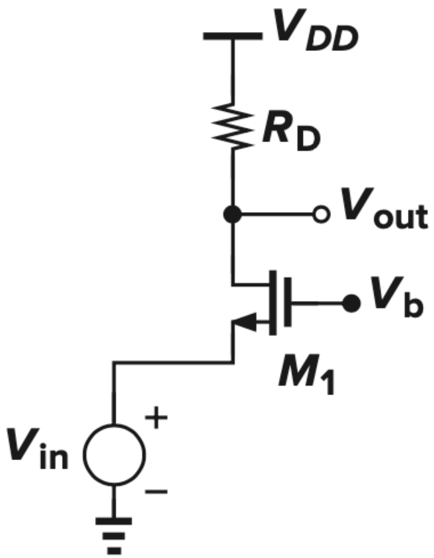
$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_D} R_D$$

Gain of a degenerated CS stage

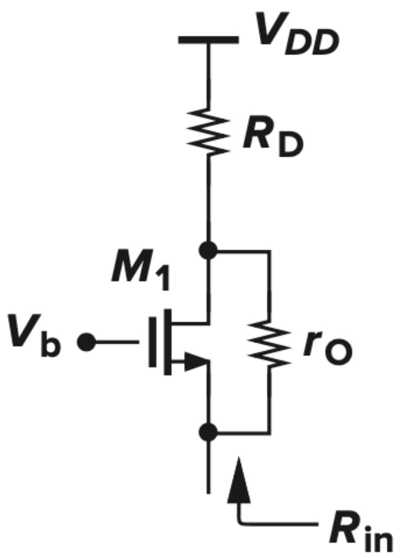
$$\frac{V_{out}}{V_{in}} = \frac{-g_m r_O R_D}{R_D + R_S + r_O + (g_m + g_{mb})R_S r_O}$$

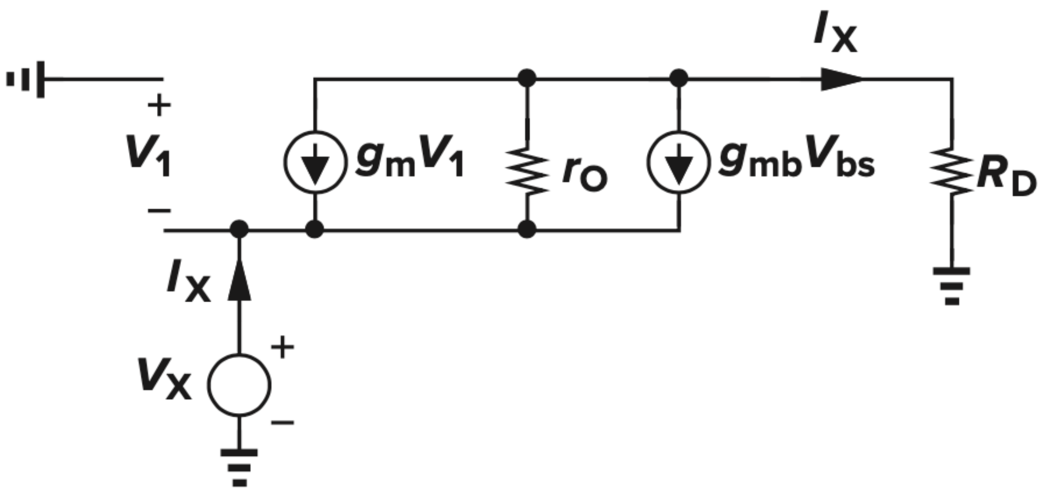
Input resistance of a CG stage





Input resistance of a CG stage



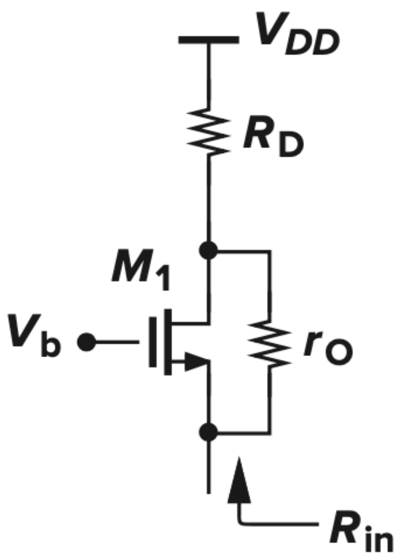


$$R_D I_X + r_O[I_X - (g_m + g_{mb})V_X] = V_X$$

$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}$$

$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}$$

Input resistance of a CG stage



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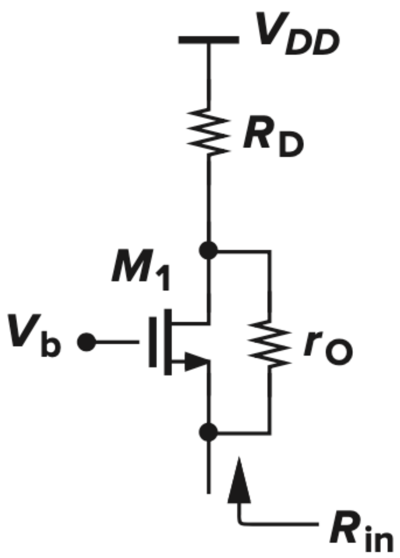
$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}$$

✓ the **drain impedance** is **divided** by $(g_m + g_{mb})r_O$ when seen at the **source**

Input resistance of a CG stage



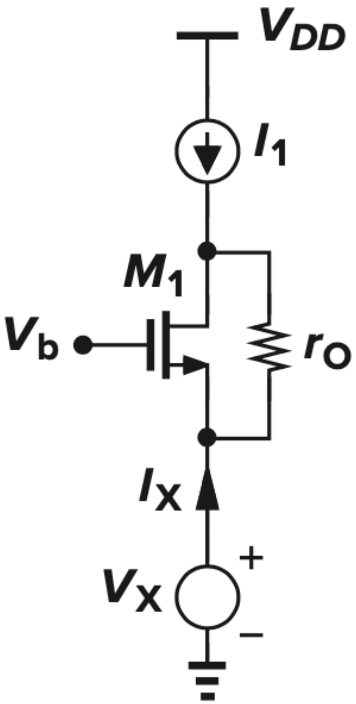
$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}$$
$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}$$

✓ the **drain impedance** is **divided** by $(g_m + g_{mb})r_O$ when seen at the **source**

$R_D = 0$ →

$$\frac{V_X}{I_X} = \frac{r_O}{1 + (g_m + g_{mb})r_O}$$
$$= \frac{1}{\frac{1}{r_O} + g_m + g_{mb}}$$

Input resistance of a CG stage

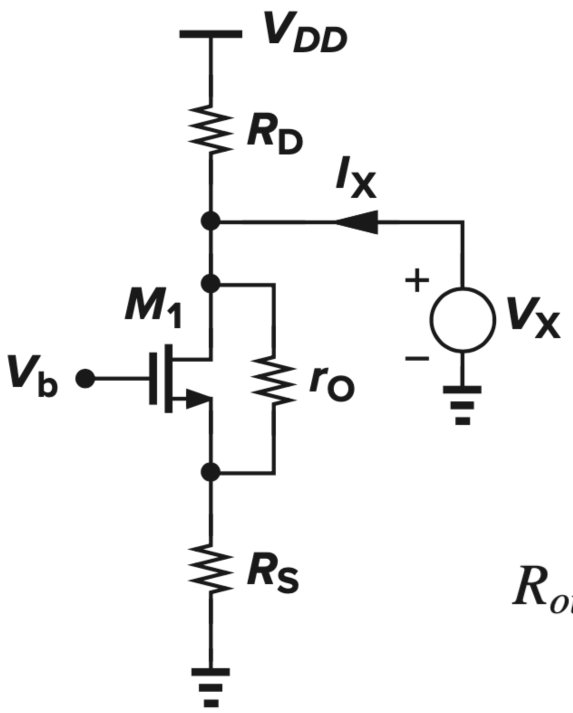


$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}$$

$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}$$

the input impedance approaches infinity

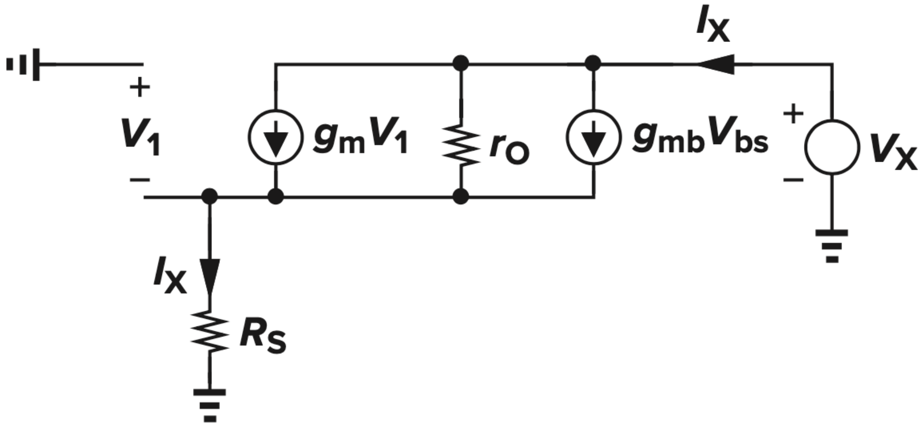
Output resistance of a CG stage

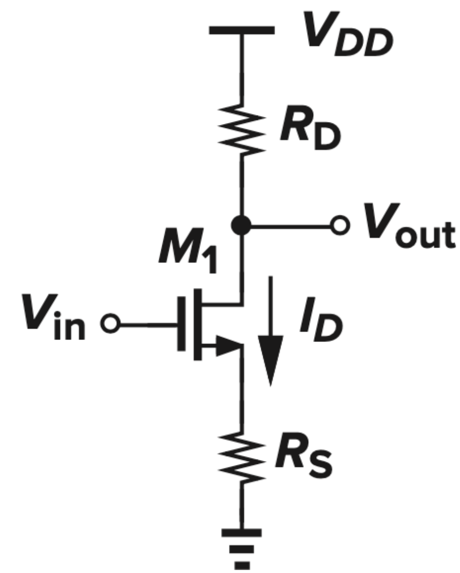


$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_S + r_O\} \| R_D$$

Recall: Output resistance of a degenerated CS

- Source degeneration **increases** the output resistance



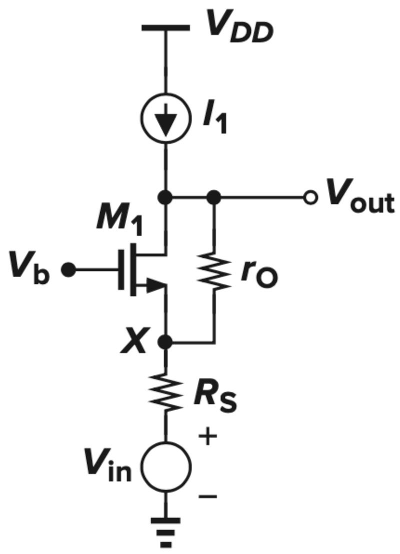


$$r_O[I_X + (g_m + g_{mb})R_S I_X] + I_X R_S = V_X$$

$$\begin{aligned} R_{out} &= [1 + (g_m + g_{mb})R_S]r_O + R_S \\ &= [1 + (g_m + g_{mb})r_O]R_S + r_O \\ &\approx (g_m + g_{mb})r_O R_S + r_O \\ &= [1 + (g_m + g_{mb})R_S]r_O \end{aligned}$$

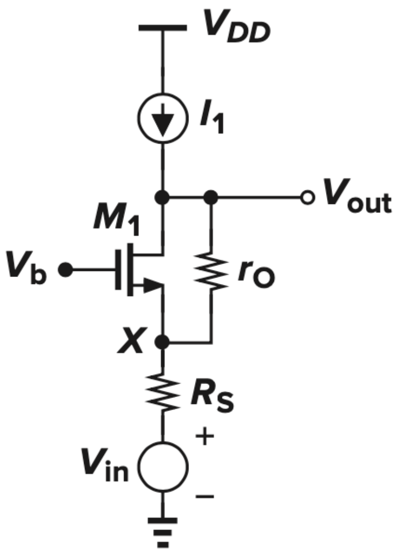
- **The overall output resistance is the parallel combination of R_{out} and R_D**

Example: Calculate the voltage gain



- A common-gate stage with a **current-source load**

Example: Calculate the voltage gain



- A common-gate stage with a current-source load

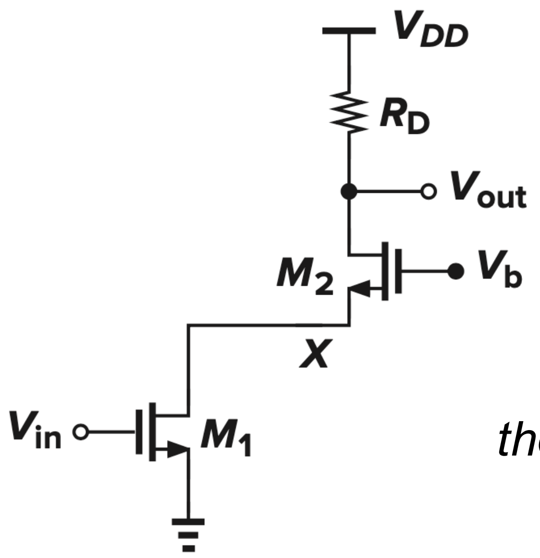
$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_D} R_D$$

$R_D \to \infty$

$$A_v = (g_m + g_{mb})r_O + 1$$

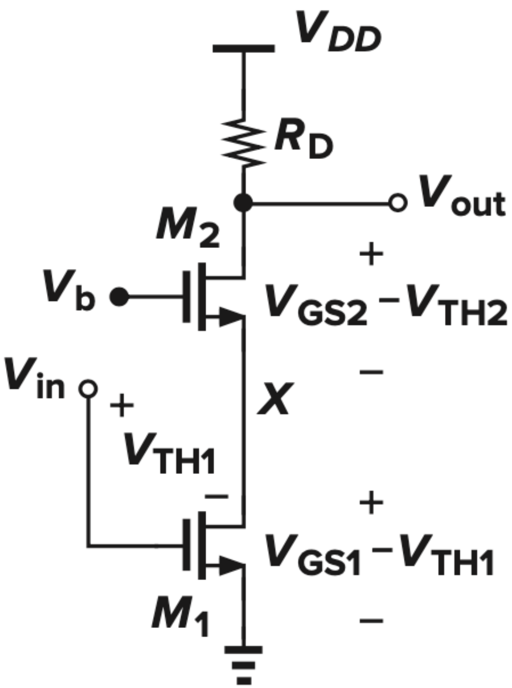
Cascode stage

- The cascade of a **CS stage and a CG stage** is called a "cascode" topology, providing many useful properties.



the "telescopic" cascode

Cascode: bias condition



$$V_b - V_{GS2} \geq V_{in} - V_{TH1}$$

$$V_{out} \geq V_b - V_{TH2}$$

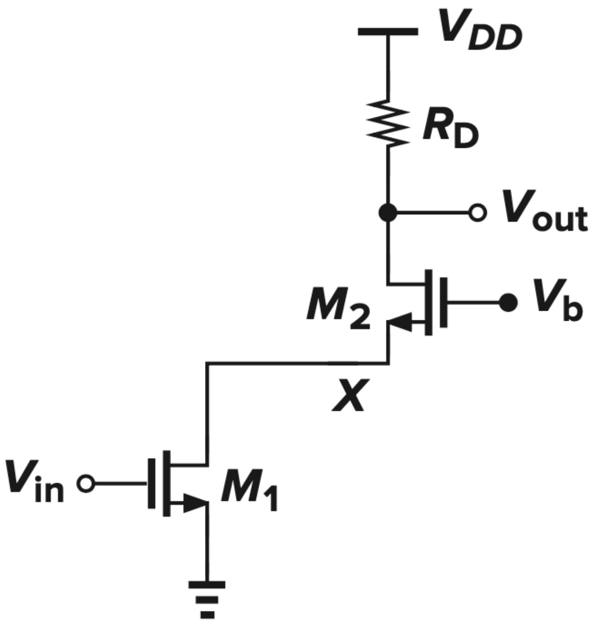
↓

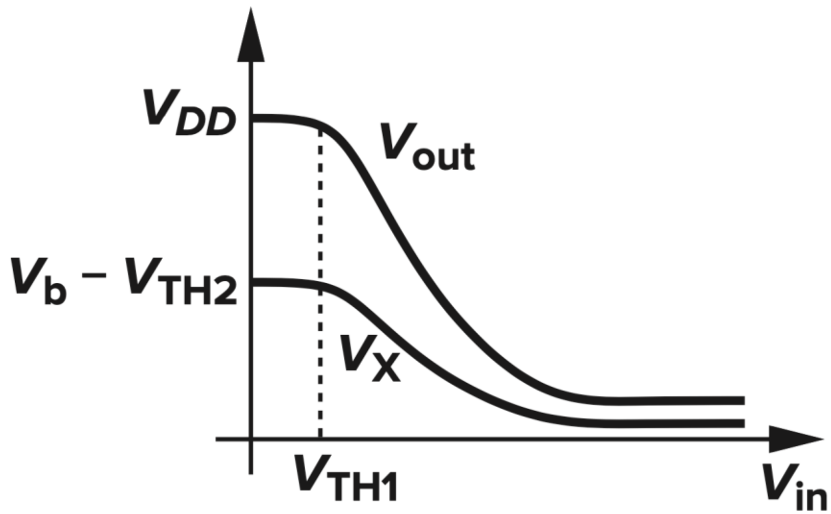
$$V_{out} \geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2}$$

$$= (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2})$$

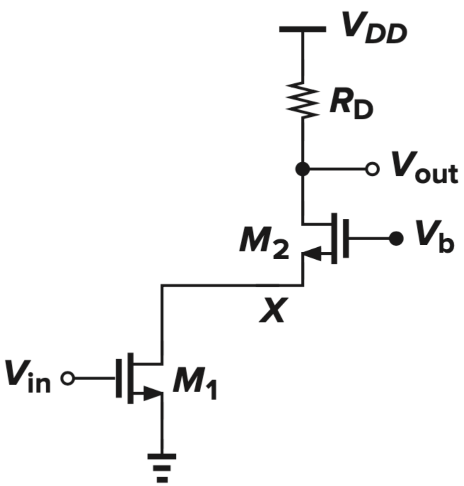
✓ the minimum output level for both transistors to operate in saturation is equal to the overdrive voltage of M_1 plus that of M_2

Cascode: large-signal behavior





Cascode stage: Small-signal model



$\lambda = 0$