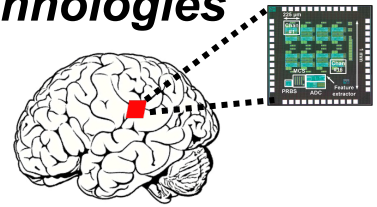
Integrated Neurotechnologies Laboratory

EPFL



Analog IC design (EE-320), Lecture 3

Prof. Mahsa Shoaran

Institute of Electrical and Micro Engineering, School of Engineering, EPFL

Review: MOS I/V Characteristics

$$\boxed{V_{DS} \leq V_{GS} - V_{TH}}$$

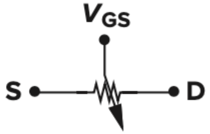
triode

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]}$$

or $V_{GD} > V_{TH}$

$$V_{DS} \ll 2(V_{GS} - V_{TH}) \longrightarrow R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

deep triode

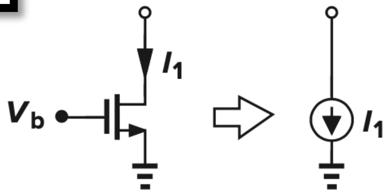


$$\boxed{V_{DS} > V_{GS} - V_{TH}}$$

saturation

$$\boxed{I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2}$$

or $V_{GD} < V_{TH}$

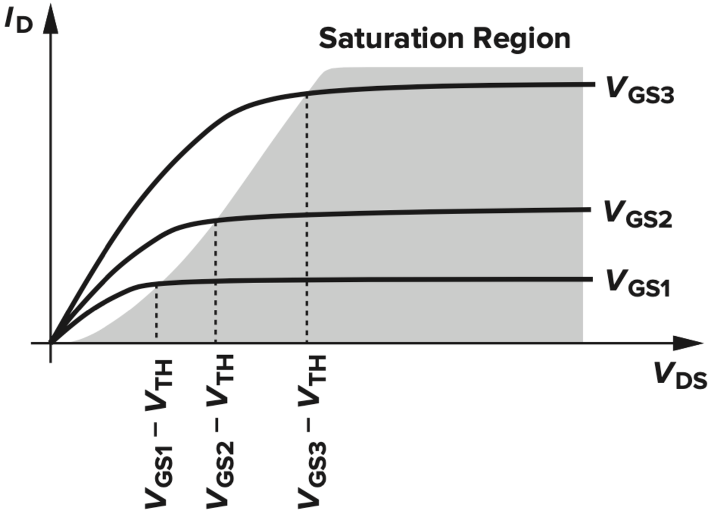


PMOS in saturation: $V_{GD} > V_{TH}$

triode: $V_{GD} < V_{TH}$ (V_{TH} is negative)

$$I_D = -\mu_p C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_D = -\frac{1}{2} \mu_p C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$$

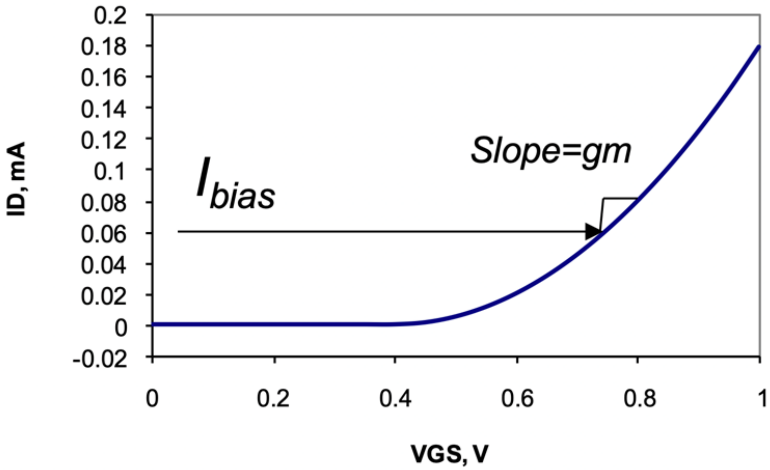


Review: MOS g_m in saturation

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS \text{ const.}}$$
$$= \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}$$
$$= \frac{2I_D}{V_{GS} - V_{TH}}$$

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$



Review: MOS g_m in saturation, second-order effects

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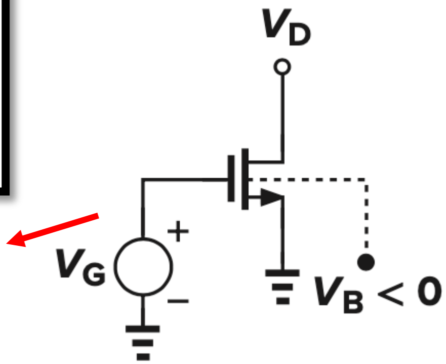
Body Effect

$$V_{TH} = V_{THO} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right)$$



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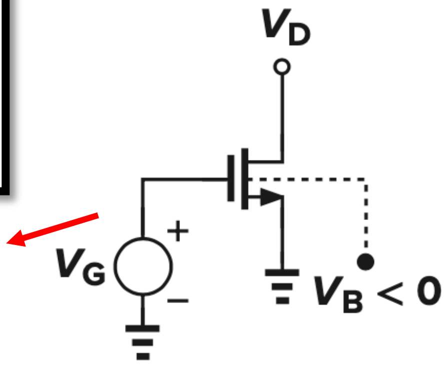
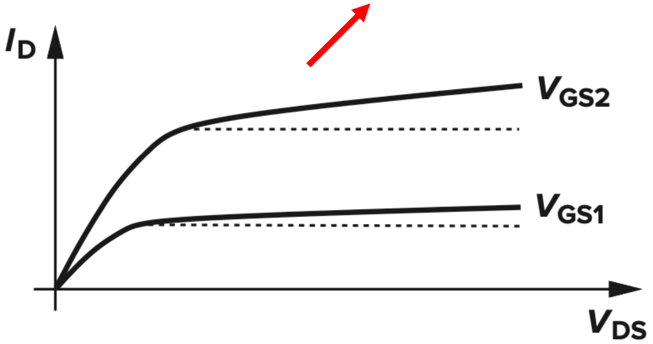


Body Effect

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right)$$

Channel-Length Modulation

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$



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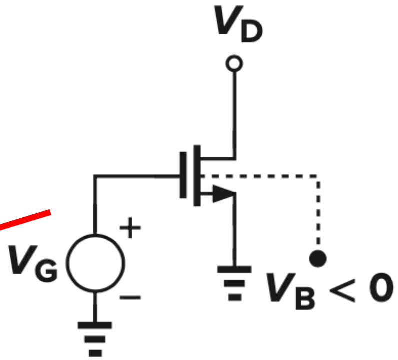

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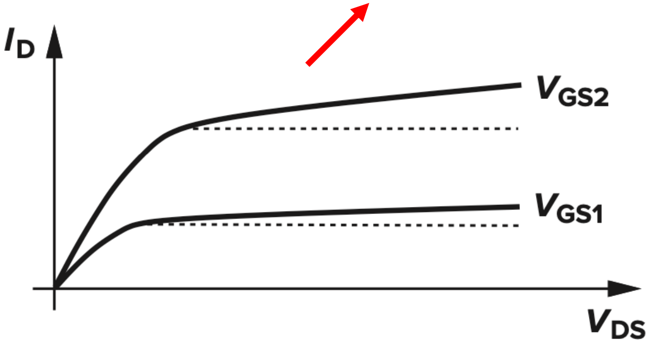
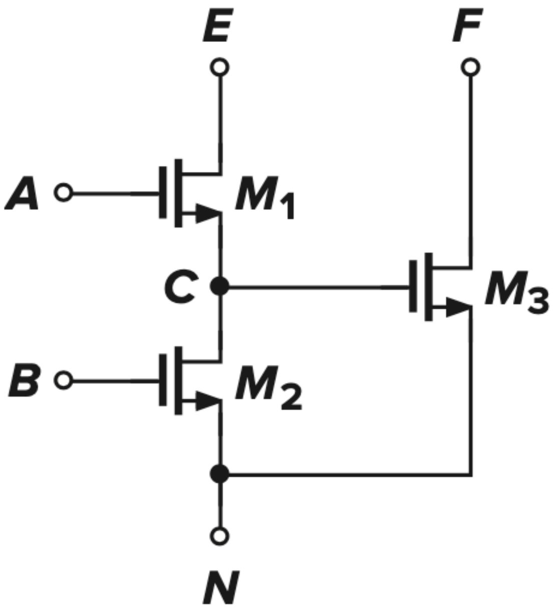
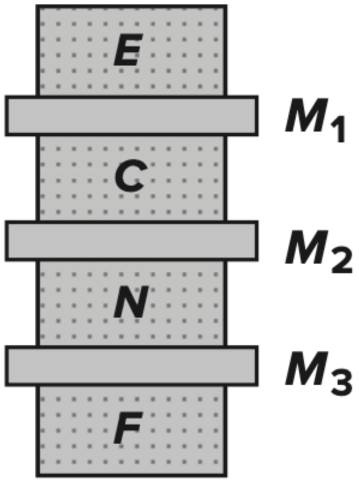


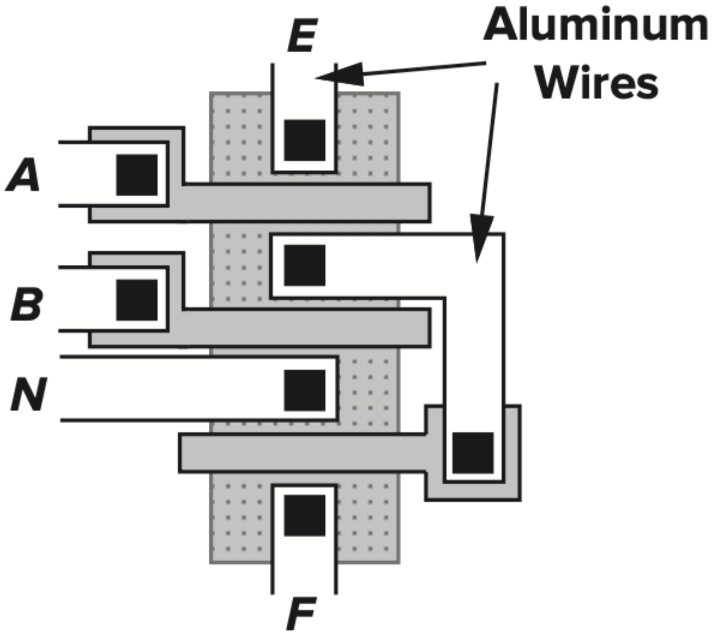
$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}) = \sqrt{2\mu_n C_{ox}(W/L) I_D (1 + \lambda V_{DS})}$$

MOS Device Layout

- The layout determined by both the electrical properties of the device and the "**design rules**" imposed by the **technology**
- ***W/L*** is chosen to set the transconductance or other circuit parameters while the **minimum *L*** is dictated by the process
- In addition to the gate, the source and drain areas must be defined properly







MOS Device Capacitances

- The basic quadratic I/V relationships along with corrections for body effect and channel-length modulation, provide some understanding of the **low-frequency** behavior of CMOS circuits

- In many analog circuits, however, the **capacitances** associated with the devices must also be taken into account to predict the **high-frequency** behavior as well

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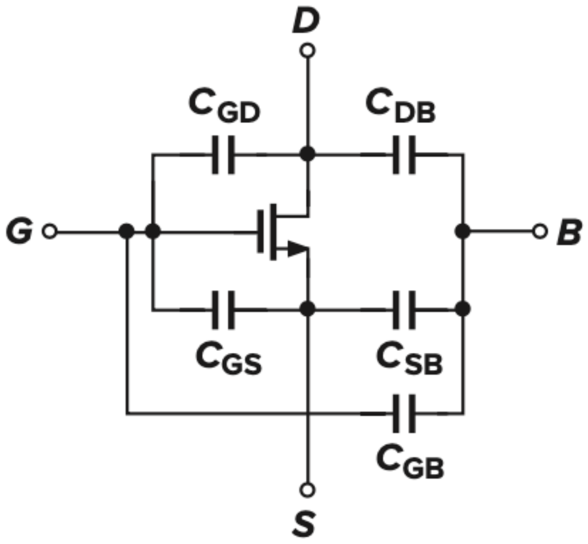
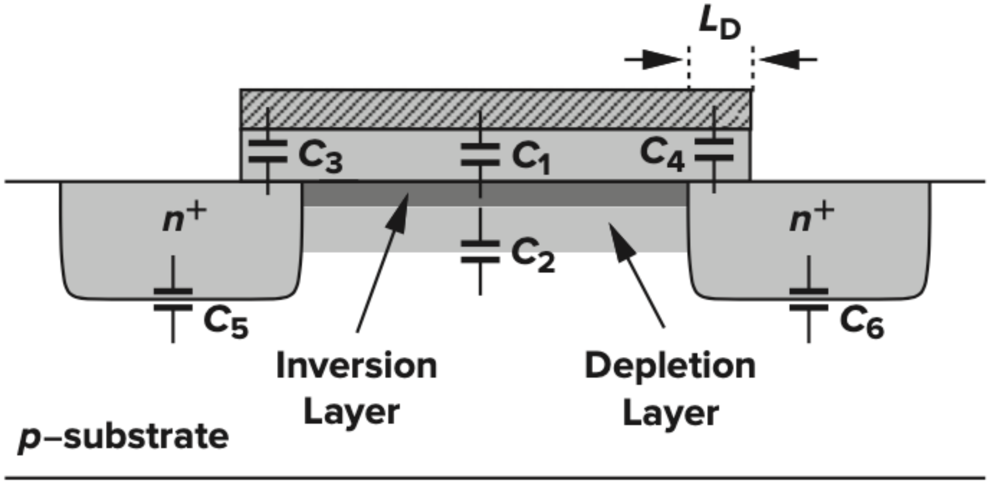
- In many analog circuits, however, the **capacitances** associated with the devices must also be taken into account to predict the **high-frequency** behavior as well
- Capacitance between each two of the four terminals of a MOS: the value may depend on the bias conditions of the transistor



MOS Device Capacitances



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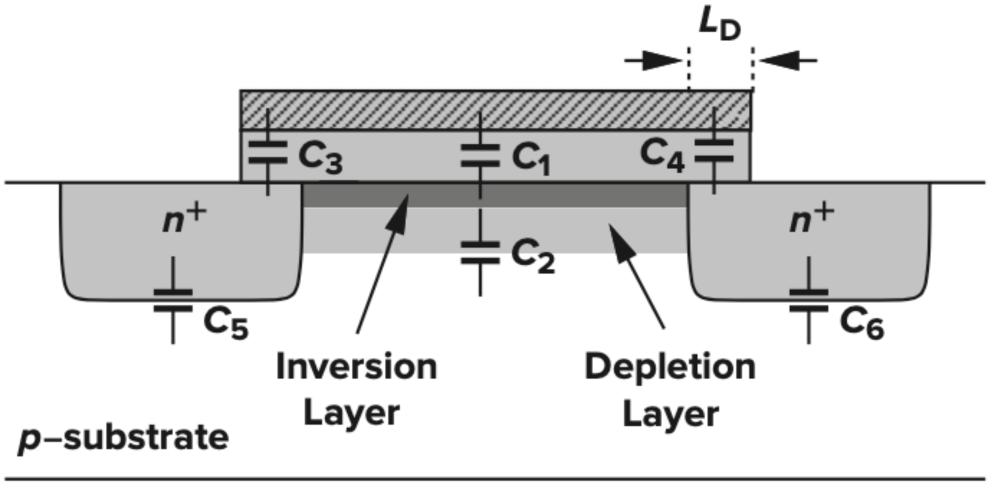
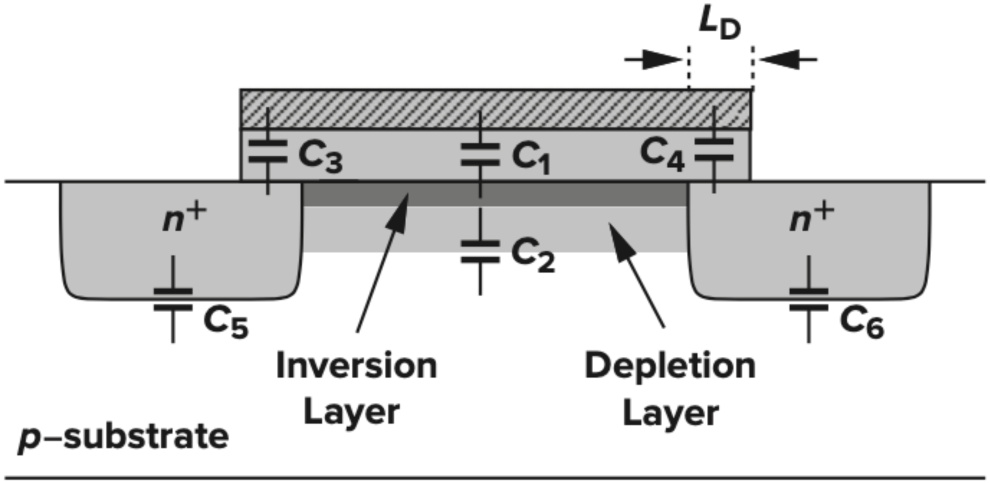


(1) the **oxide** capacitance between the **gate** and the **channel**

$$C_1 = WLC_{ox}$$

MOS Device Capacitances



(1) the **oxide** capacitance between the **gate** and the **channel**

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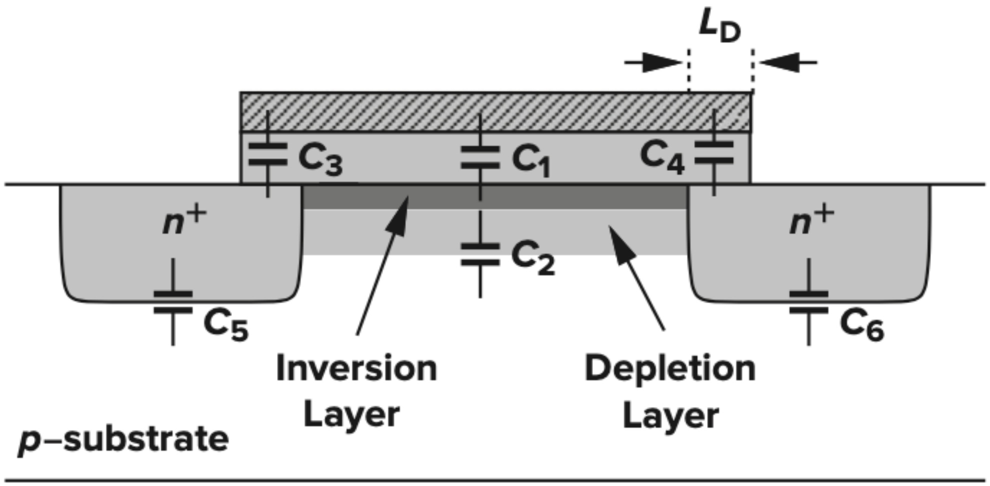
$$C_2 = WL\sqrt{q\epsilon_{si}N_{sub}/(4\Phi_F)}$$

MOS Device Capacitances



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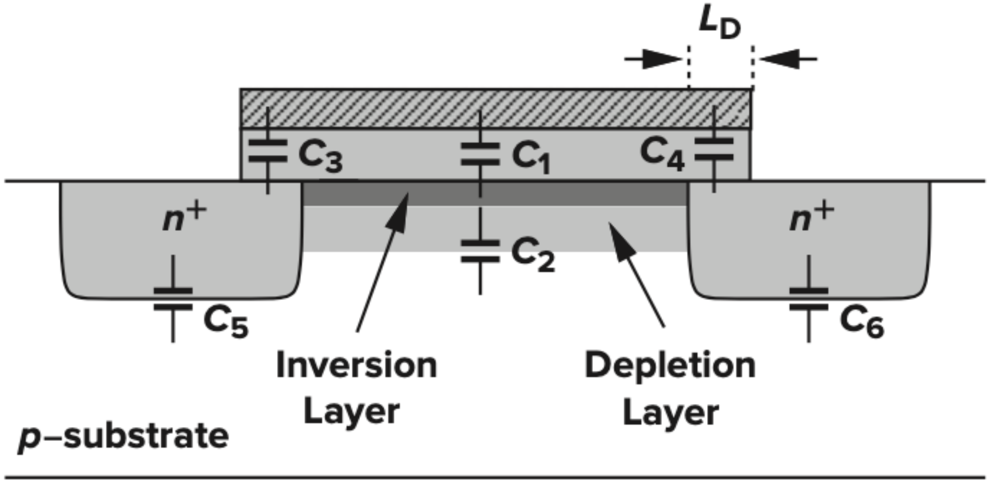
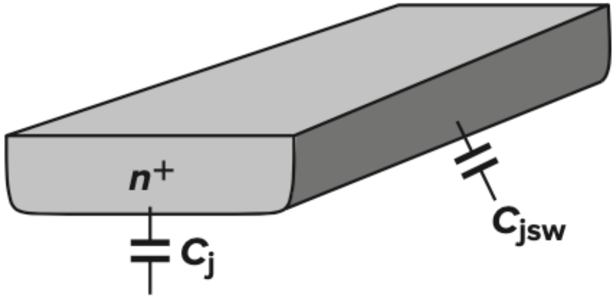
(3) the capacitance due to **overlap** of the **gate** poly with **source** and **drain**, C_3 and C_4

The overlap capacitance **per unit width**: C_{ov} in F/m (or fF/µm). Multiply C_{ov} by W to obtain the **gate-source and gate-drain overlap capacitances**

MOS Device Capacitances

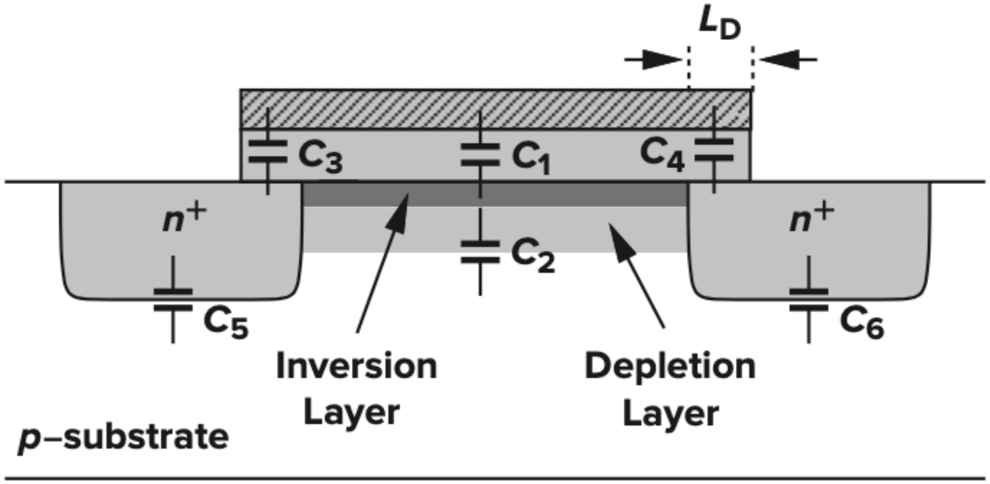


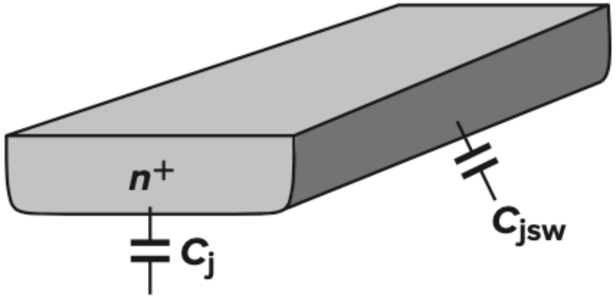


(4) The **junction capacitance** between the **S/D** areas and the **substrate**, it has two components: the **bottom-plate capacitance** at the bottom of the junction **C_j**, and the **sidewall capacitance** due to the perimeter of the junction, **C_{jsw}**

- C_j and C_{jsw} as capacitance per unit *area* (in F/m2) and unit *length* (in F/m)
- C_j is multiplied by the S/D **area**, and C_{jsw} by the S/D **perimeter**

MOS Device Capacitances





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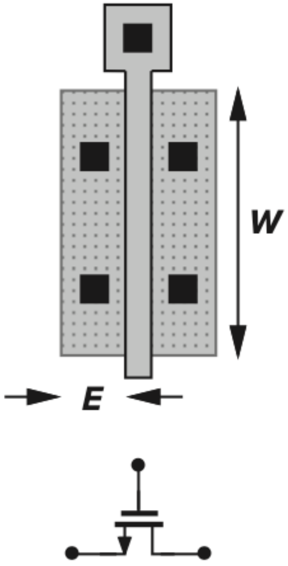
- Each **junction capacitance** can be expressed as $C_j = C_{j0}/[1 + V_R/(\Phi_B)]^m$

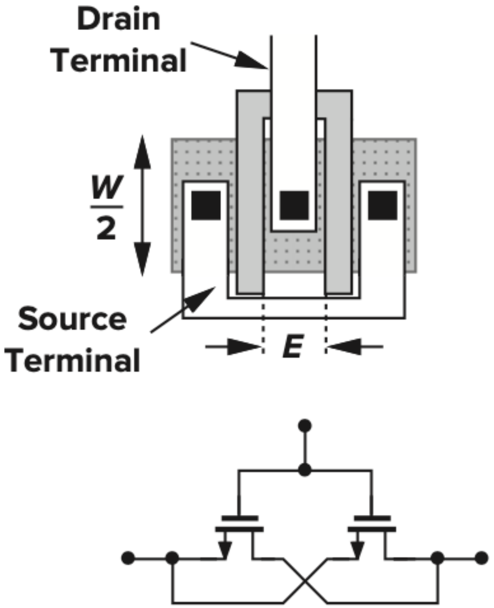
where V_R is the reverse voltage across the junction, Φ_B is the junction built-in potential, and m is a power typically in the range of 0.3 and 0.4

Example: MOS Device Capacitances

- Calculate the source and drain junction capacitances of the structures below:



(a)



(b)

Example: MOS Device Capacitances

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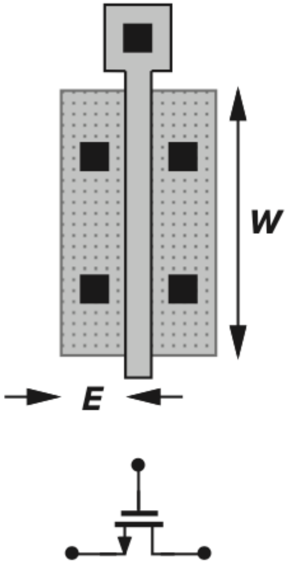

(a)

$$C_{DB} = C_{SB} = WEC_j + 2(W + E)C_{jsw}$$

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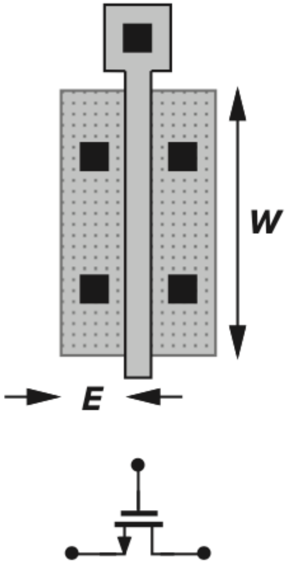

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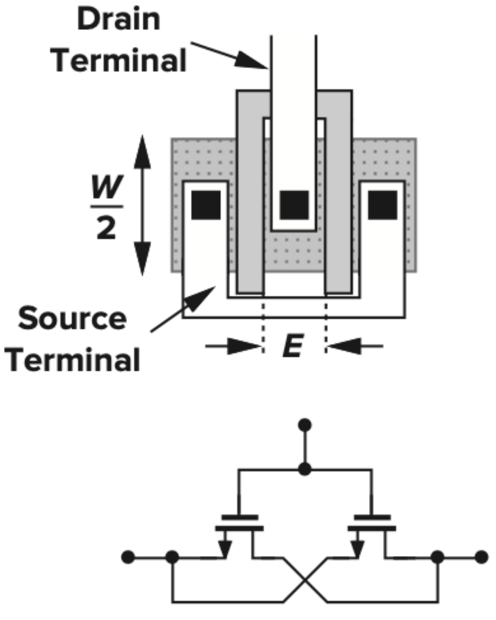

(b)

$$C_{DB} = \frac{W}{2} E C_j + 2\left(\frac{W}{2} + E\right) C_{jsw}$$

$$C_{SB} = 2\left[\frac{W}{2} E C_j + 2\left(\frac{W}{2} + E\right) C_{jsw}\right]$$

$$= W E C_j + 2(W + 2E) C_{jsw}$$

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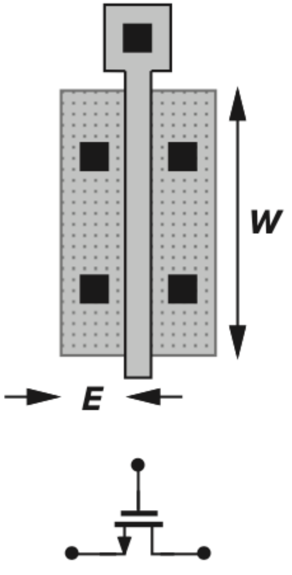

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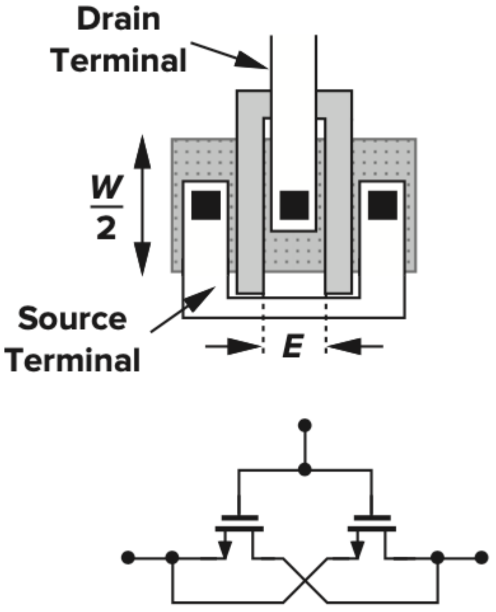

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$$C_{DB} = \frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw}$$

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$$= WEC_j + 2(W + 2E)C_{jsw}$$

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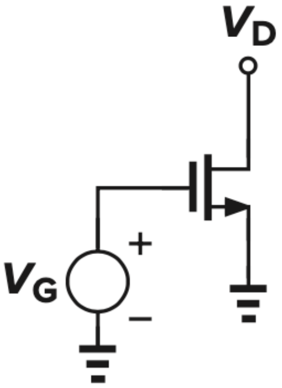
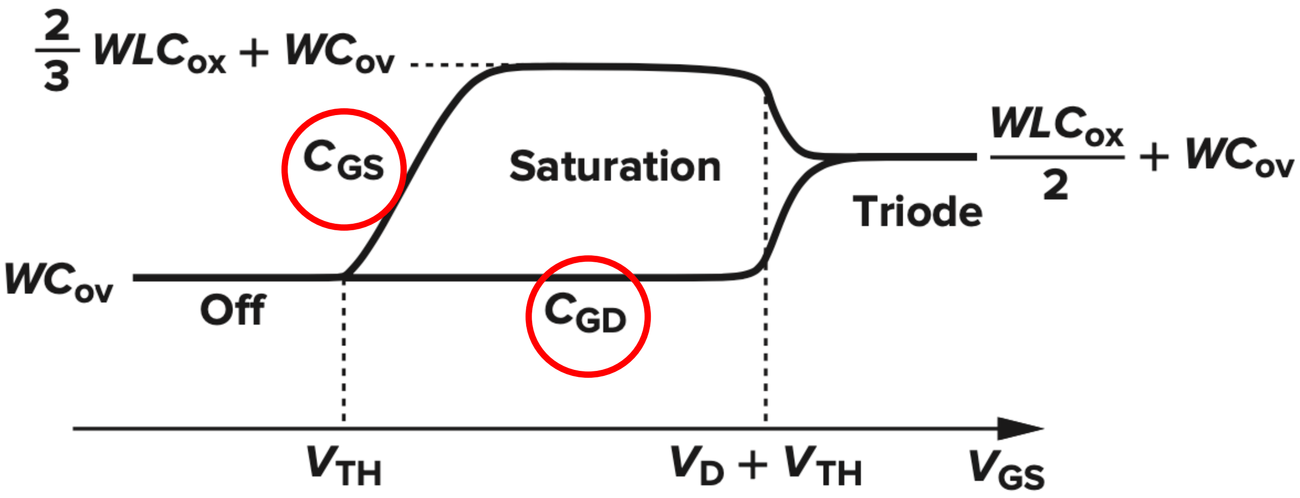
a "folded" structure (b) has substantially **less drain junction capacitance** than (a) while providing the same *W*/*L*

MOS Capacitances in different regions





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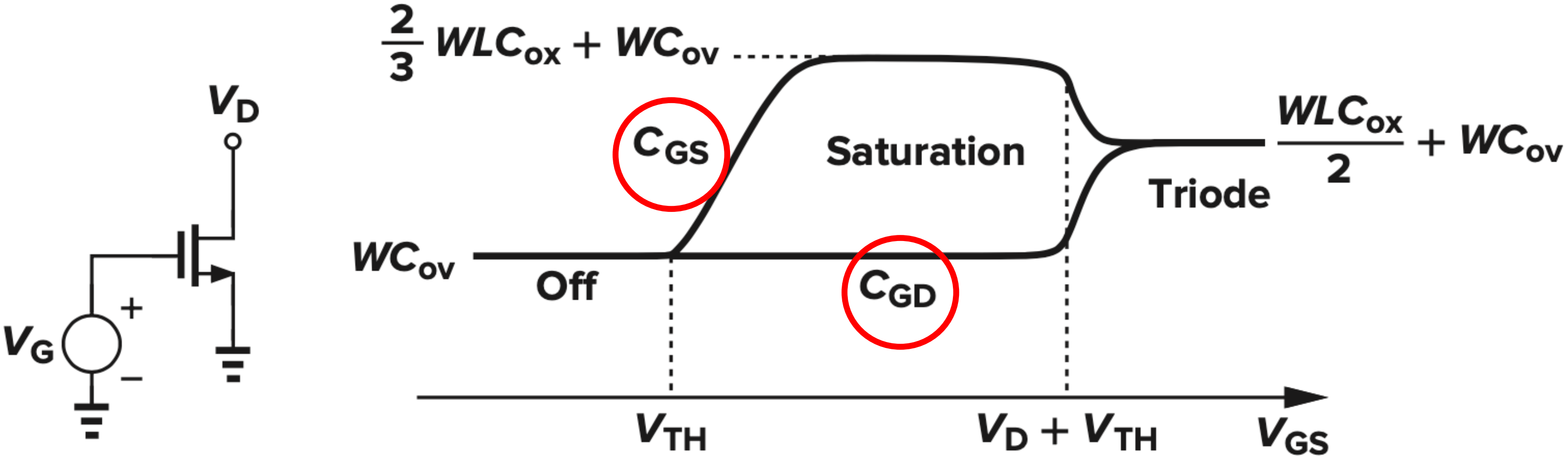

- If the device is **off**, $C_{GD} = C_{GS} = C_{ov}W$, and the **gate-bulk** capacitance consists of the series combination of the gate-oxide capacitance and the depletion-region capacitance, i.e., $C_{GB} = (WLC_{ox})C_d/(WLC_{ox} + C_d)$, where L is the effective length

$$C_d = WL\sqrt{q\epsilon_{si}N_{sub}/(4\Phi_F)}$$

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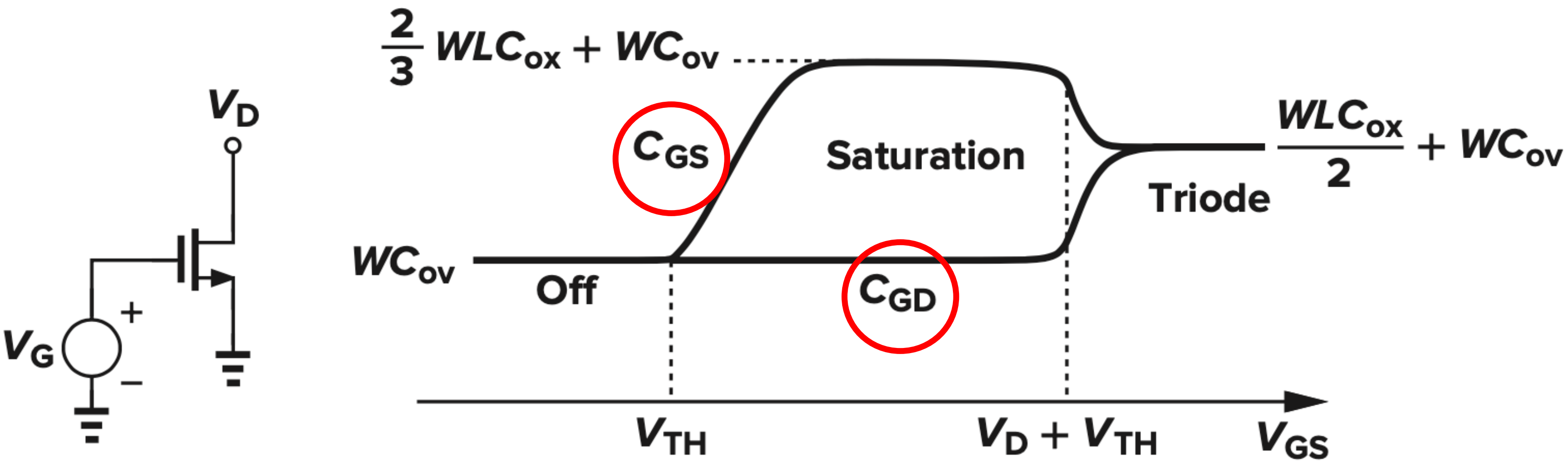

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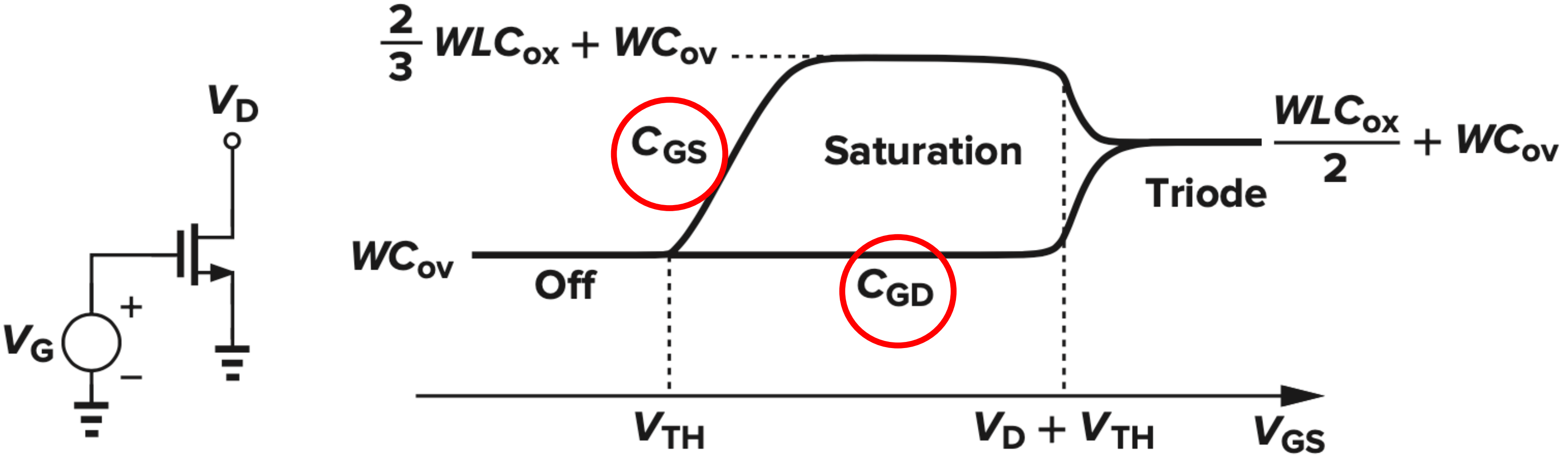

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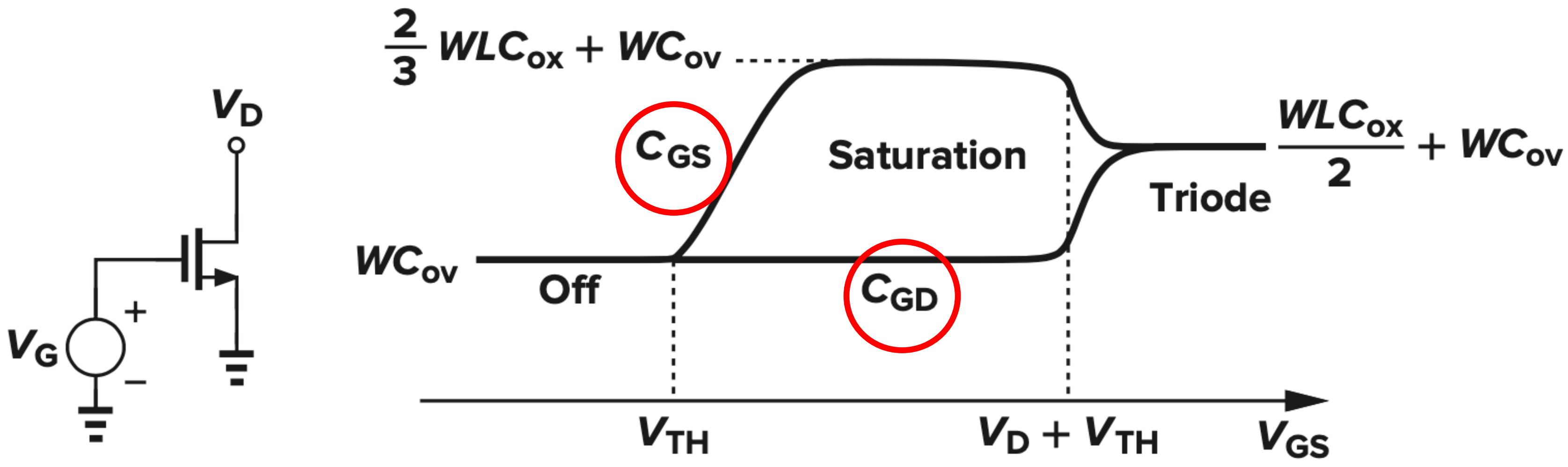
- In **deep triode**, (S and D at approximately equal voltages), the **gate-channel** capacitance, WLC_{ox}, is divided equally between the G and S and the G and D, since a change of G voltage draws equal charge from S and D:

$$\boxed{C_{GD} = C_{GS} = WLC_{ox}/2 + WC_{ov}}$$

MOS Capacitances in different regions



- If in **saturation**, the MOS exhibits a **gate-drain** capacitance roughly equal to WC_{ov}

- For $\boldsymbol{C_{GS}}$, the potential difference between gate and channel varies from V_{GS} at the source to V_{TH} at the pinch-off point, resulting in a nonuniform vertical electric field in the gate oxide from S to D

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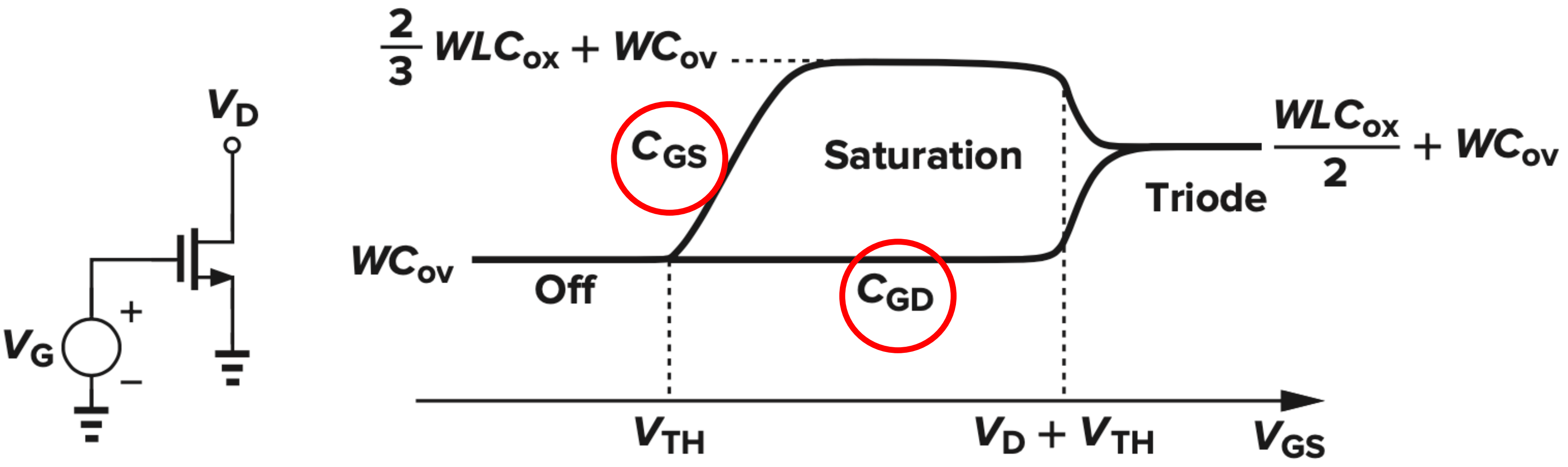

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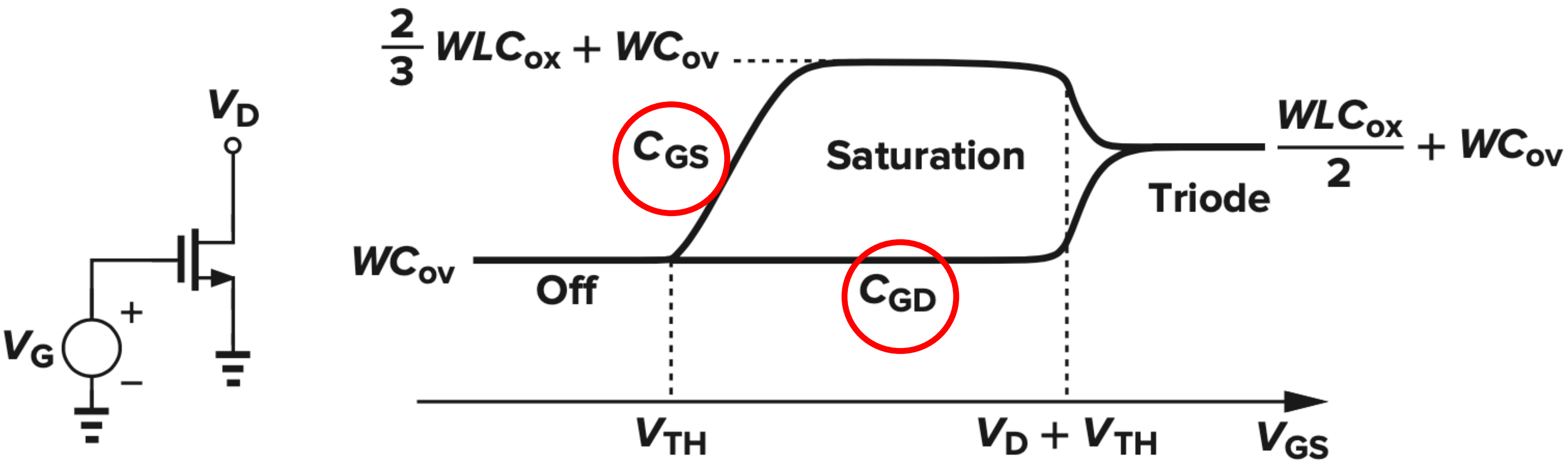
- It can be proved that the equivalent capacitance, excluding the gate-source overlap capacitance, equals $(2/3)WLC_{ox}$ → $\boxed{C_{GS} = 2WL_{eff}C_{ox}/3 + WC_{ov}}$

MOS Capacitances in different regions



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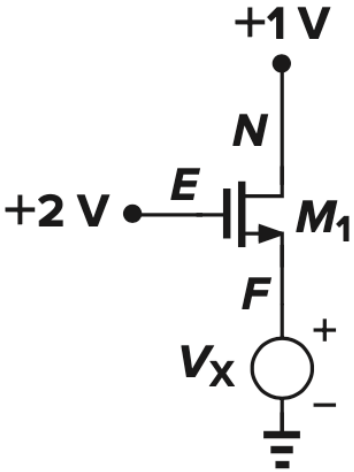
- The **gate-bulk** capacitance is usually neglected in **triode** and **saturation** because the inversion layer acts as a “shield” between G and B

Example: MOS Capacitances in different regions

- Sketch the capacitances of M_1 as V_X varies from zero to 3 V. Assume that $V_{TH} = 0.3$ V and $\lambda = \gamma = 0$.



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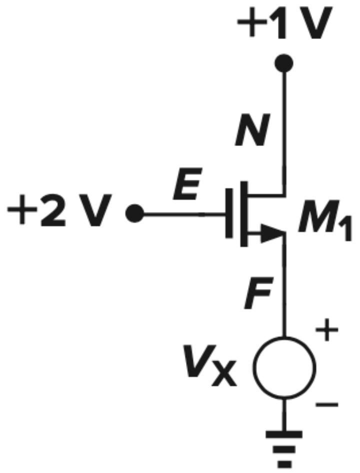
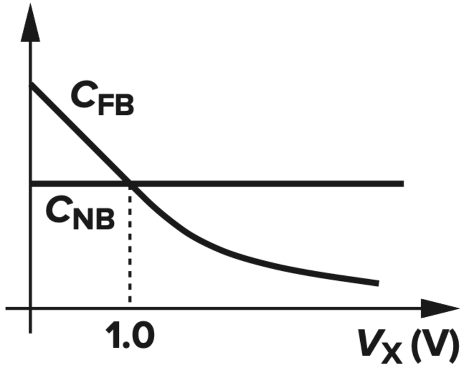


$$C_j = C_{j0}/[1 + V_R/(\Phi_B)]^m$$



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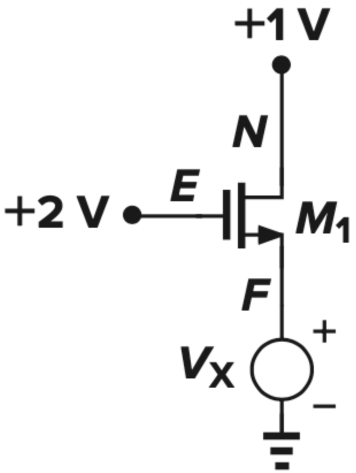
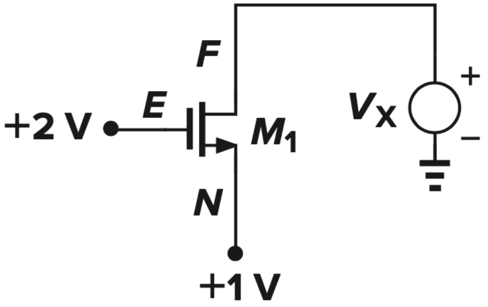
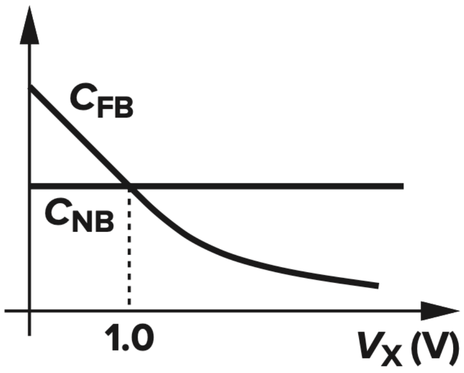


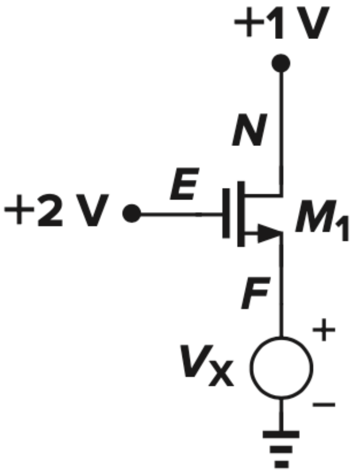
As V_X exceeds 1 V, the role of the S and D is exchanged:





Example: MOS Capacitances in different regions

- Sketch the capacitances of M_1 as V_X varies from zero to 3 V. Assume that $V_{TH} = 0.3$ V and $\lambda = \gamma = 0$.



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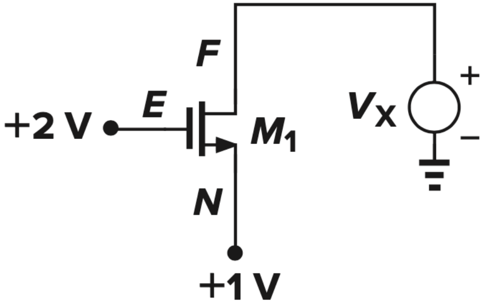
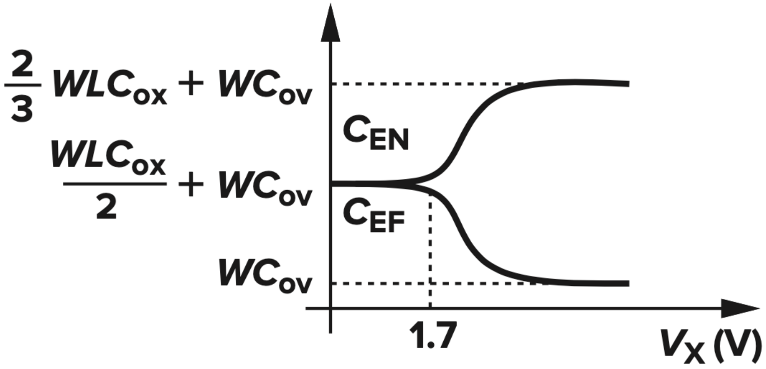
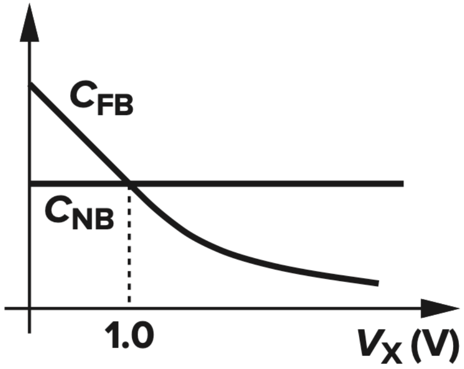






Small-Signal model of MOS

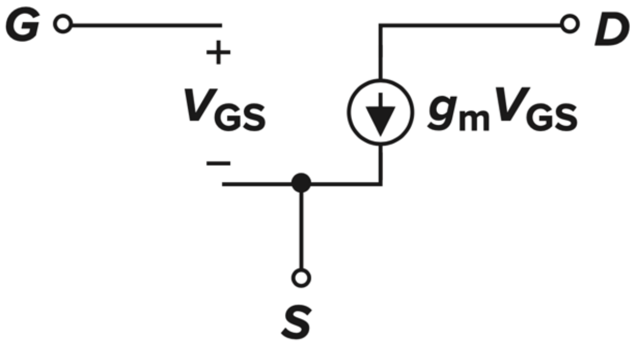
- The “**large-signal**” behavior of NMOS devices, to predict the drain current for arbitrary voltages applied to the G, S, and D, but
  - nonlinear nature of large-signal models: difficult to analyze

  - if the perturbation in bias conditions is **small**, a “**small-signal**” model (an approximation of the large-signal model around the operating point), can simplify the calculations

- Since in many analog circuits, MOSFETs are biased in the saturation region, we derive the **small-signal model** for **saturation**

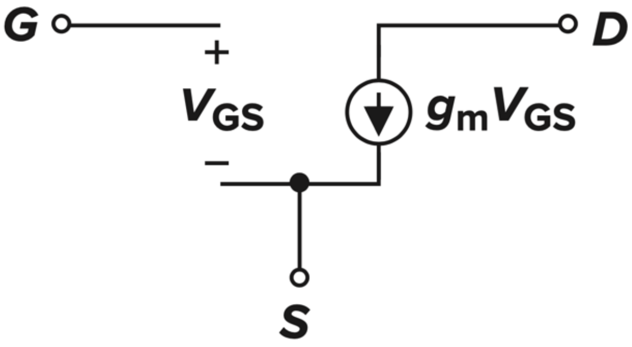
- For MOS operating as a switch: a **linear resistor** together with capacitances

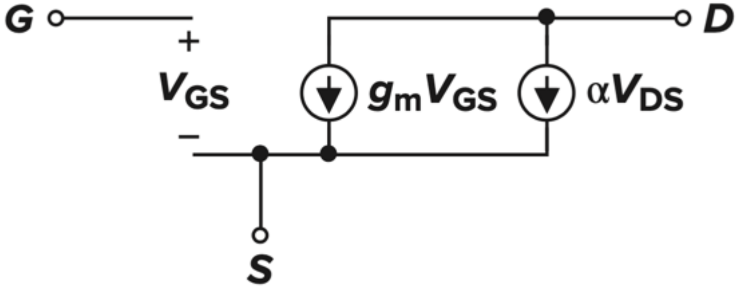
Small-Signal model of MOS

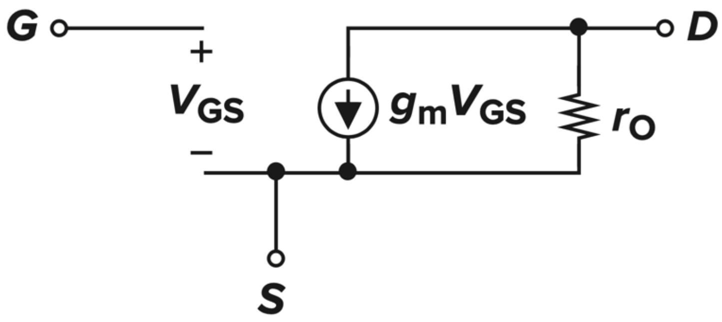


Small-Signal model of MOS

Small-Signal model of MOS

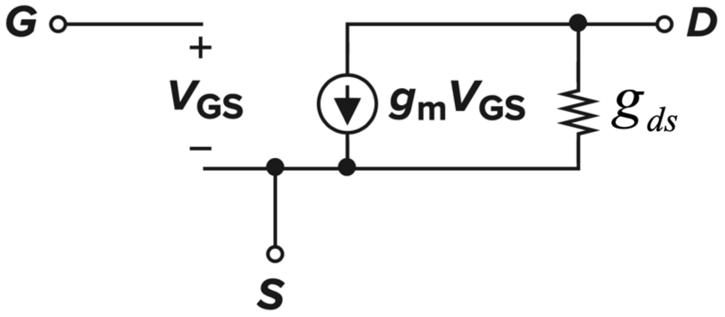




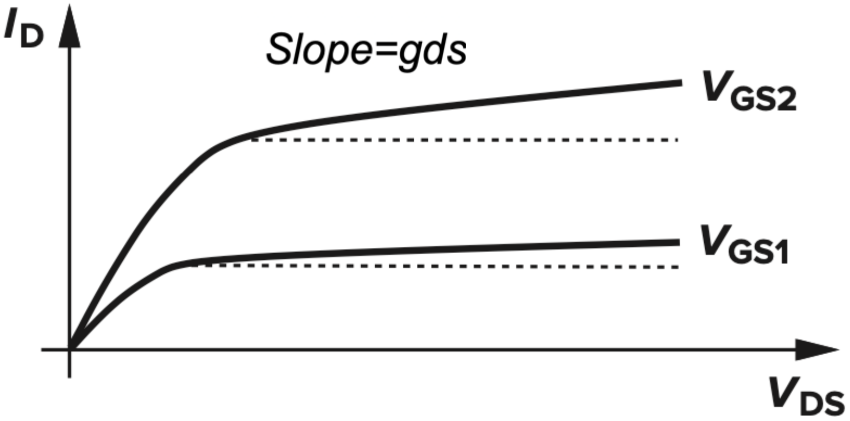


$$
\begin{aligned}
r_O &= \frac{\partial V_{DS}}{\partial I_D} \\
&= \frac{1}{\partial I_D / \partial V_{DS}} \\
&= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \cdot \lambda} \\
&\approx \frac{1+\lambda V_{DS}}{\lambda I_D} \\
&\approx \frac{1}{\lambda I_D}
\end{aligned}
$$

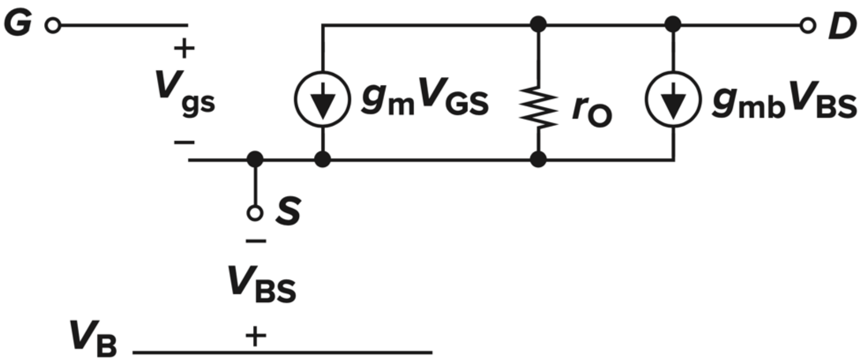
Small-Signal model of MOS (less common)



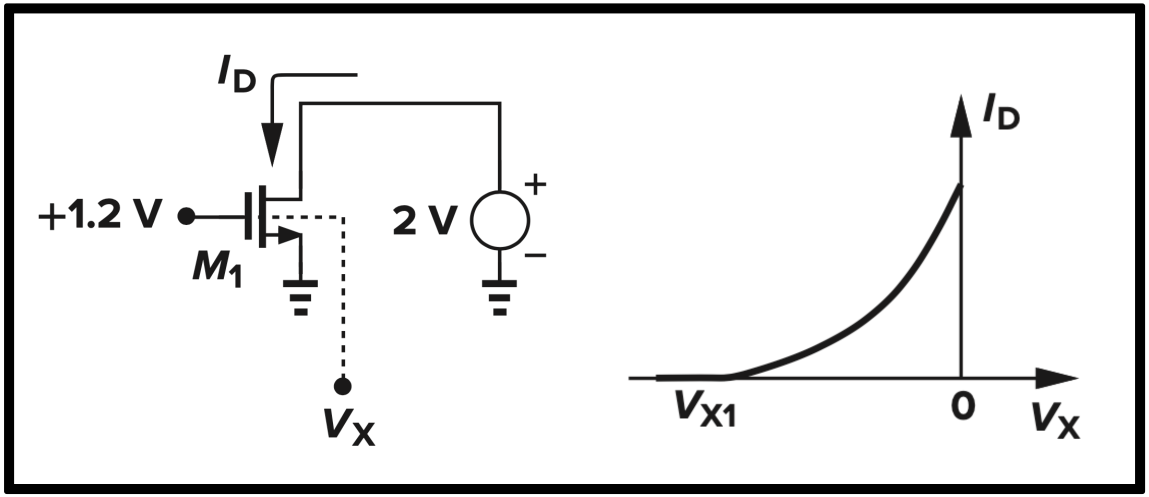
$$\boxed{g_{ds} = \frac{\partial I_D}{\partial V_{DS}}}$$



Small-Signal model of MOS with body effect



$$\boxed{V_{TH} = V_{THO} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right)}$$



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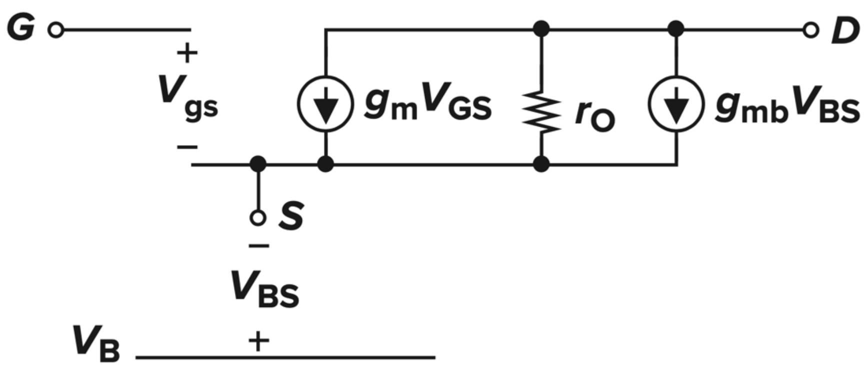
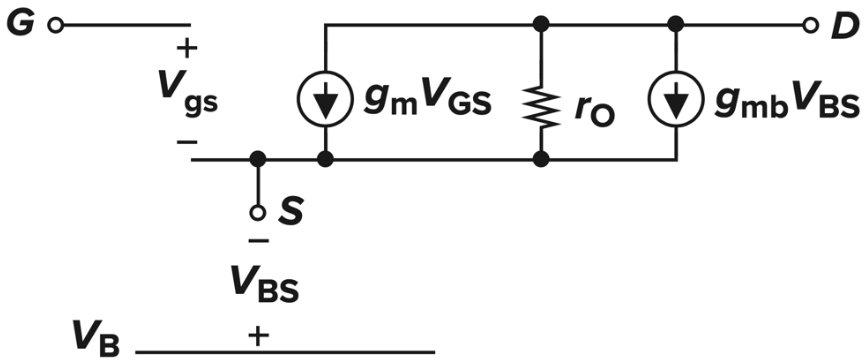


$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$$

$$= \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right)$$

Small-Signal model of MOS with body effect



$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$$

$$= \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \left(-\frac{\partial V_{TH}}{\partial V_{BS}} \right)$$

$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}}$$

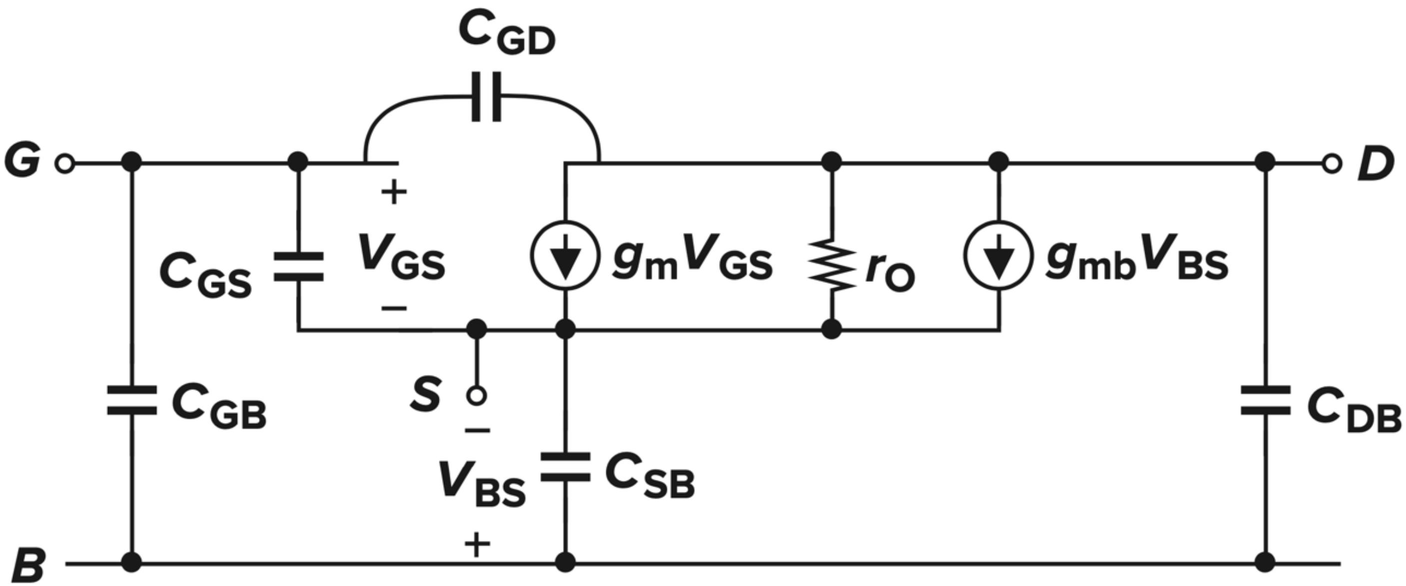
$$= -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2}$$

$$\boxed{V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|} \right)}$$

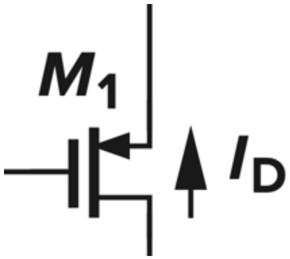
- g_m V_{GS} and $g_{mb}V_{BS}$ have **the same polarity**

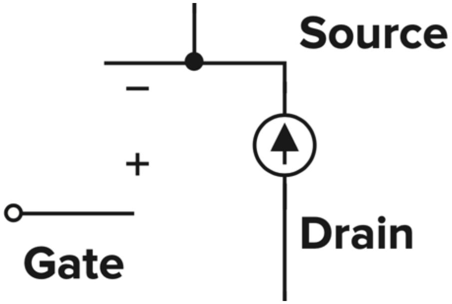
$$\boxed{\begin{aligned} g_{mb} &= g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} \\ &= \eta g_m \end{aligned}}$$

Complete MOS small-signal model



PMOS small-signal model





Signal Amplification

An essential function in most analog circuits

- We amplify an analog or digital signal because
  - it may be too small to drive a load
  - overcome the noise of a subsequent stage
  - provide logical levels to a digital circuit
  - …

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  - it may be too small to drive a load
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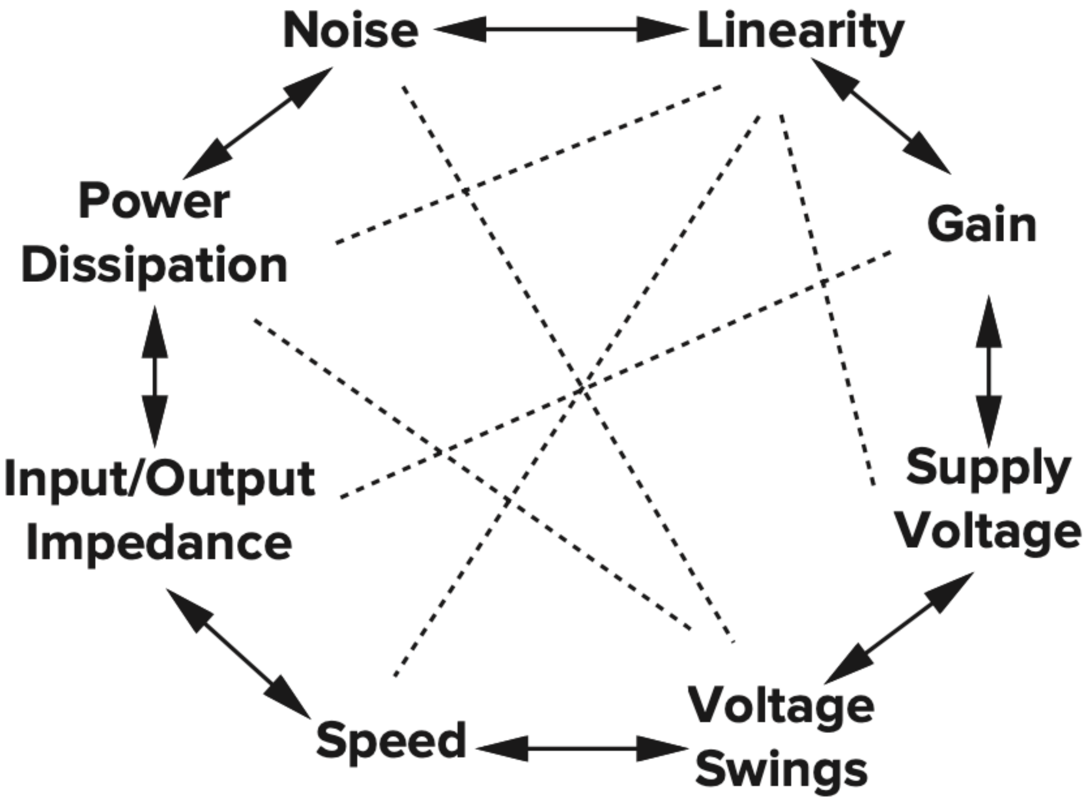
  - …

- Four types of amplifiers:
  - **common-source**
  - **common-gate**
  - **source follower**
  - **cascodes**

Analog design tradeoffs



Noise

Linearity

Power Dissipation

Gain

Input/Output Impedance

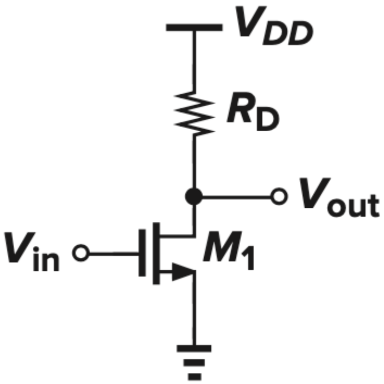
Supply Voltage

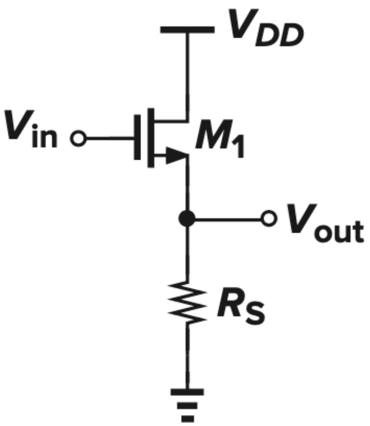
Speed

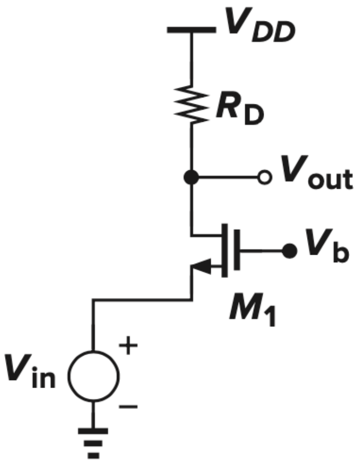
Voltage Swings

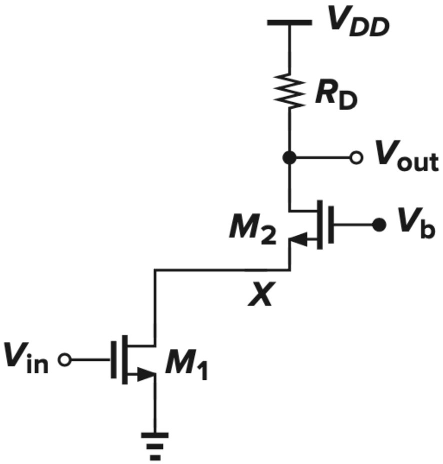
Amplifier topologies

Common-Source Stage	Source Follower	Common-Gate Stage	Cascode
With Resistive Load	With Resistive Bias	With Resistive Load	Telescopic
With Diode-Connected Load	With Current-Source Bias	With Current-Source Load	Folded
With Current-Source Load			
With Active Load			
With Source Degeneration			



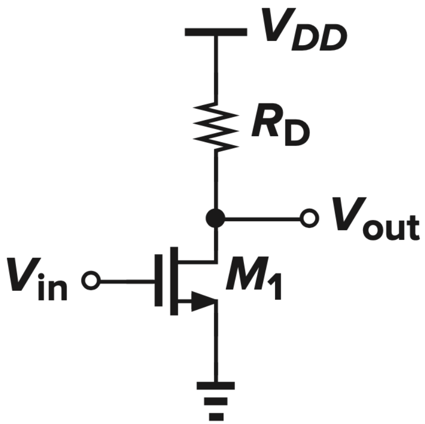






Common-Source Stage - with Resistive Load

- The **common-source** topology: receives the input at the **gate** and produces the output at the **drain**



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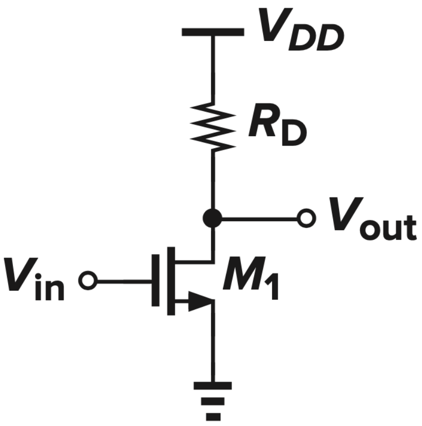
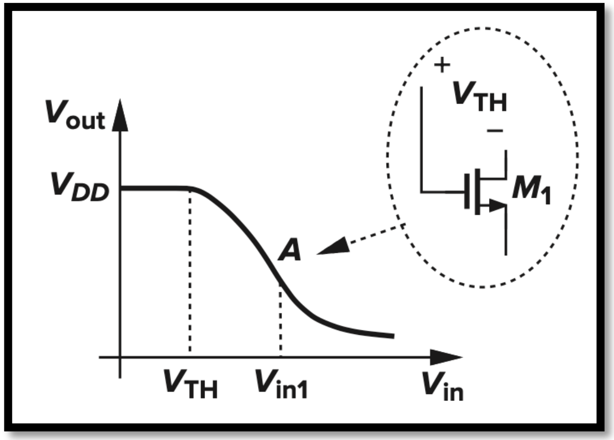


$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})^2$$ *(saturation)*

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{TH})^2$$

↓ *(triode)*

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right]$$



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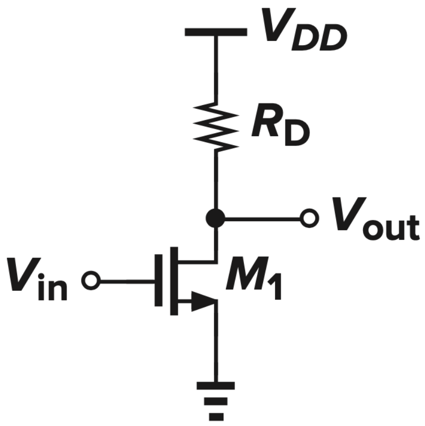


$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2$$ *(saturation)*

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{TH})^2$$

$\downarrow$ *(triode)*

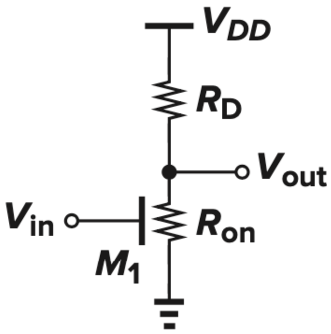
$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right]$$

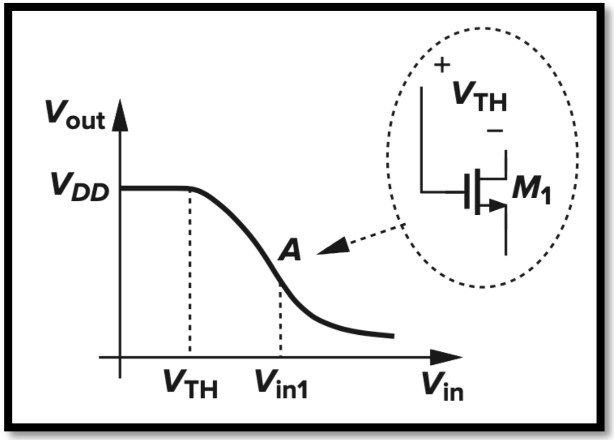
$$V_{out} \ll 2(V_{in} - V_{TH})$$

$$V_{out} = V_{DD}\frac{R_{on}}{R_{on} + R_D}$$

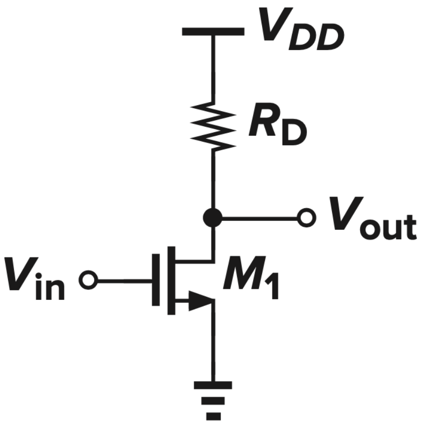
$$= \frac{V_{DD}}{1 + \mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})}$$

$\rightarrow$





Common-Source Stage - with Resistive Load



$$\boxed{V_{out} > V_{in} - V_{TH}}$$

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

$$\begin{aligned} A_v &= \frac{\partial V_{out}}{\partial V_{in}} \\ &= -R_D \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) \\ &= -g_m R_D \end{aligned}$$

small-signal model: