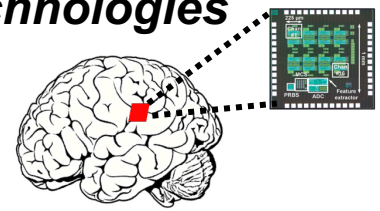
Integrated Neurotechnologies Laboratory

EPFL



Analog IC design (EE-320), Lecture 1

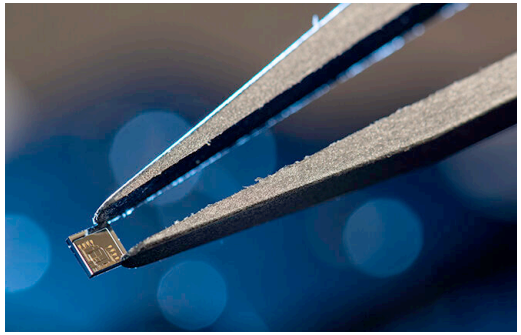
Prof. Mahsa Shoaran

Institute of Electrical and Micro Engineering, School of Engineering, EPFL

Analog IC design

Summary

Introduction to the design of analog CMOS integrated circuits at the transistor level. Understanding and design of basic structures.



Content

- Review of physics of MOS transistor
- MOS transistor: operating modes, large and small signal models, parasitic effects
- Basic building blocks for linear analog integrated circuits: single-stage amplifiers, current mirrors, differential pairs, and cascodes
- Transistor-level design of operational transconductance amplifiers
- Frequency response of amplifiers
- Layout techniques for analog integrated circuits

Lire la suite ▲

Keywords

Transistor, CMOS, analog integrated circuit

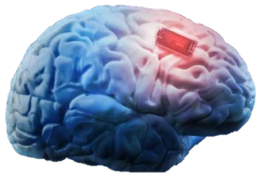
Learning Prerequisites

RECOMMENDED COURSES

Electronics I and II

About the Instructor

- Prof Mahsa Shoaran
  - **Integrated Neurotechnologies Lab (INL)**
    - Institute of Electrical and Micro Engineering (IEM)
    - Neuro-X Institute (Campus Biotech)
  - 2017-2019: Assistant Prof at **Cornell University**, NY, USA



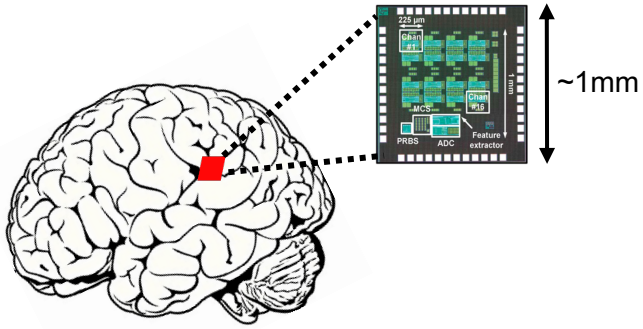
EPFL SCHOOL OF ENGINEERING ELECTRICAL ENGINEERING

Institute of Electrical and Micro Engineering

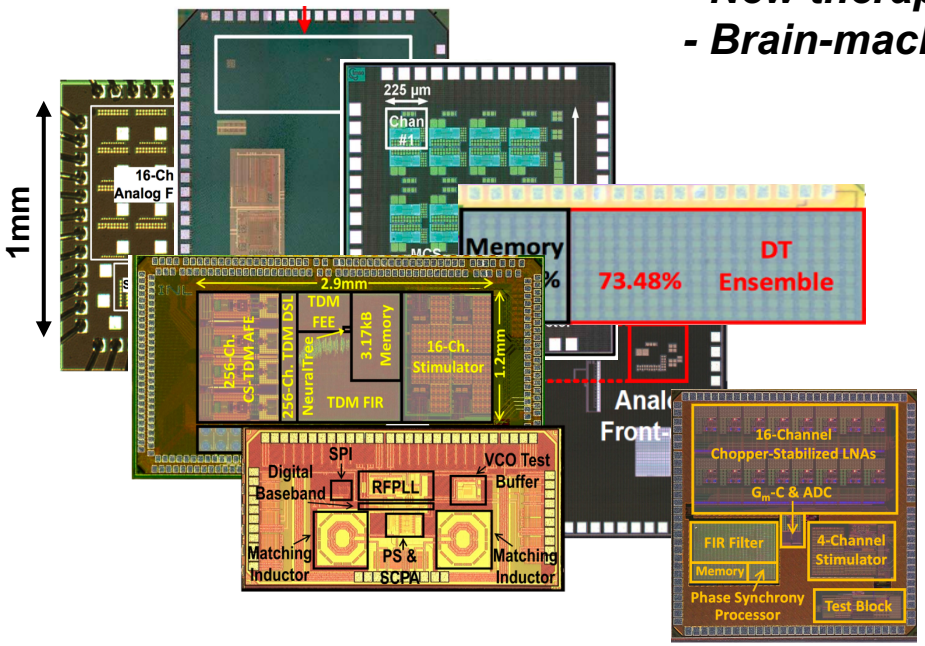
Neuro-X Institute

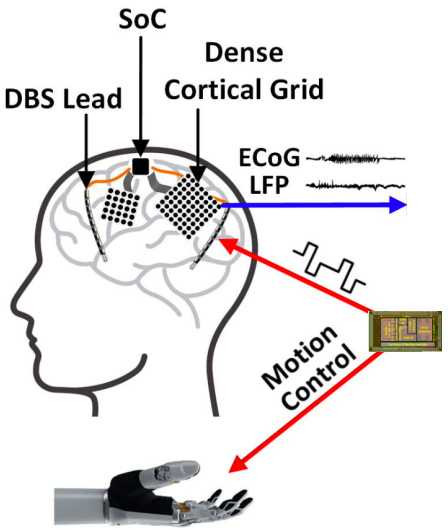
What we do: Neural Interface IC Design

- **Analog/digital/mixed-signal IC design**
- Neural signal processing
- Machine learning, integrated on chip



- New therapeutic devices for brain disorders
- Brain-machine interfaces



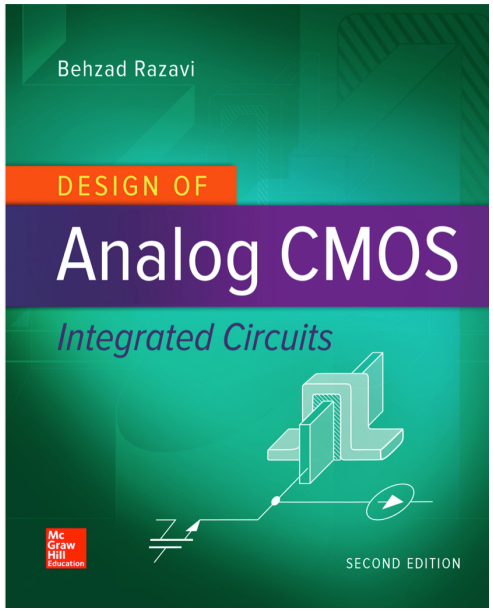


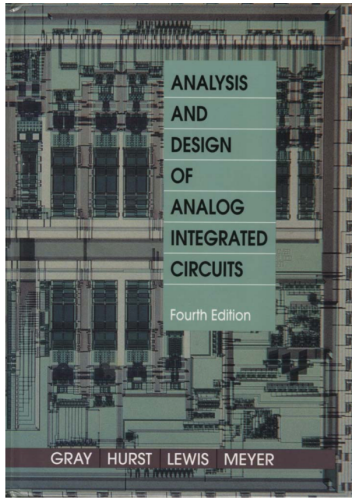
Analog IC design: Reference books, moodle

- **Design of Analog CMOS Integrated Circuits**, B. Razavi
- Analysis and Design of Analog Integrated Circuits, P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer
- Scientific papers, book chapters, …

Most figures in this set of slides are taken from the first reference

Moodle: https://go.epfl.ch/EE-320
EE-320 Analog IC design





Weekly Schedule (may be updated as needed)

Week	Subject by week – EE-320: Analog IC design – Fall 2025	Suggested Chapters
Week 1: **08/09** – 14/09	**Introduction, organization, review of MOS transistors** + Exercise1	Ch 1, Ch 2.1-2.4, Slides on Moodle
Week 2: **15/09** – 21/09	**MOS large and small-signal models, regimes of operations** + Exercise2	Ch 2.1-2.4
Week 3: **22/09** – 28/09	**Holiday – No class**	
Week 4: **29/09** – 05/10	**MOS parasitic effects, layout basic, single-stage amplifiers** + Exercise3	Ch 2.1-2.4, Ch 3.1
Week 5: **06/10** – 12/10	**Single-stage amplifiers** + Exercise4	Ch 3.1-3.7
Week 6: **13/10** – 19/10	**Single-stage amplifiers** + Exercise5	Ch 3.1-3.7
Week 7: **20/10** – 26/10	**Break – No class**	
Week 8: **27/10** – 02/11	**Single-stage amplifiers + Cascode** + Exercise6 + **Homework1**	Ch 3.1-3.7
Week 9: **03/11** – 09/11	**Differential amplifiers** + Exercise7	Ch 4.1-4.4
Week 10: **10/11** – 16/11	**TP1** Practical exercise session on Cadence	Tutorial on Moodle
Week 11: **17/11** – 23/11	**TP2** Practical exercise session on Cadence	Tutorial on Moodle
Week 12: **24/11** – 30/12	**TP3** Practical exercise session on Cadence + **Homework2**	Tutorial on Moodle
Week 13: **01/12** – 07/12	**TP4** Practical exercise session on Cadence	Tutorial on Moodle
Week 14: **08/12** – 14/12	**Differential amplifiers, current mirrors** + Exercise8	Ch 4.1-4.4, Ch 5.1-5.3
Week 15: **15/12** – 22/12	**Current mirrors** + Exercise9	Ch 5.1-5.3

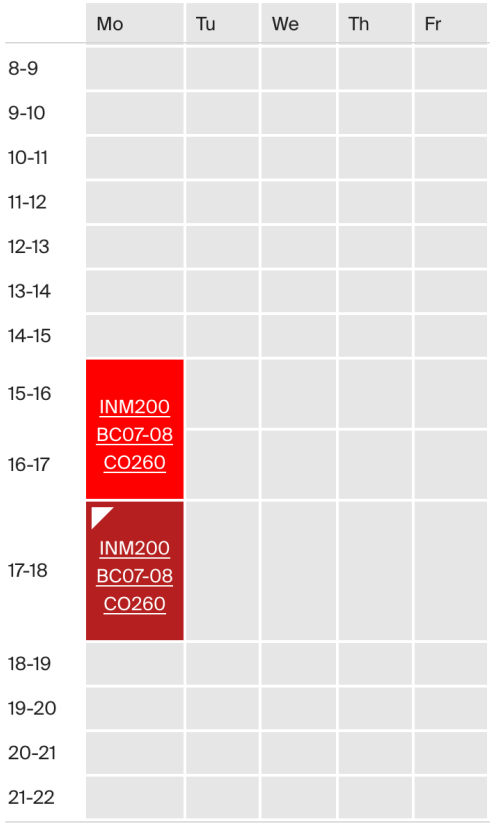
Assessment:

- **Written final exam**: 70% of the final grade
- **Homework (2 in total)**: 30% of the final grade

Course structure

- In-person lectures: 2 hours per week in **INM200**
- On-campus exercises: 1 hour per week in **INM200**
- Four TP (Cadence) sessions: 3 hours in BC07/08

- Questions through moodle forum
- On-demand office hours (Professor and TAs)
  - Alin Thomas Tharakan (alin.tharakan@epfl.ch)
  - **Alireza Mafi (alireza.mafi@epfl.ch)**
  - Cong Huang (cong.huang@epfl.ch)
  - **Jieun Joo (jieun.joo@epfl.ch)**
  - **Alexandre Domenech (alexandre.domenech@epfl.c**
  - Yiheng Fu (yiheng.fu@epfl.ch)

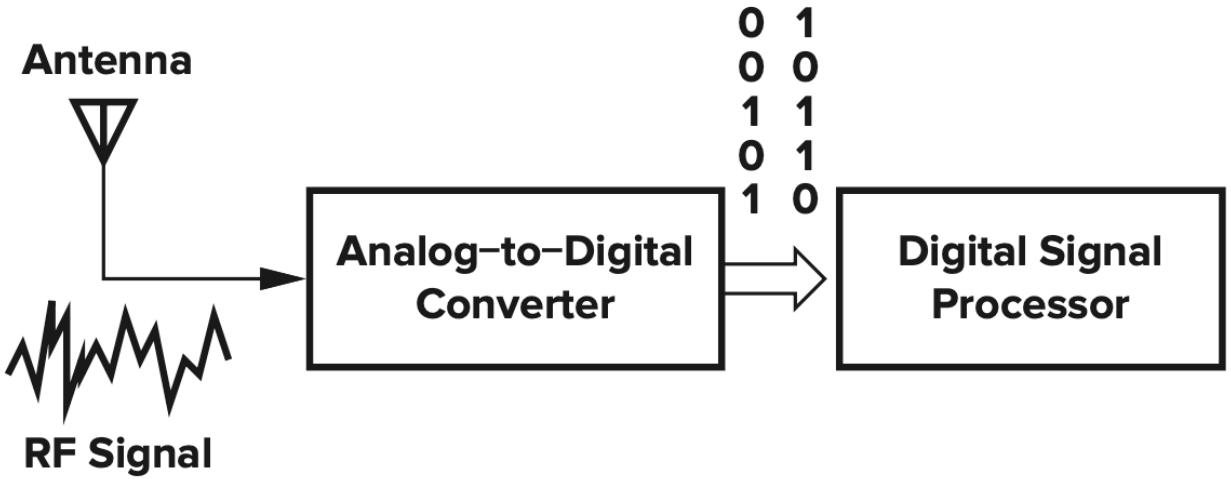


Make sure to

- attend the lecture and exercise sessions, take notes
- invest time on exercises and homeworks

Analog Circuit Design

- The sensing interface demands analog design experts



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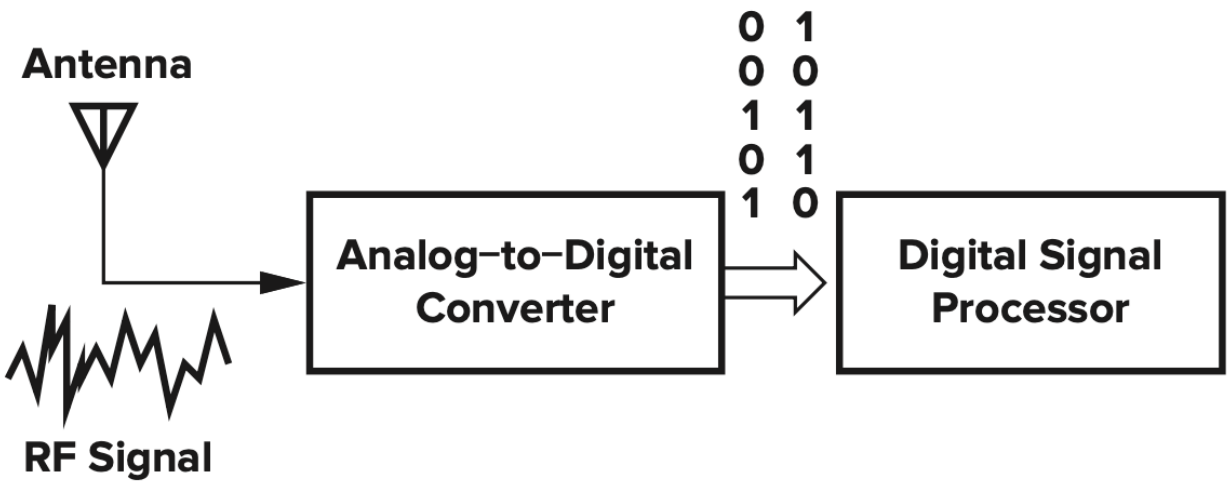
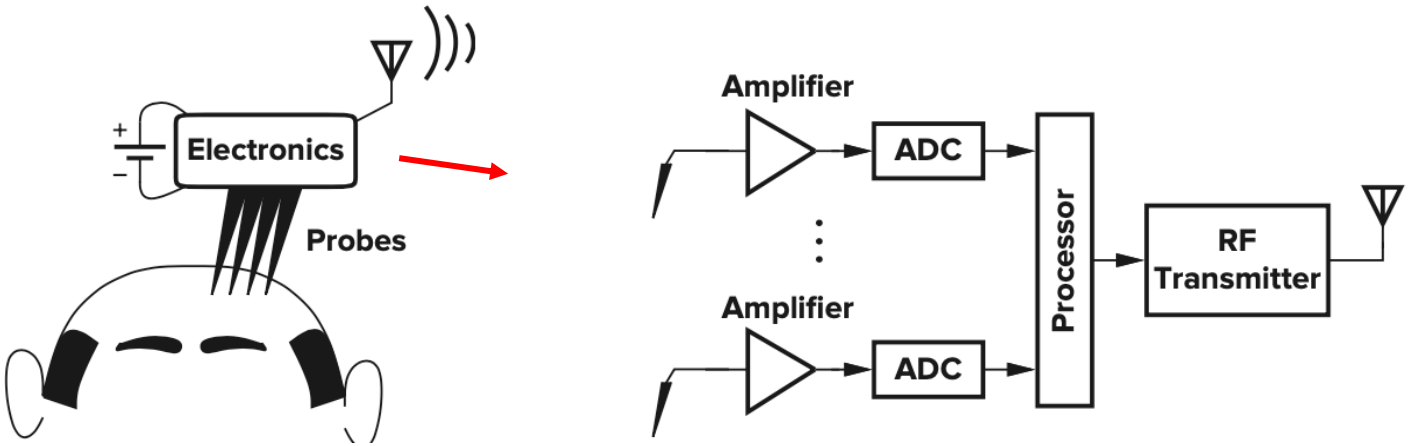
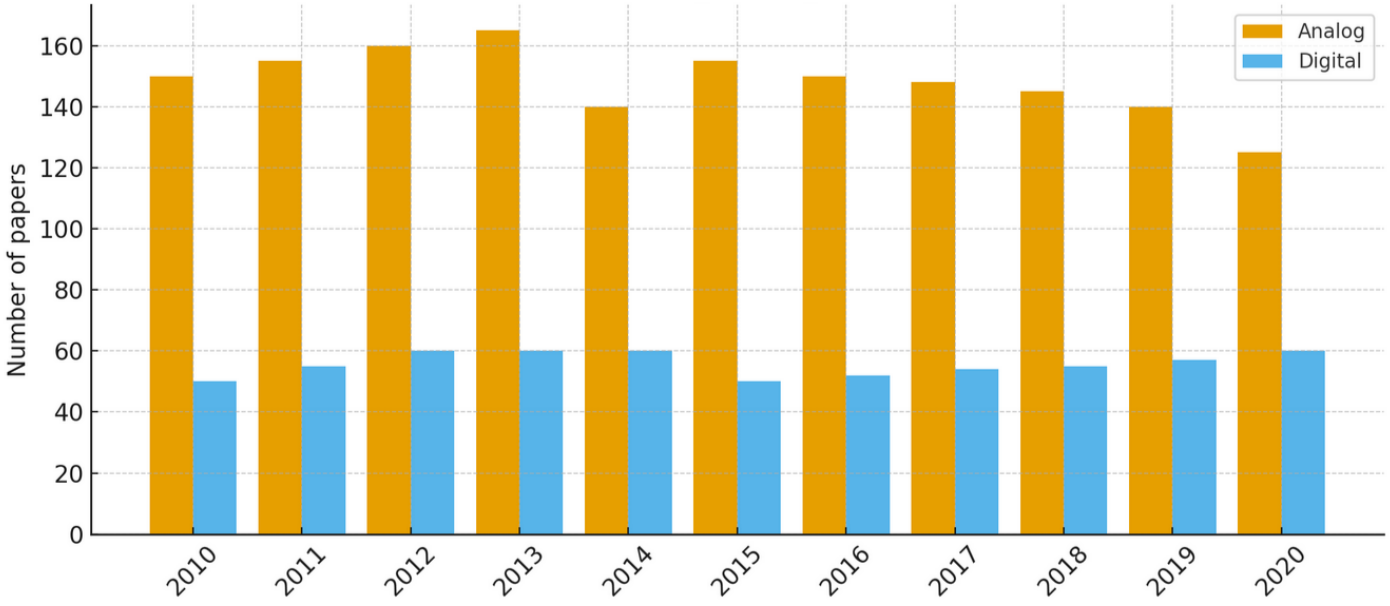




Analog Design in High Demand

- **Analog circuits typically less complex than digital circuits**
  - An amplifier or ADC contain several 100s to 1000 transistors, a microprocessor has **billions** or even more!

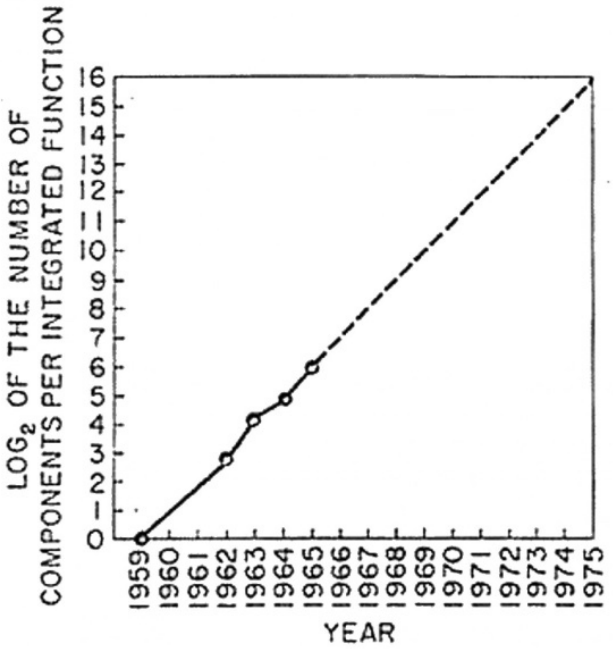
- Still a large contribution of papers in top circuit conferences involve analog design concepts



IEEE International Solid-State Circuits Conference (ISSCC)

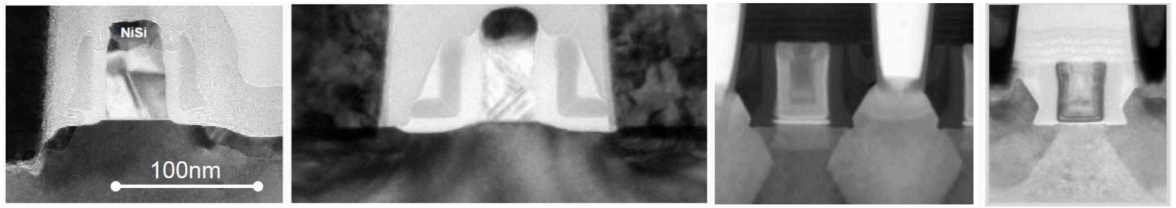
Technology Scaling

- **Gordon Moore,1975**: the MOS device dimensions scale down by a factor of 2 every 3 years, **the number of transistors per chip would double every 1 to 2 years >>** tremendous improvement in the **speed** of integrated circuits



- **Challenges for IC designers**
  - Low supply voltage
  - Leakage
  - PVT variations
  - …

90 nm node **65 nm node** **45 nm node** **32 nm node**



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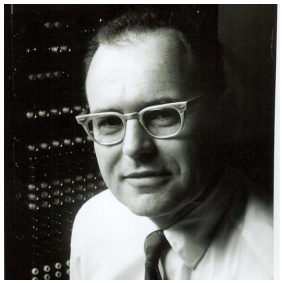
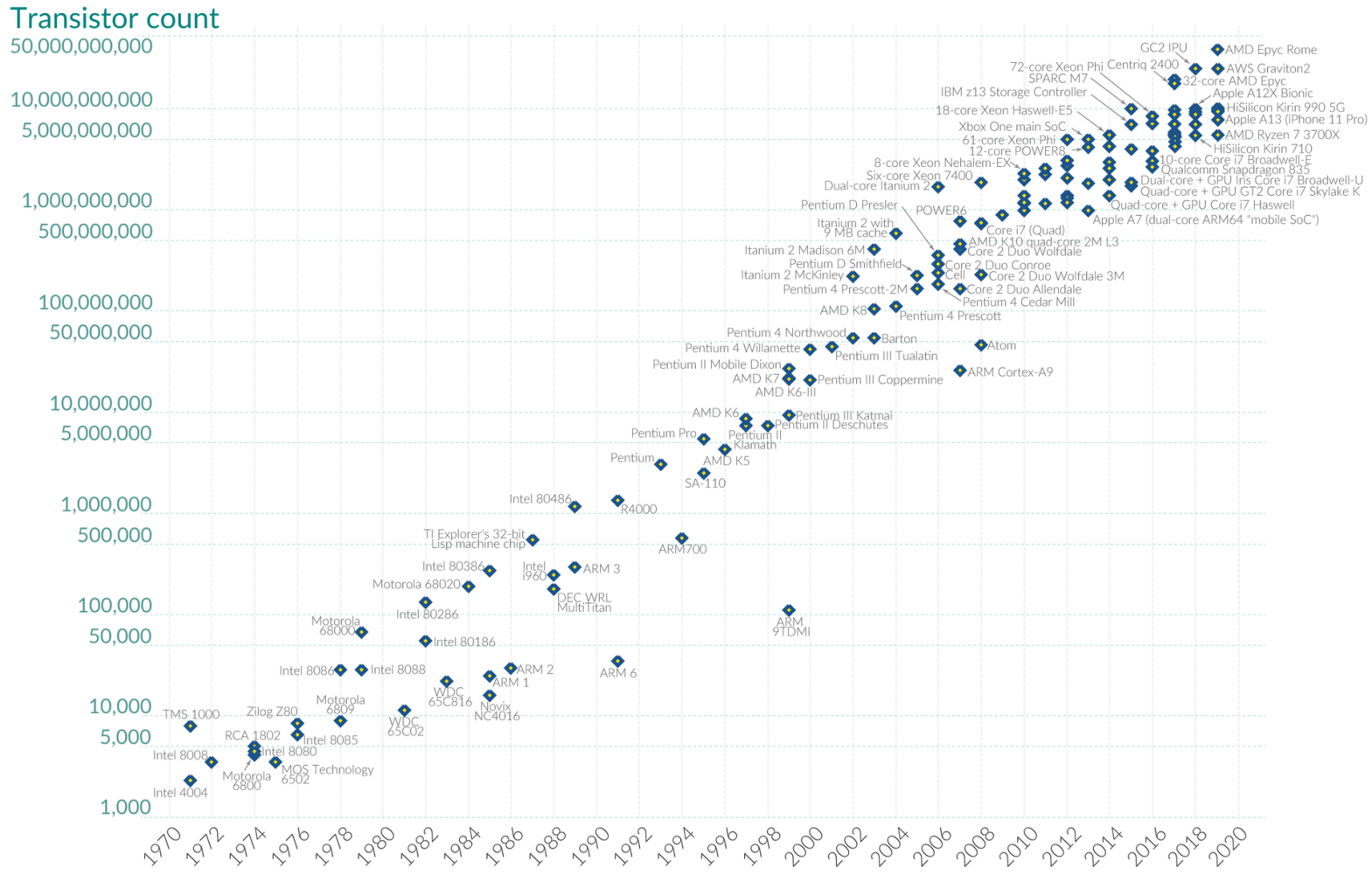


courtesy V. Moroz, IEDM

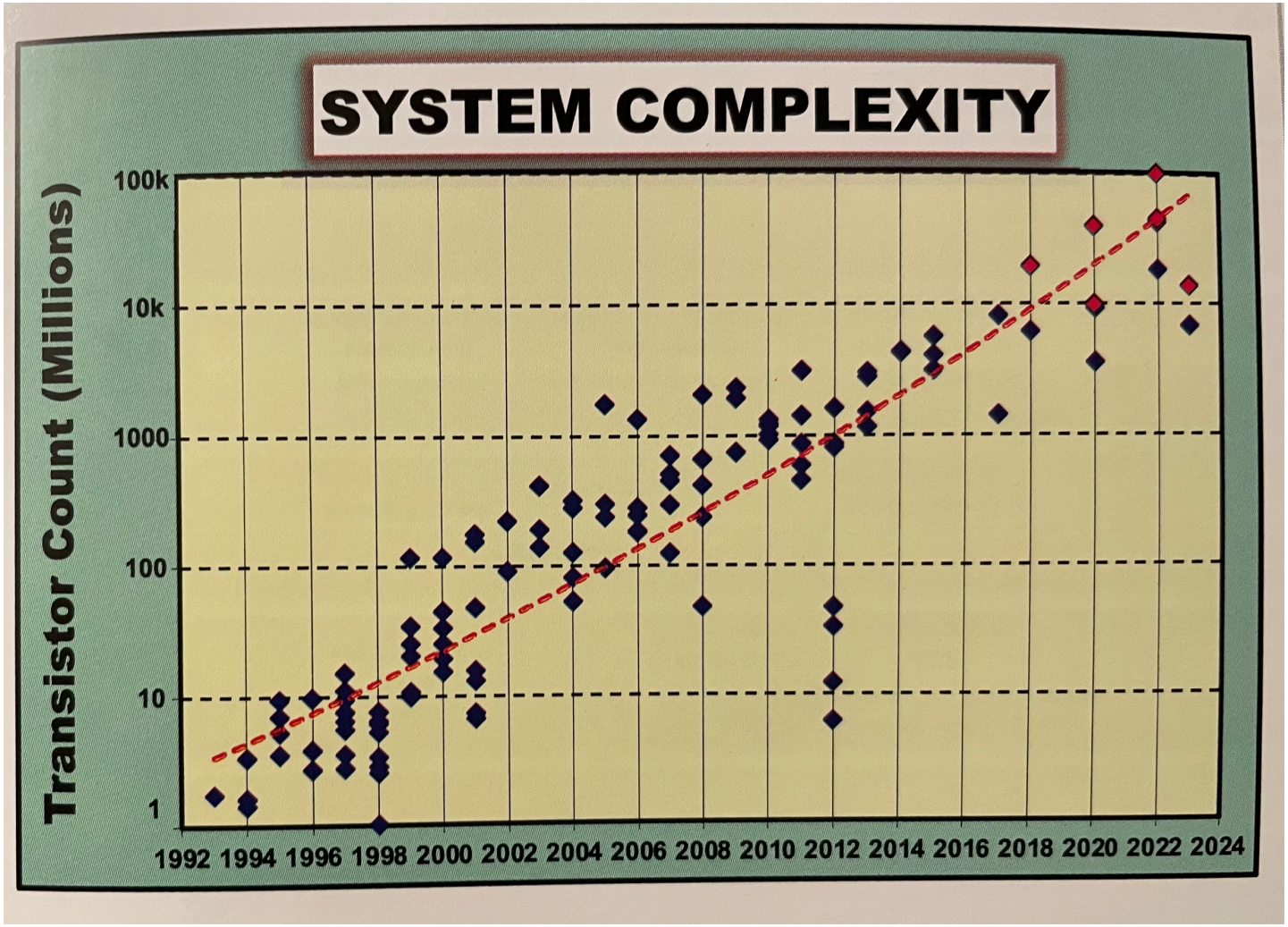
Moor's Law

- **Microprocessor Transistor Counts 1970-2020 and Moore's Law**

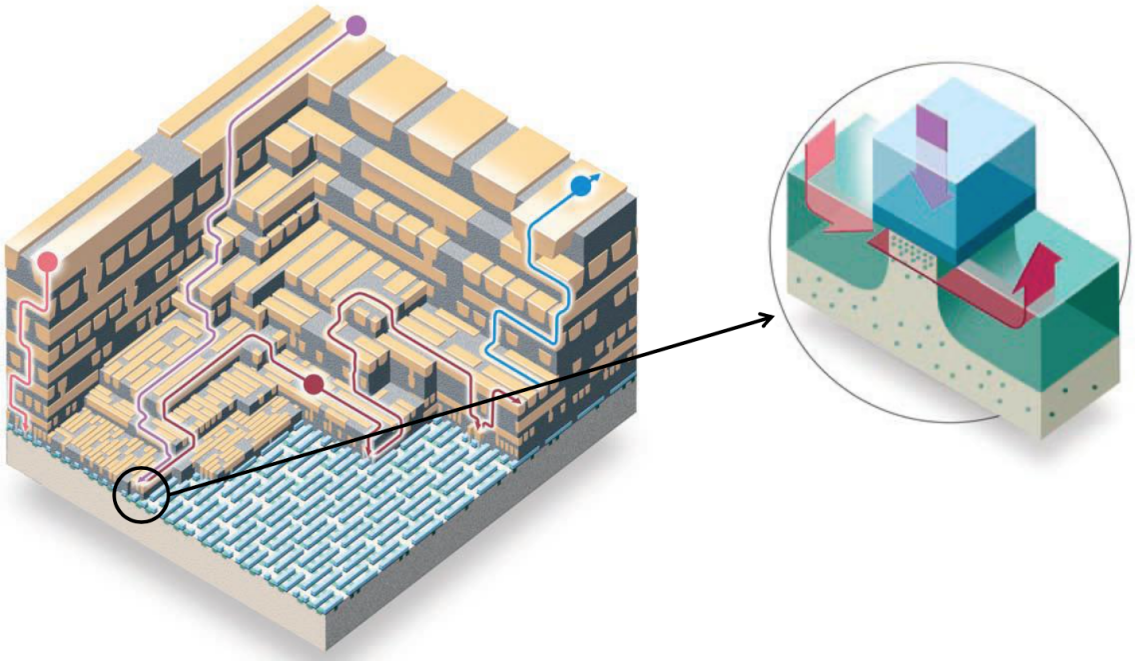


System Complexity

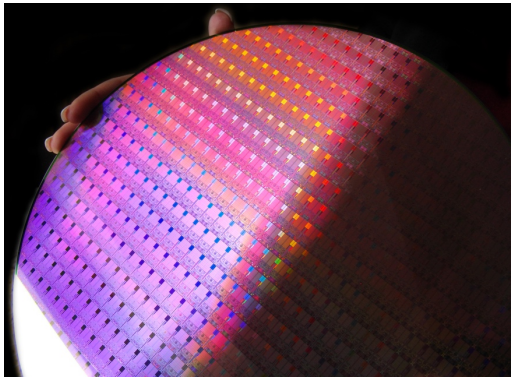
- **Chip-complexity scaling trends (ISSCC 2023)**



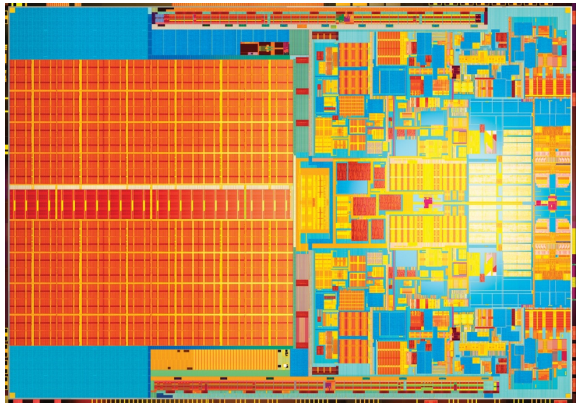
Intel's 45nm Process



45nm process wafer



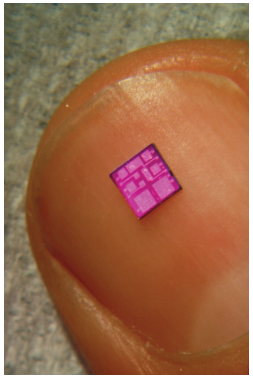
Dual-core processor die



https://www.intel.com/pressroom/kits/45nm/photos.htm

Why Integrated?

- Placing multiple devices **on the same substrate**: late 1950s
- From **simple chips with a handful of components** to flash drives and microprocessors with **several billion devices**
- **Integrated circuit (IC)** enable **complexity, speed, and precision** that is **impossible** to achieve with **discrete** implementations



https://www.pinterest.ch/pin/431360470545933628/
https://www.britannica.com/technology/integrated-circuit

Why CMOS?

- Metal-oxide-semiconductor field-effect transistors (**MOSFETs**) by J. E. Lilienfeld in **early 1930s**—well before the invention of bipolar transistor

- **Mid-1960s**: complementary MOS (**CMOS**) devices (both n-type and p-type transistors), led to a revolution in the semiconductor industry

J. E. Lilienfeld

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- CMOS gates dissipated power **only during switching**, as opposed to bipolar counterparts
- The dimensions of MOS devices could be **scaled down** more easily than those of other types of transistors

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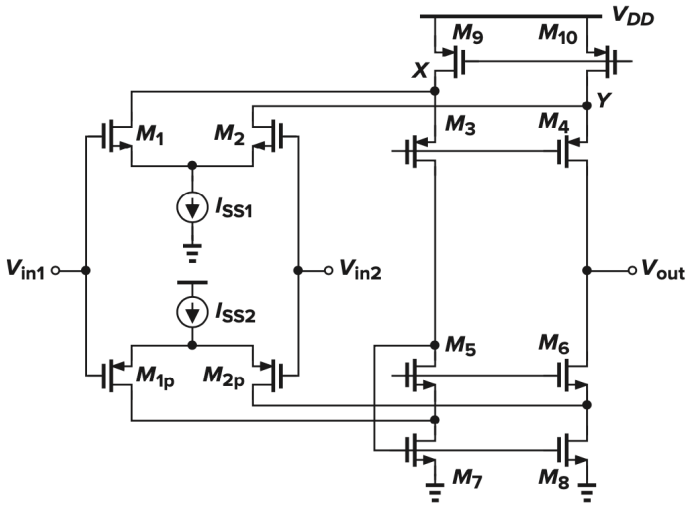
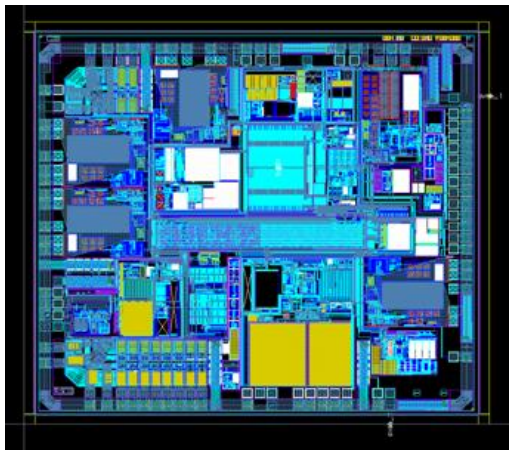
- CMOS gates dissipated power **only during switching**, as opposed to bipolar counterparts
- The dimensions of MOS devices could be **scaled down** more easily than those of other types of transistors
- The **low cost of fabrication** and the possibility of placing both analog and digital circuits on the same chip
- Principal force: **device scaling**
  - Lower **supply voltage**, lower **power**

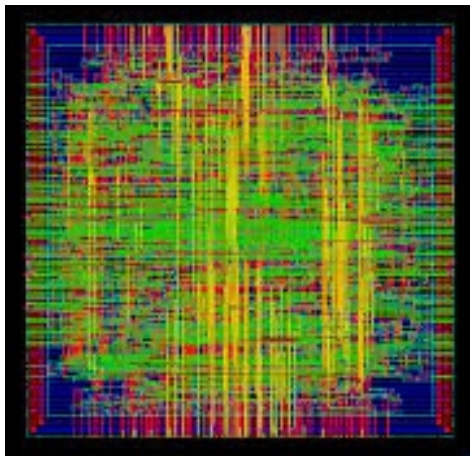
Good Analog Design is an Art!

- Good analog design requires intuition, rigor, and creativity

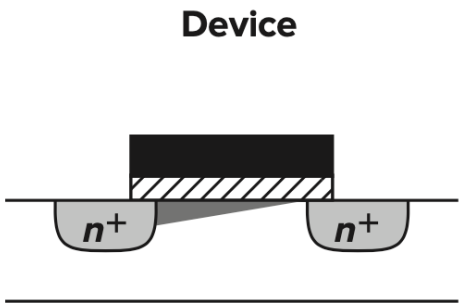
- As analog designers, we must
  - Have intuitive understanding of a large circuit
  - Be able to quantify important effects in a circuit
  - **Invent new circuit topologies**

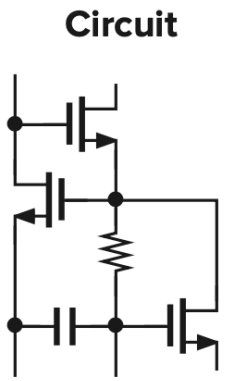


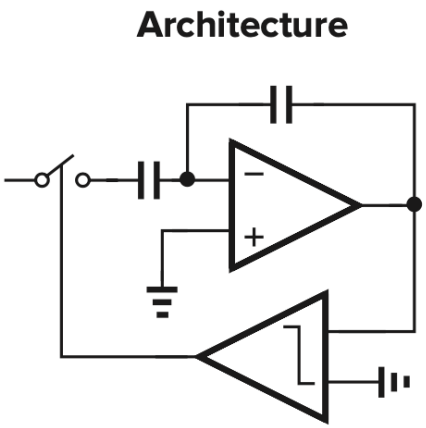


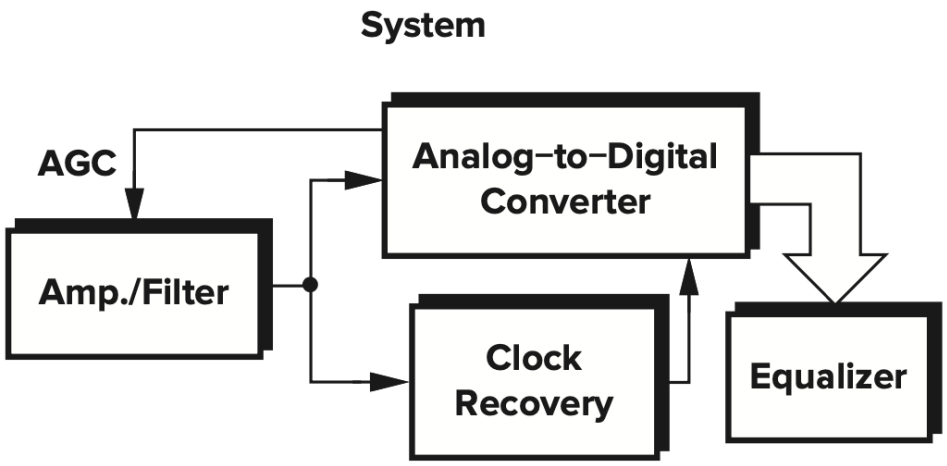


IC Design: Device, Circuit, Architecture, System

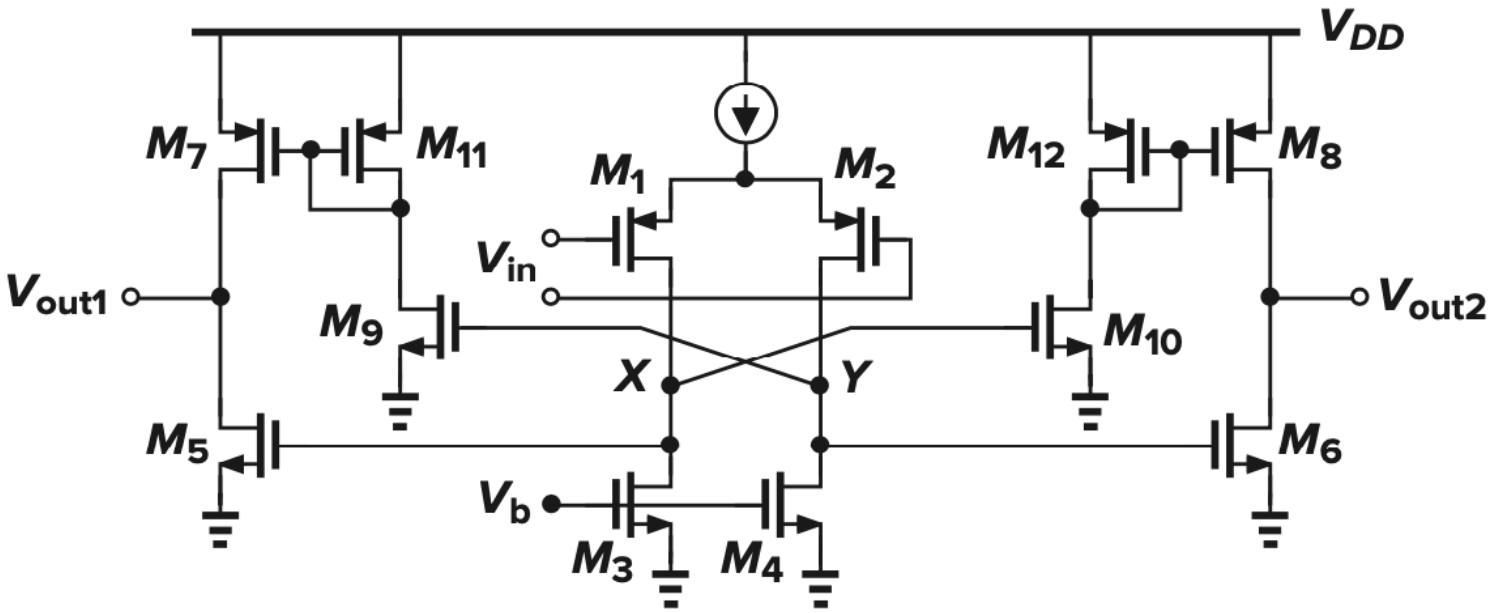




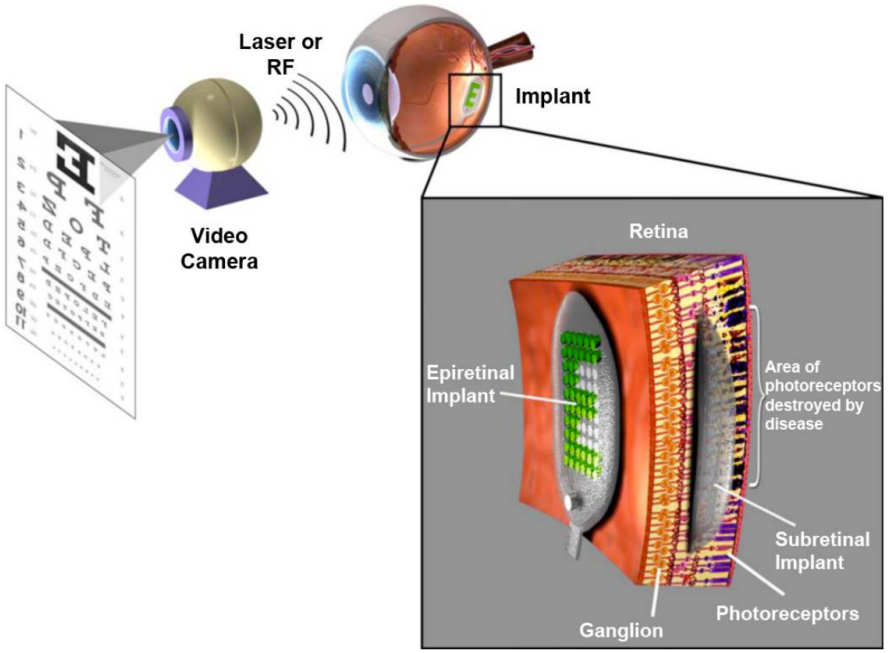


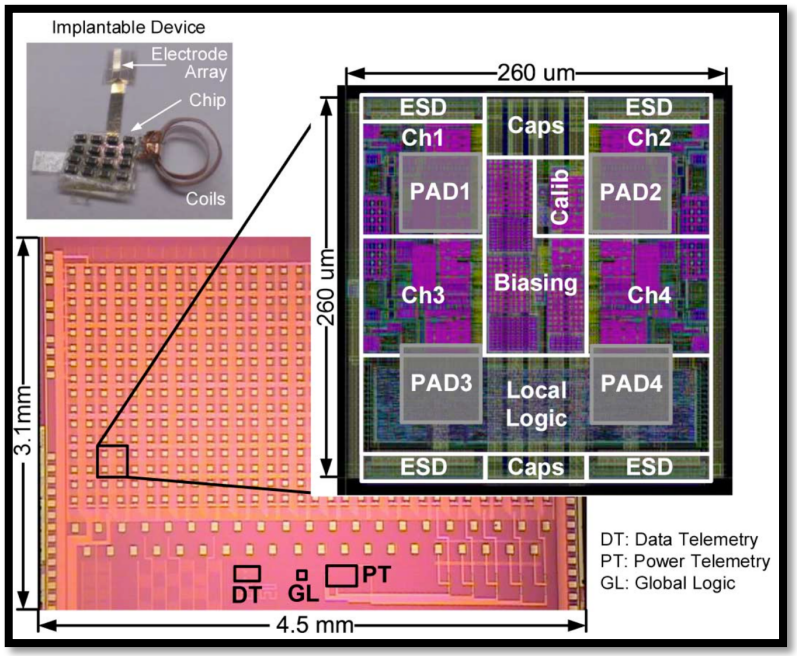


To understand Complex CMOS Circuits



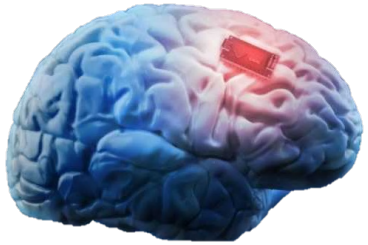
Biomedical Systems-on-chip (SoCs)

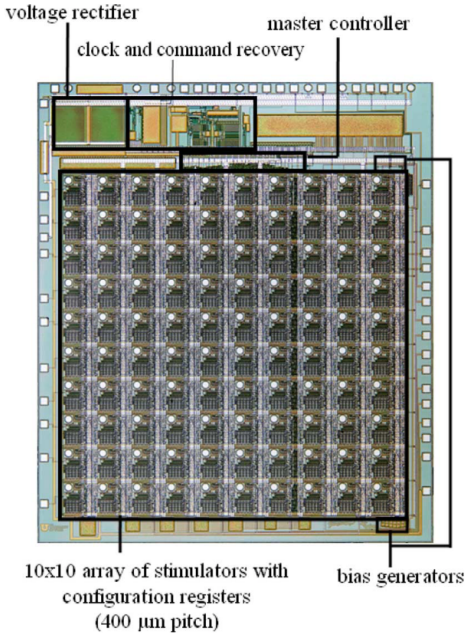




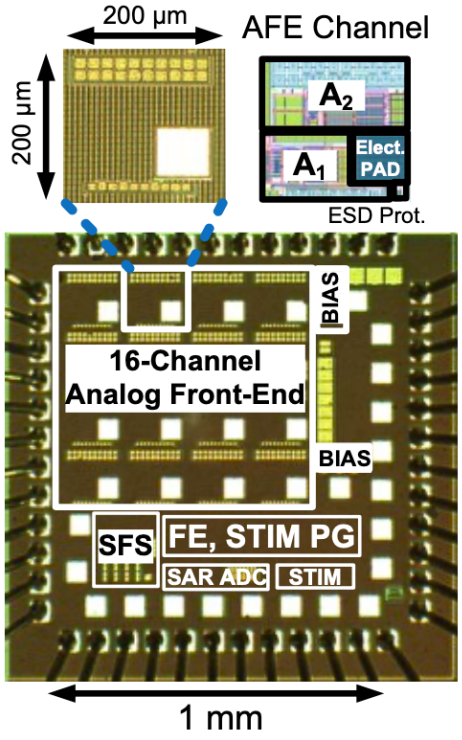
An Epiretinal prosthesis
M. Monge et al., IEEE TBioCAS 2013

Neural Interfaces

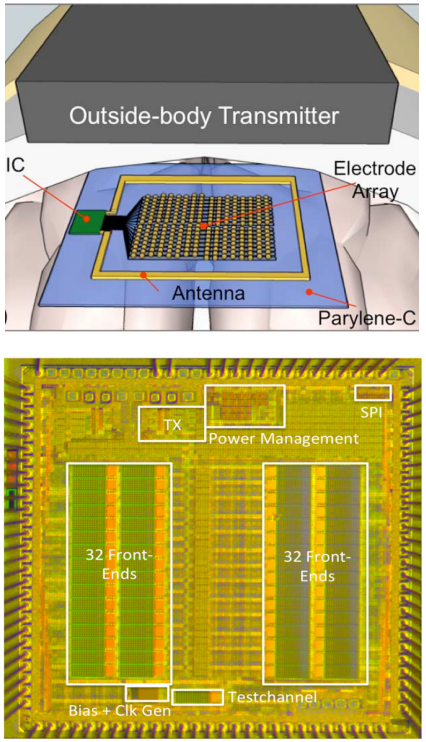




A neurostimulator chip
R. Harrison et al., TBioCAS 2009

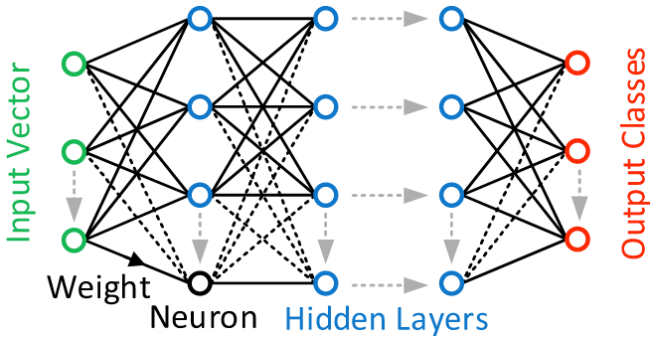


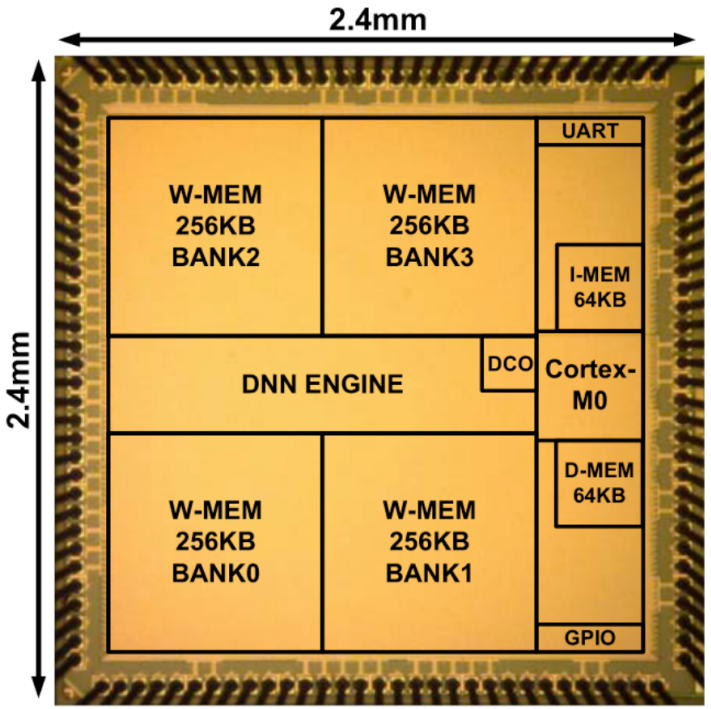
A seizure control chip
M. Shoaran et al., VLSI Symp 2016



A neural recording chip
R. Muller et al., JSSC 2015

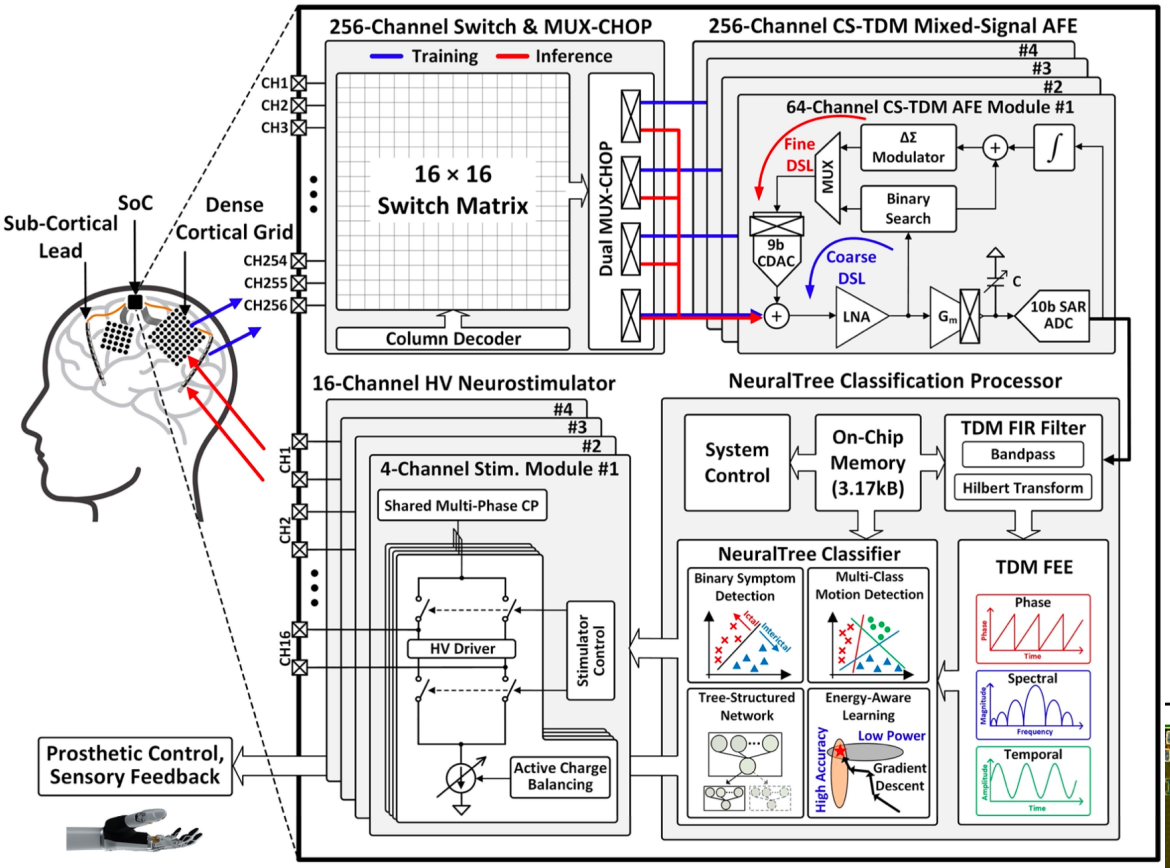
Machine Learning SoCs



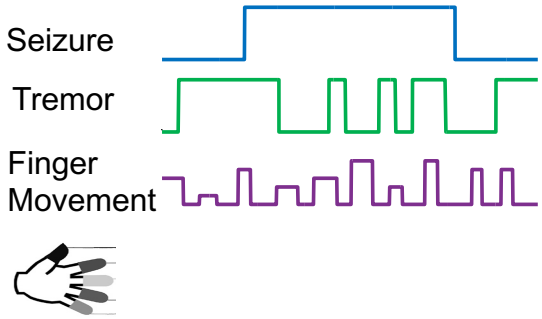


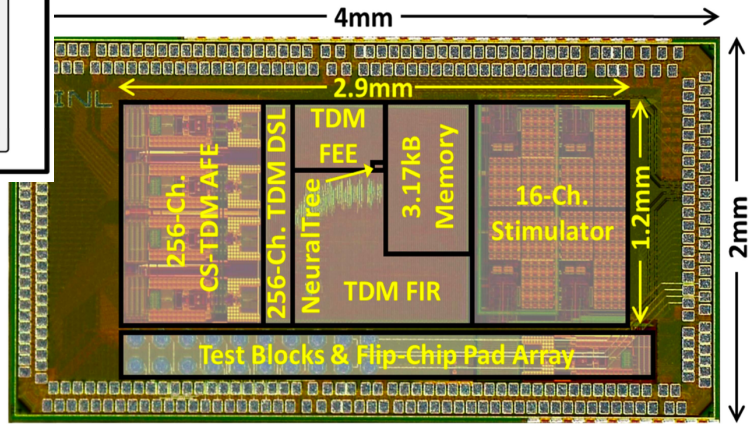
A DNN accelerator
P. N. Whatmough et al., JSSC 2018

Closed-loop Neuromodulation with On-Chip ML



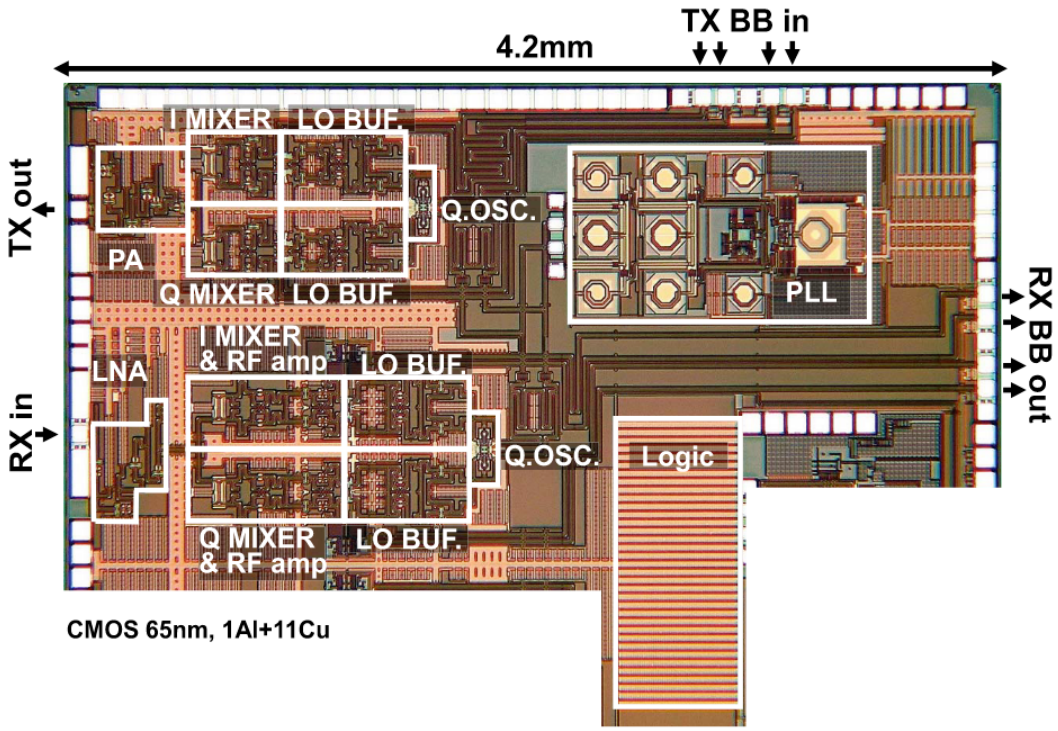
Classifier/decoder Output





A closed-loop stimulation chip
U. Shin et al., ISSCC'22, JSSC'22

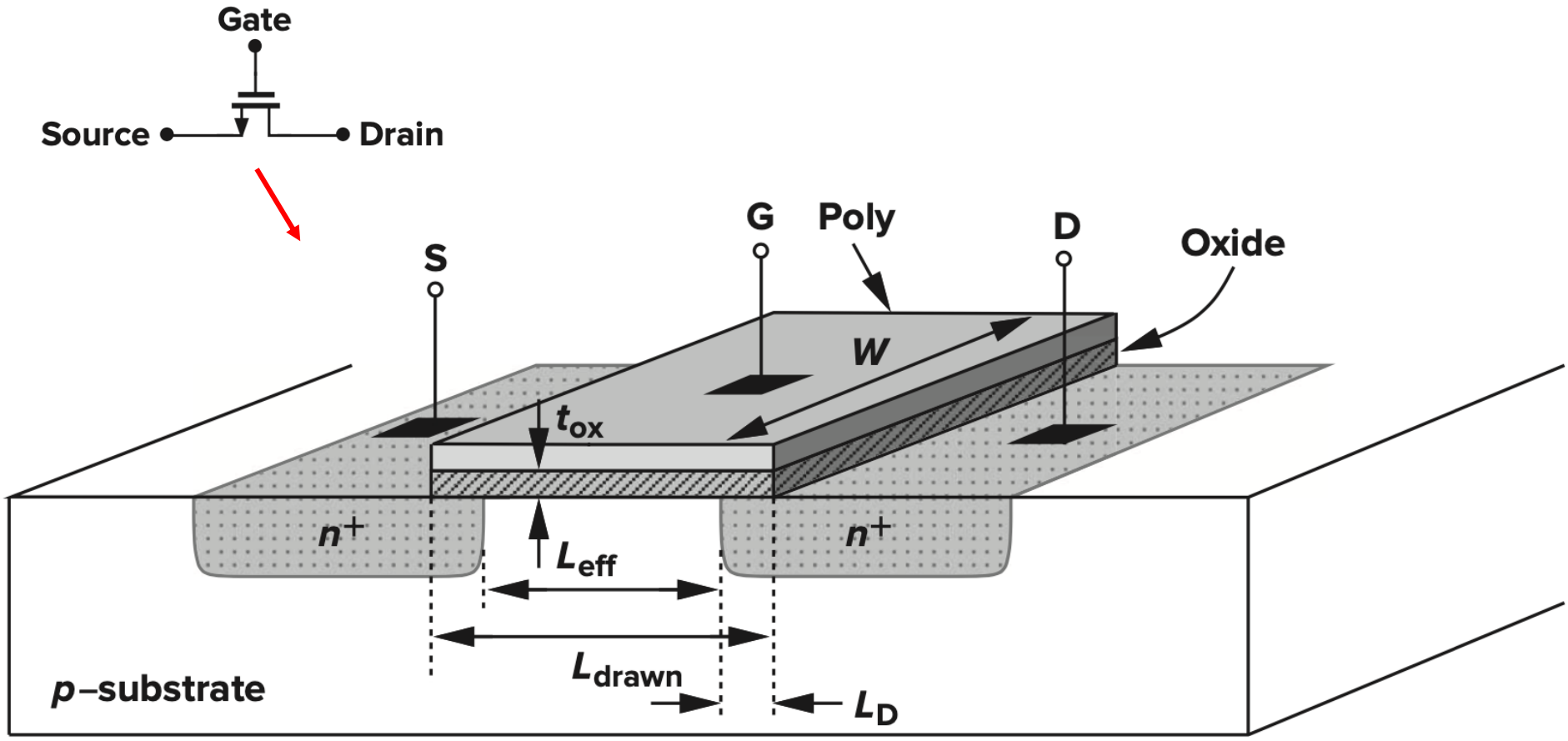
High-frequency Transceivers



A 60-GHz transmitter
R. Wu et al., JSSC 2017

MOS: Basic Device Physics

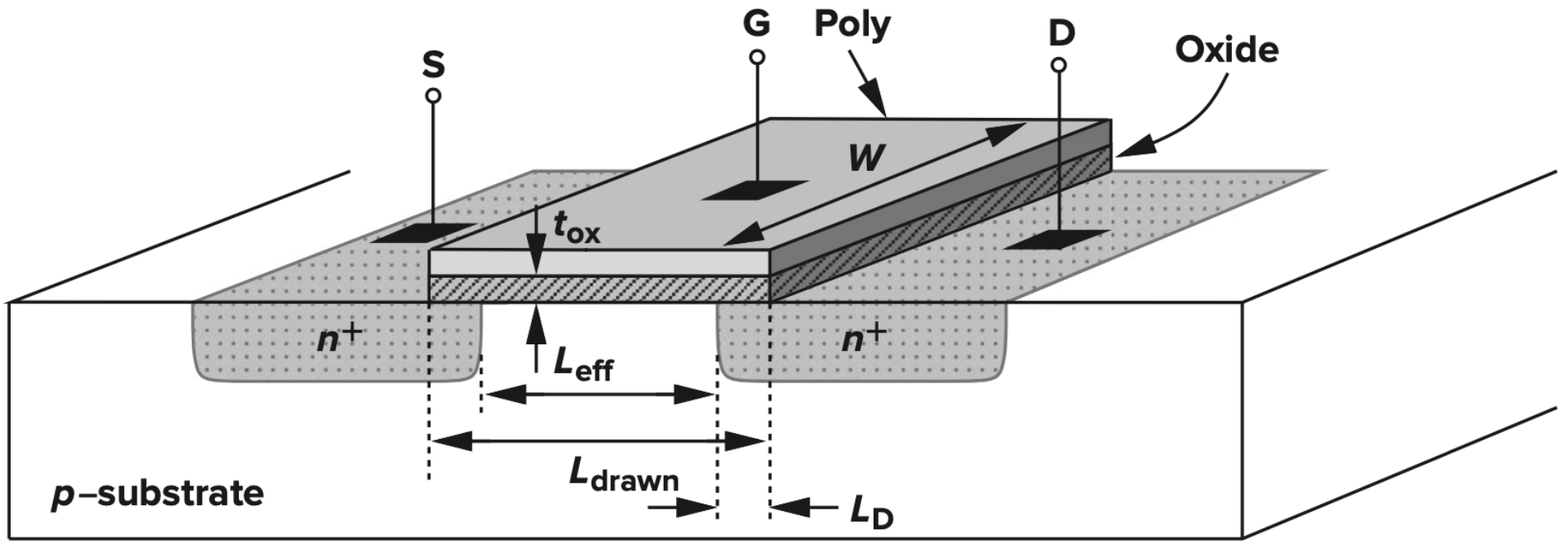
- An n-type MOS (**NMOS**) device on a **p-type substrate**
  - a heavily-doped polysilicon **(conductor)** operating as the **gate**
  - a thin layer of silicon dioxide (SiO_2) **insulating** the gate from the substrate
  - two heavily-doped **n regions**: **source** and **drain** terminals



MOS: Basic Device Physics

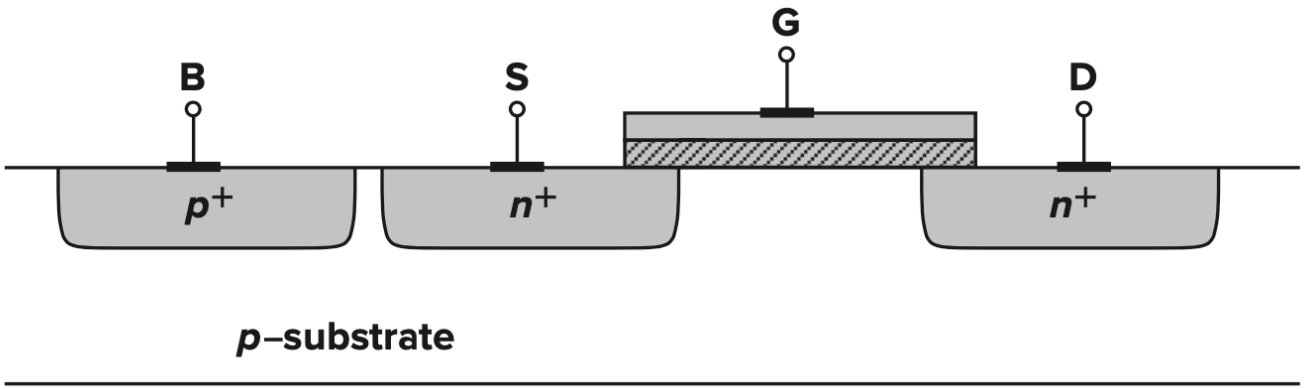
- The MOS structure is **symmetric** with respect to S and D
  - The source terminal provides charge carriers (electrons in NMOS) and the drain terminal collects them
  - Depending on source and drain voltage, they may exchange roles

$$L_{eff} = L_{drawn} - 2L_D$$



NMOS: Substrate connection

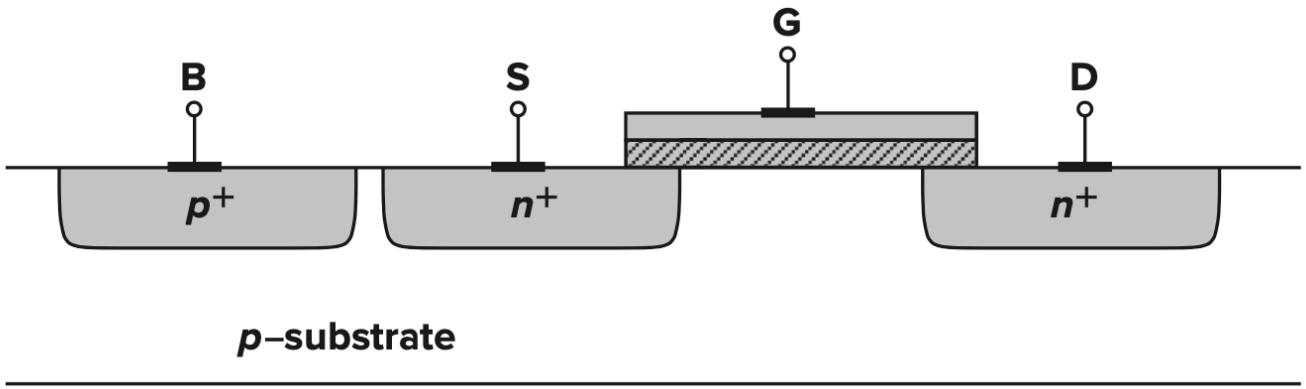
- The **substrate potential** greatly influences the device characteristics
  - So MOSFET is a **four-terminal** device



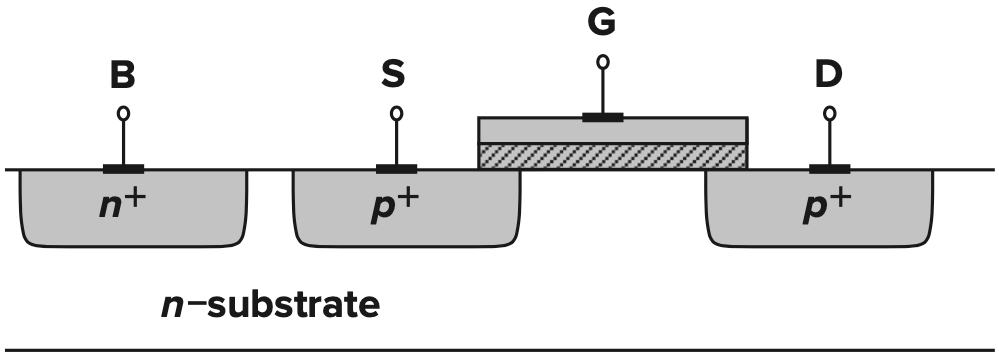
NMOS: Substrate connection

- The **substrate potential** greatly influences the device characteristics
  - So MOSFET is a **four-terminal** device

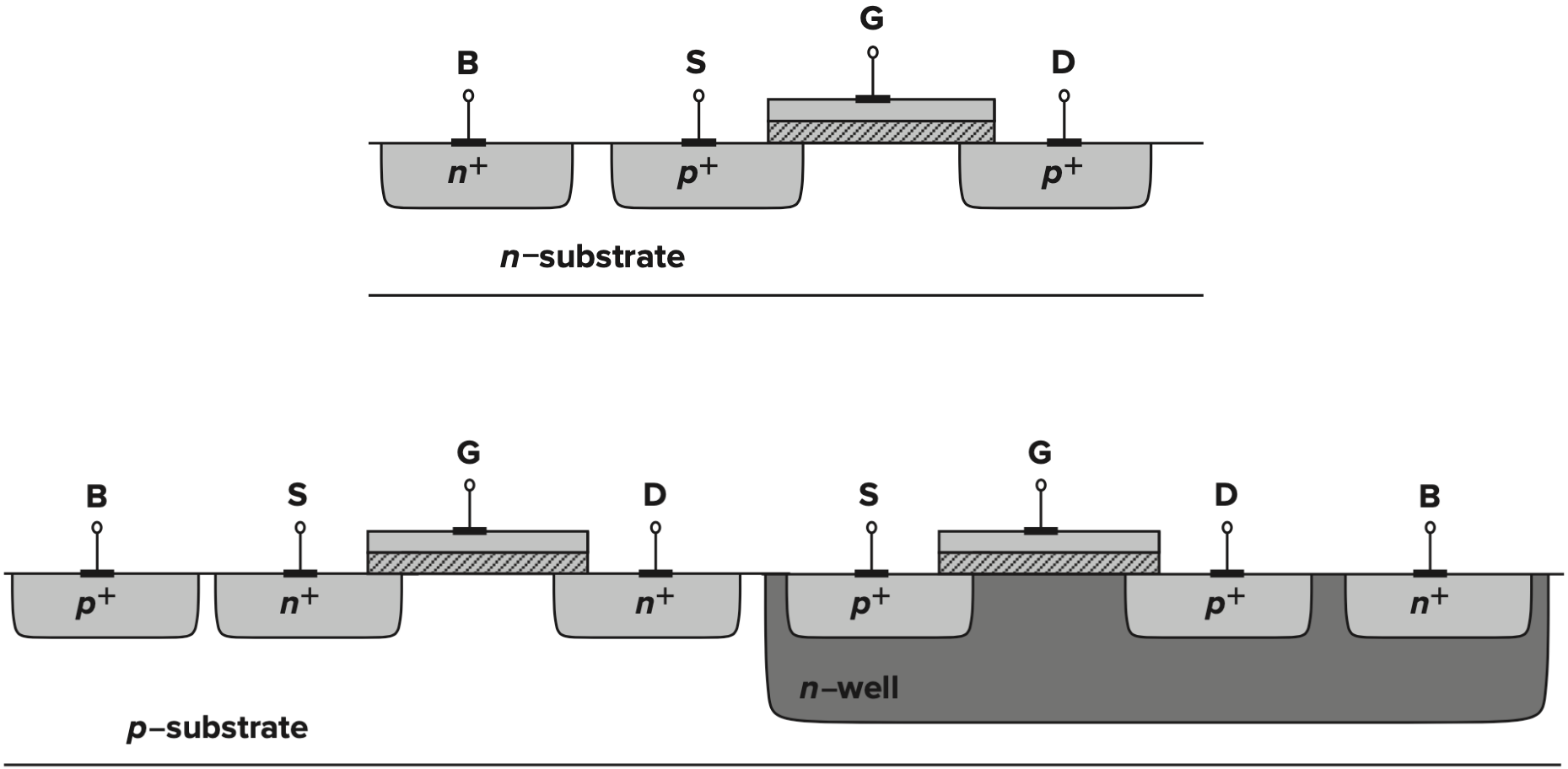
- In typical MOS operation, the **S/D junction diodes** must be **reverse-biased**
  - **Substrate of NMOS** is typically connected to the **most negative supply**
  - **Substrate of PMOS** is typically connected to the **most positive supply**



PMOS transistor



PMOS inside an n-well

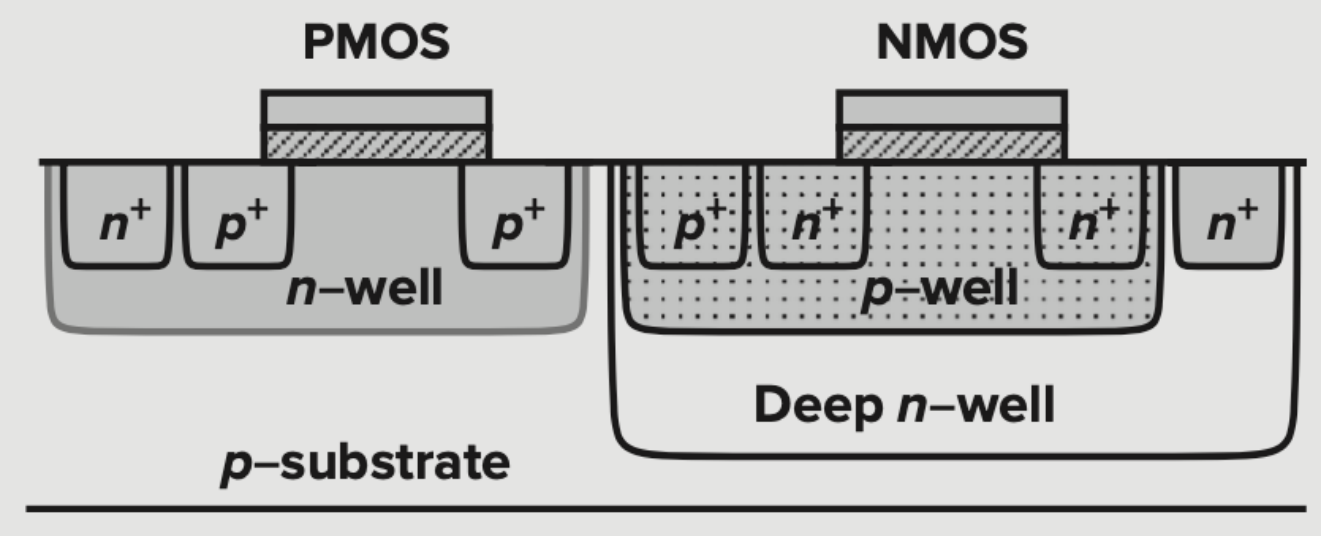


Deep n-well: NMOS with localized substrate

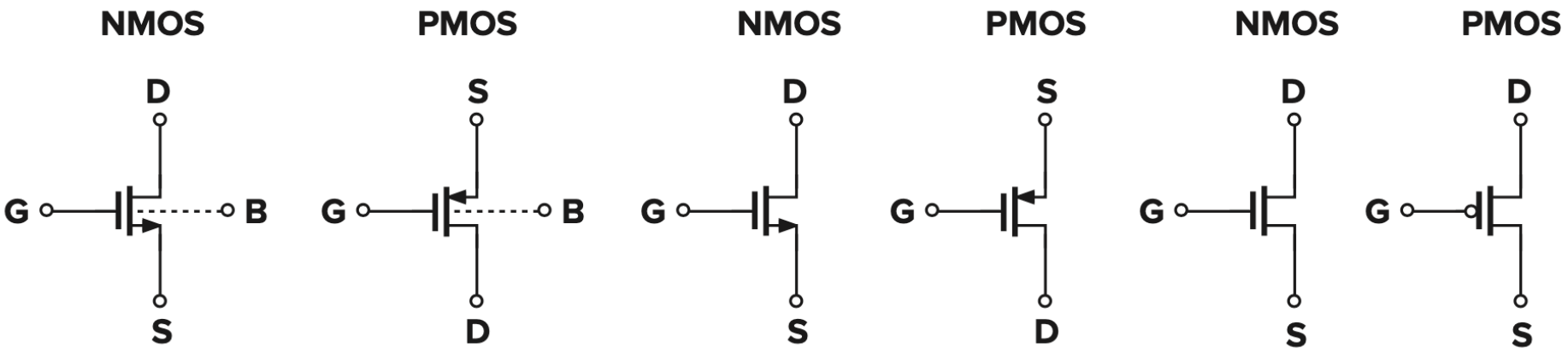
- Some modern processes offer a "**deep n-well**," an n-well that contains an **NMOS and its p-type bulk** (triple wells)

✓ The NMOS bulk **localized**, not tied to other devices

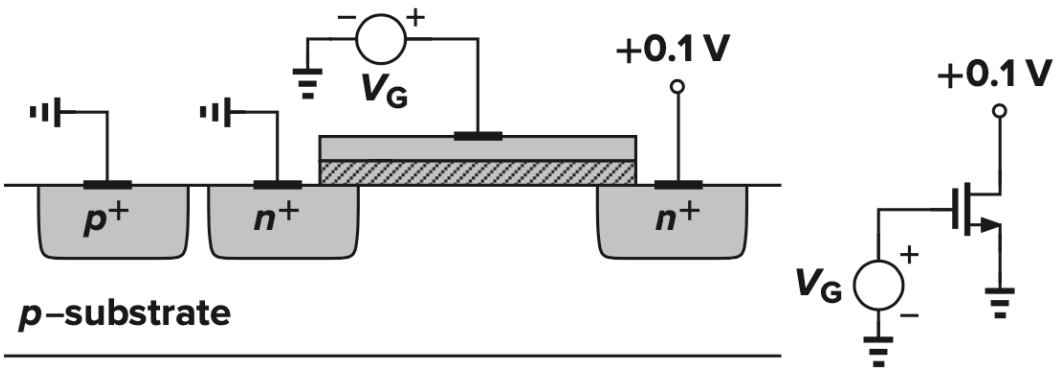
✗ Substantial **area overhead**



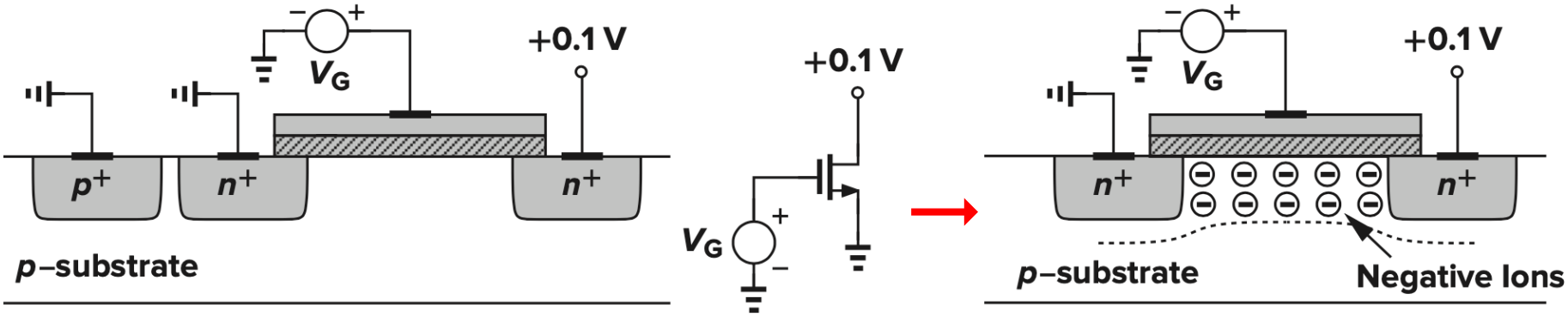
MOS Symbols



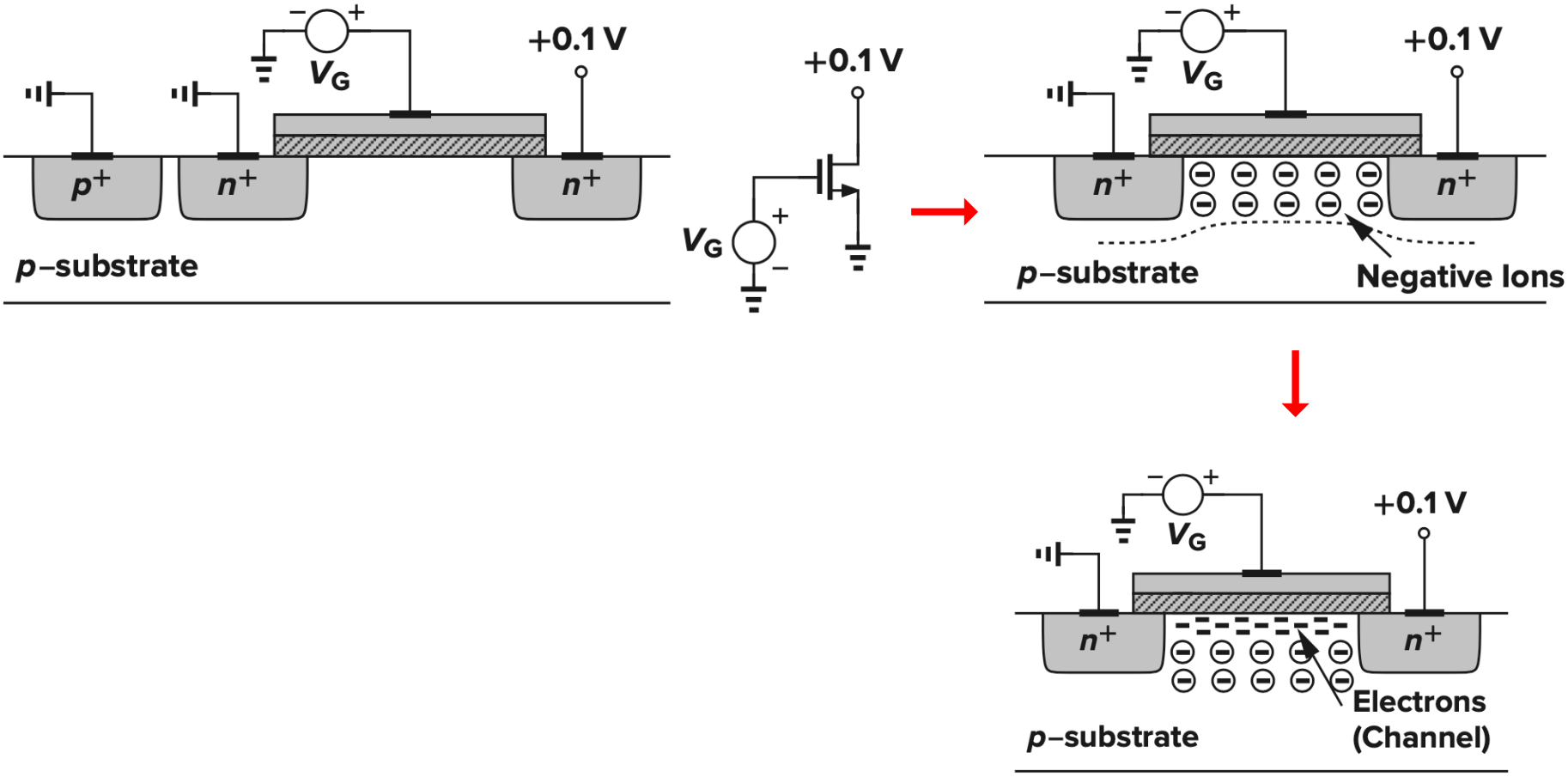
MOS driven by a gate voltage: threshold?



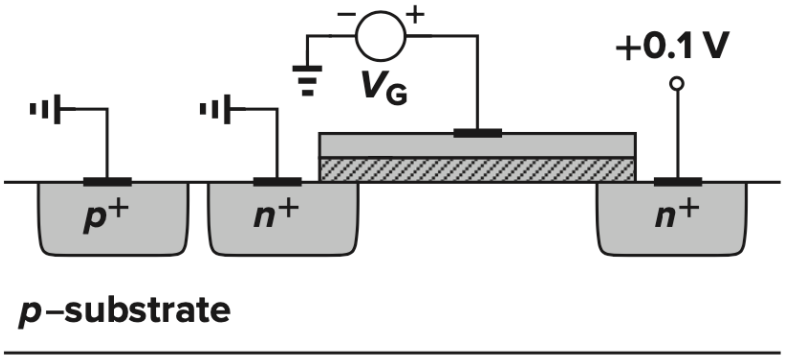
Formation of depletion region

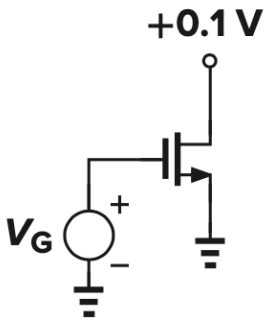


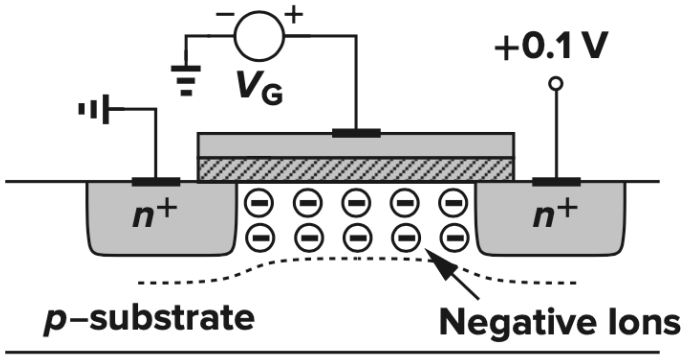
Formation of inversion layer



MOS threshold voltage



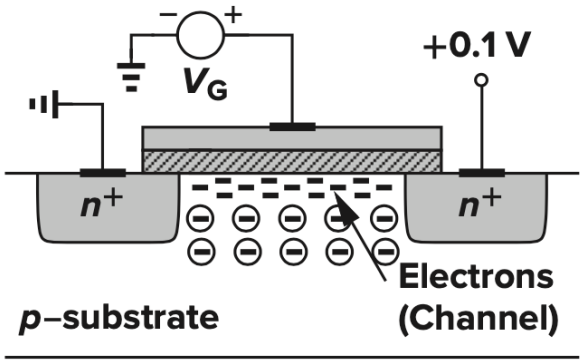




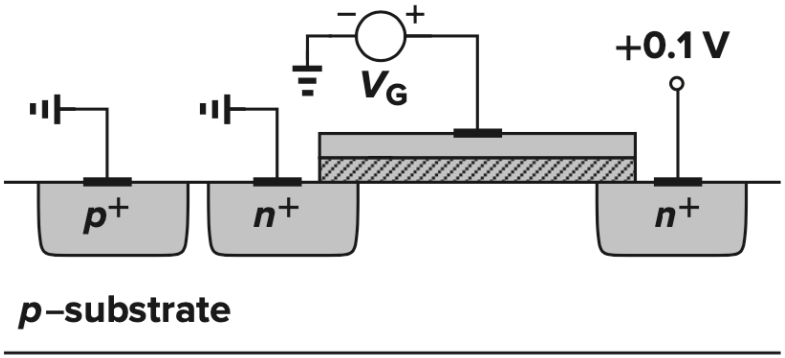
$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

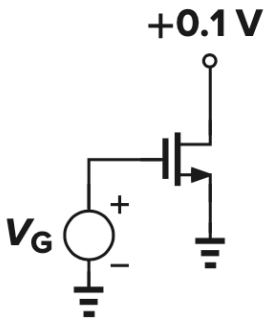
$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

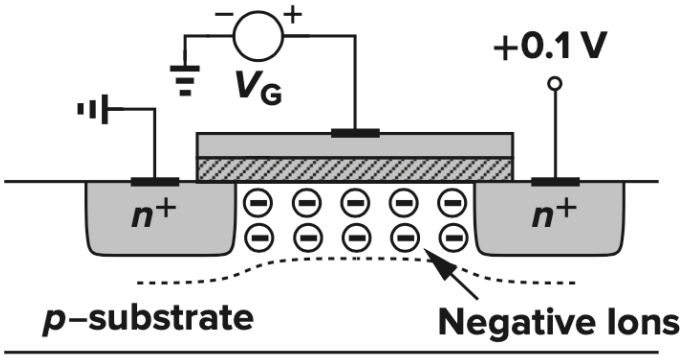
$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$



MOS threshold voltage







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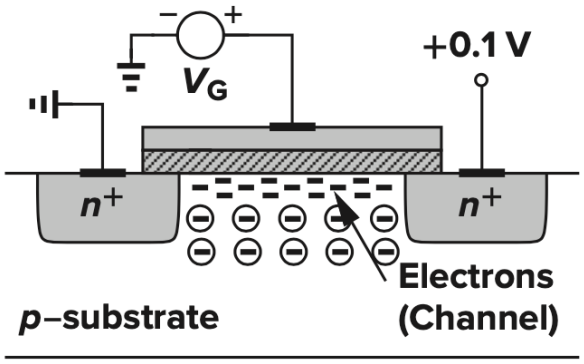


Q_{dep} : charge in the depletion region

N_{sub}: *doping density of the substrate*

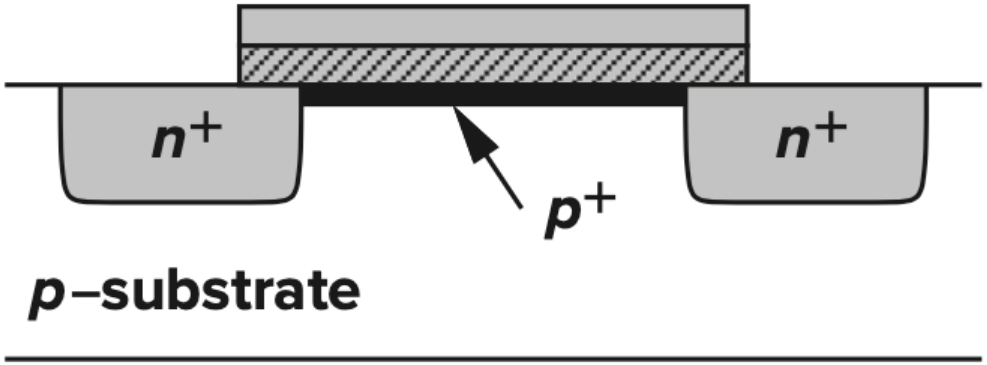
C_{ox} : the gate-oxide capacitance per unit area

n_i : density of electrons in undoped silicon

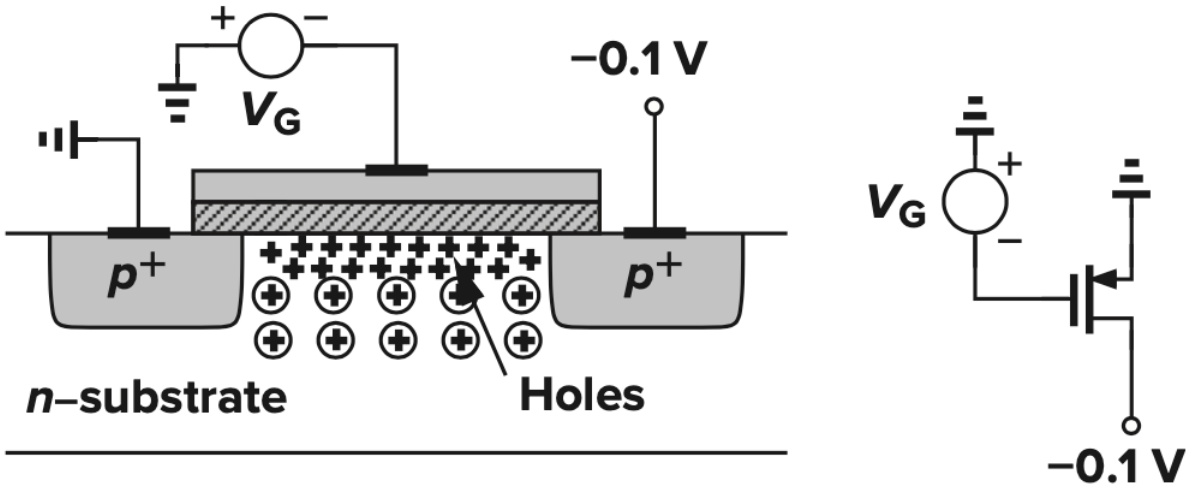
ε_{si} : the dielectric constant of silicon

Φ_{MS} : the difference between the work functions of the poly (gate) and substrate

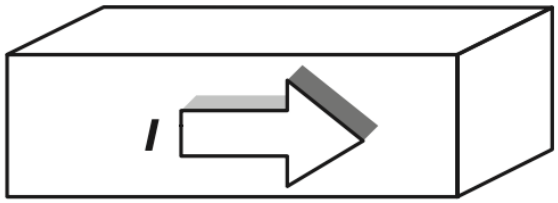
Dopant implantation to alter the threshold



Inversion layer in PMOS



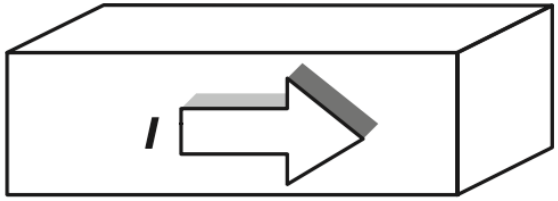
Derivation of I/V Characteristics



$$I = Q_d \cdot v$$

- Q_d is the **mobile charge density** along the direction of current (coulombs/meter)
- And **v** is the velocity of the charge (meters/second)

Derivation of I/V Characteristics



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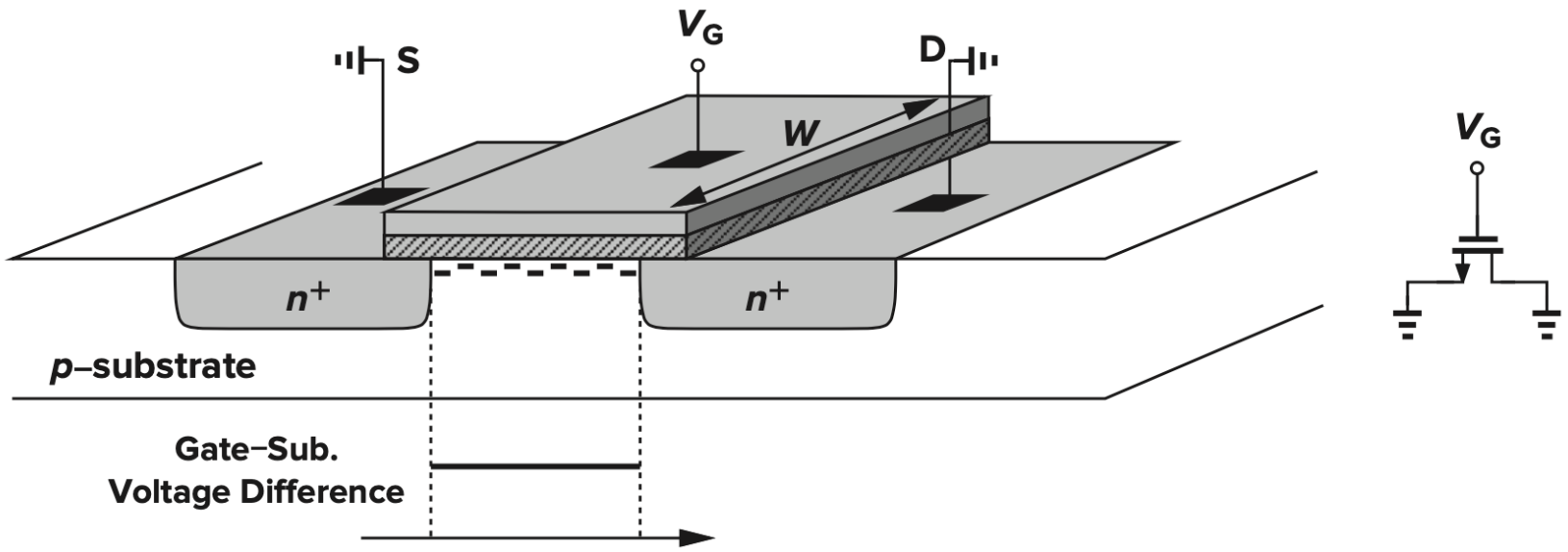
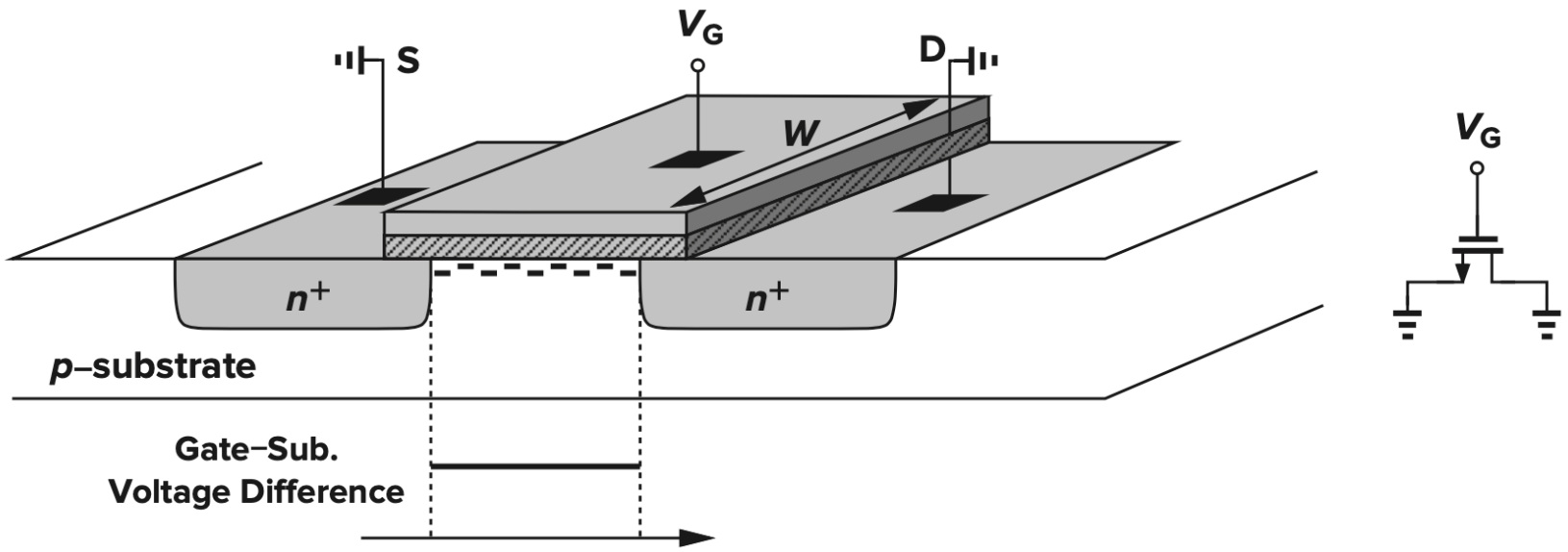


Derivation of I/V Characteristics

- Charge density in the inversion layer (**charge per unit length** along the S-D path):

$$Q_d = WC_{ox}(V_{GS} - V_{TH})$$

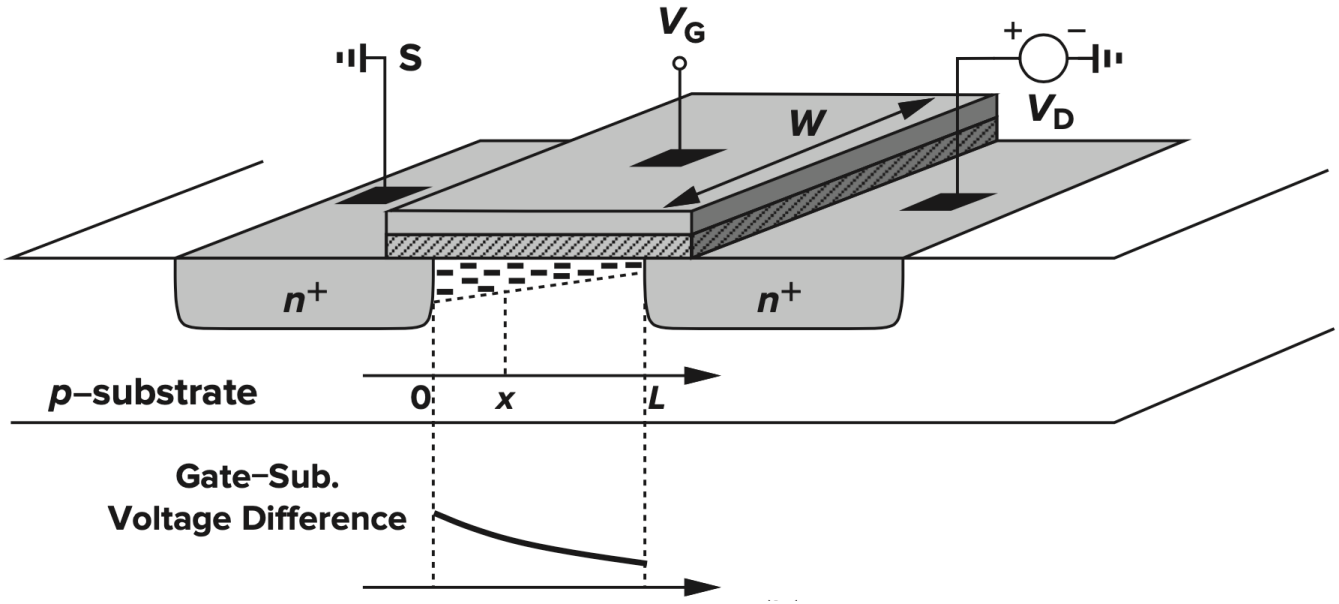


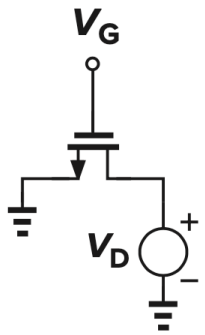
Derivation of I/V Characteristics

- The local voltage difference between the gate and the channel varies from V_G to $V_G - V_D$. The charge density at a point *x* along the channel:

$$Q_d(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}]$$

$$I_D = -WC_{ox}[V_{GS} - V(x) - V_{TH}]v$$





Derivation of I/V Characteristics

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$$v = \mu E$$

$$E(x) = -dV/dx$$

Derivation of I/V Characteristics

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$$v = \mu E$$
$$E(x) = -dV/dx$$

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

where V(0) = 0 and V(L) = V_{DS}

Derivation of I/V Characteristics

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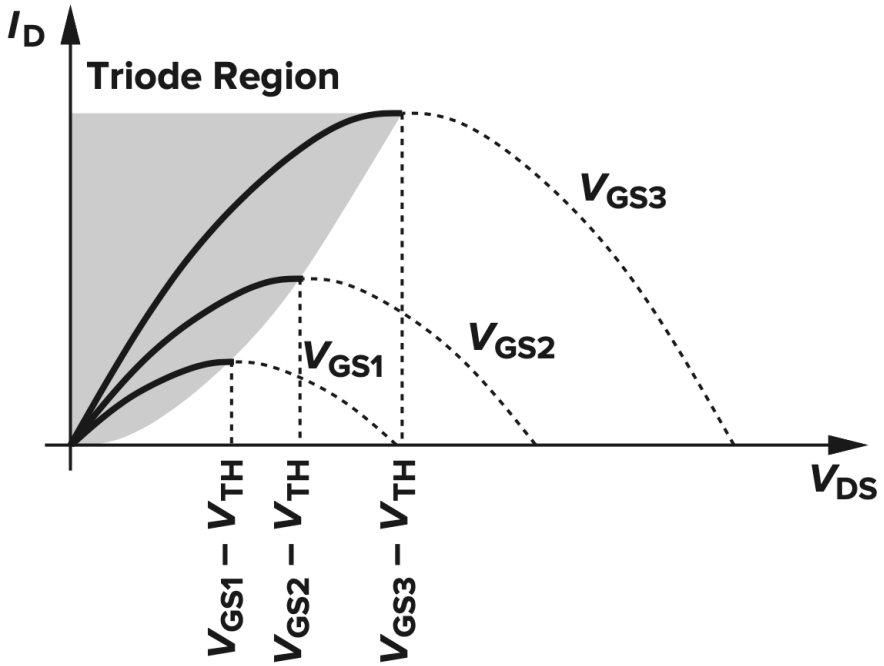
where V(0) = 0 and V(L) = V_{DS}

$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dV$$

$$\boxed{I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]}$$

I_D vs. V_{DS} in the triode region

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

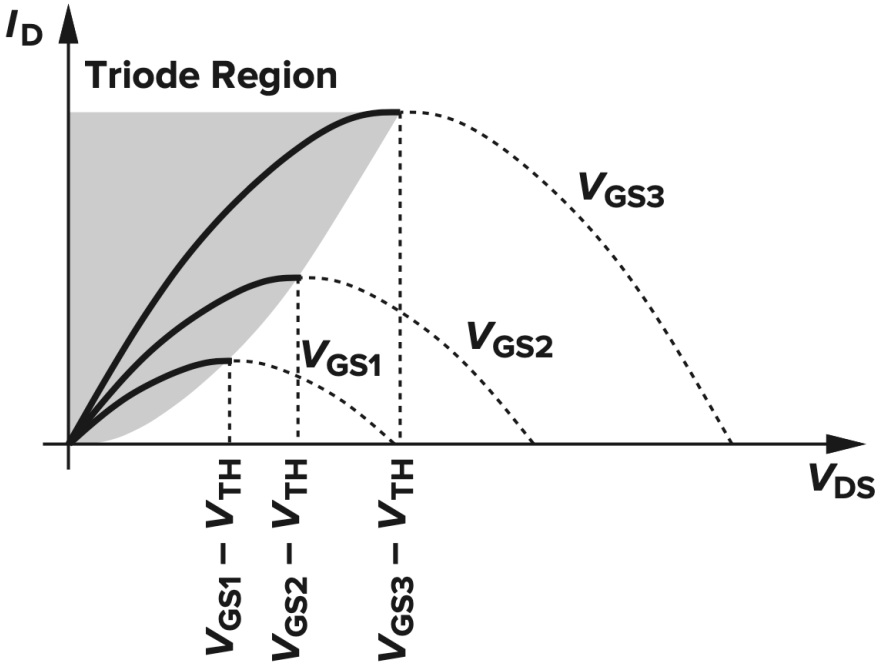


I_D vs. V_{DS} in the triode region

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_{D,max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

- ***The overdrive voltage:*** $V_{GS} - V_{TH}$
- ***The aspect ratio:*** *W/L*



I_D vs. V_{DS} in the triode region

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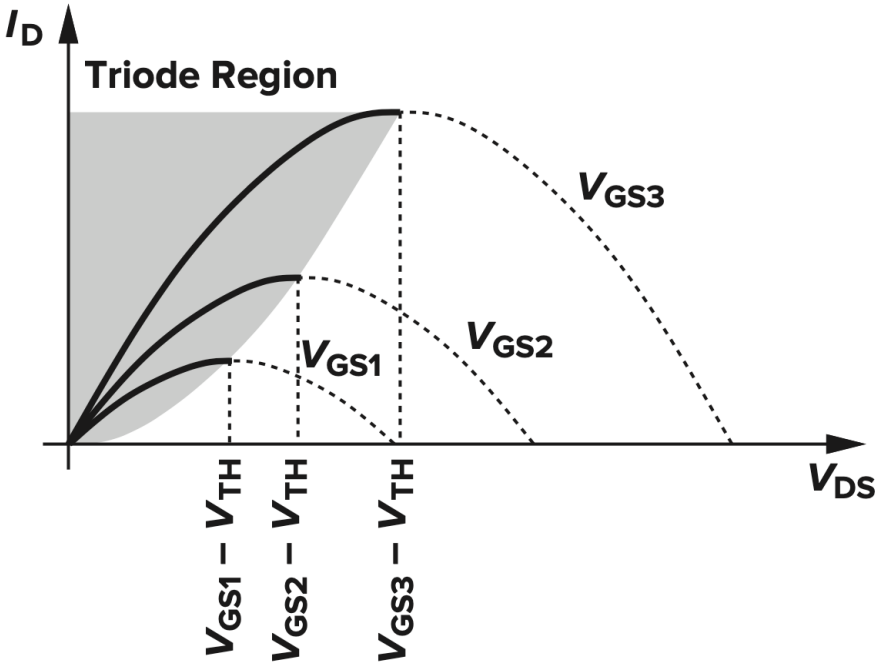
- ***The overdrive voltage:*** $V_{GS} - V_{TH}$
- ***The aspect ratio:*** *W/L*

$$V_{DS} \leq V_{GS} - V_{TH}$$

$\downarrow$ *or* $V_{GD} > V_{TH}$

- The device operates in the "**triode**" region (or **linear** region)



I_D vs. V_{DS} in the triode region

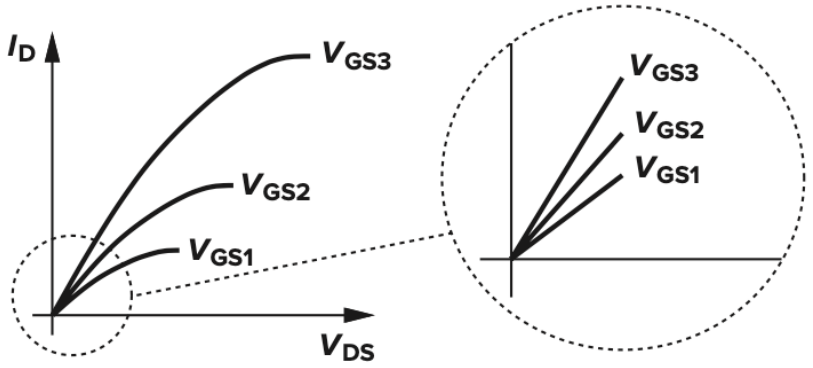
$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$V_{DS} \ll 2(V_{GS} - V_{TH})$$

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

- ***The drain current is a linear function of V_{DS}***

Deep triode region



I_D vs. V_{DS} in the triode region

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$$V_{DS} \ll 2(V_{GS} - V_{TH})$$

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

- ***The drain current is a linear function of V_{DS}***

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

Deep triode region