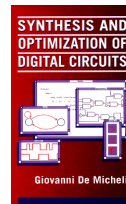


Networks on Chips

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Module 1

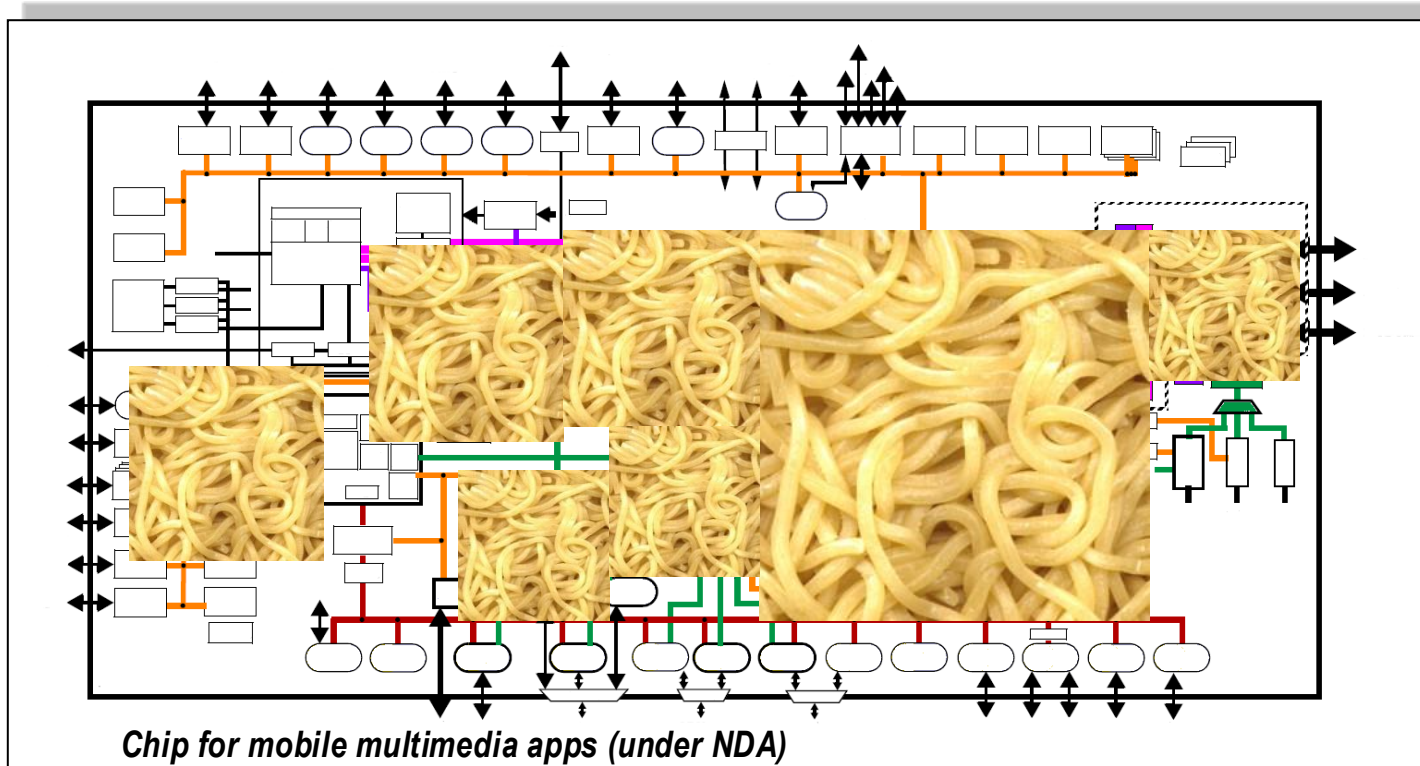
- u **Networks on Chips**

- s **Motivation**

- s **Concept**

- s **Design automation**

Smart interconnect



Nocs in a nutshell

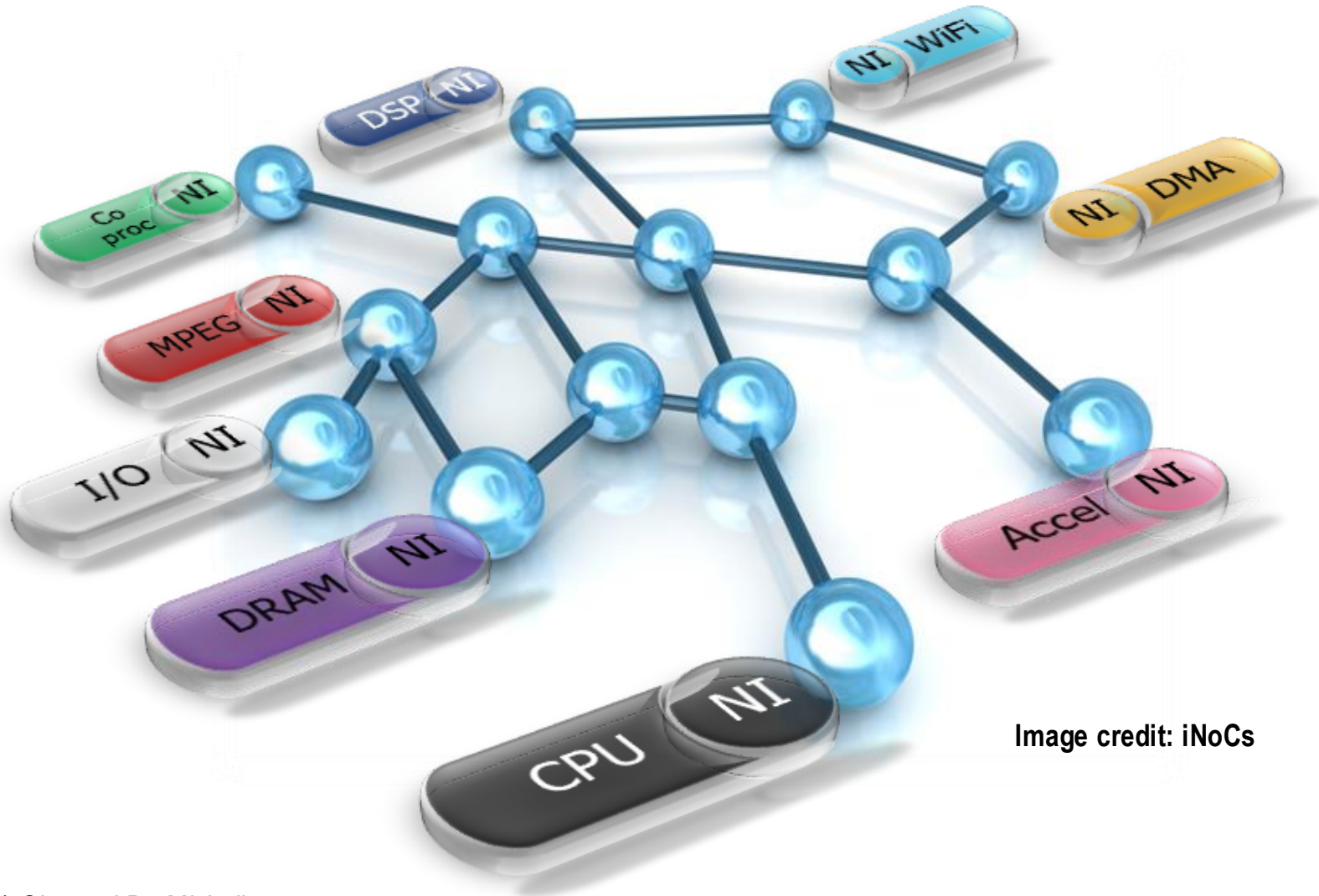


Image credit: iNoCs

The Main Promises

- u ***Scalability***

- s Hundreds/thousands of connected cores

- u ***Tunable Power/Frequency/Area***

- s With data packetization, links can be tuned locally:

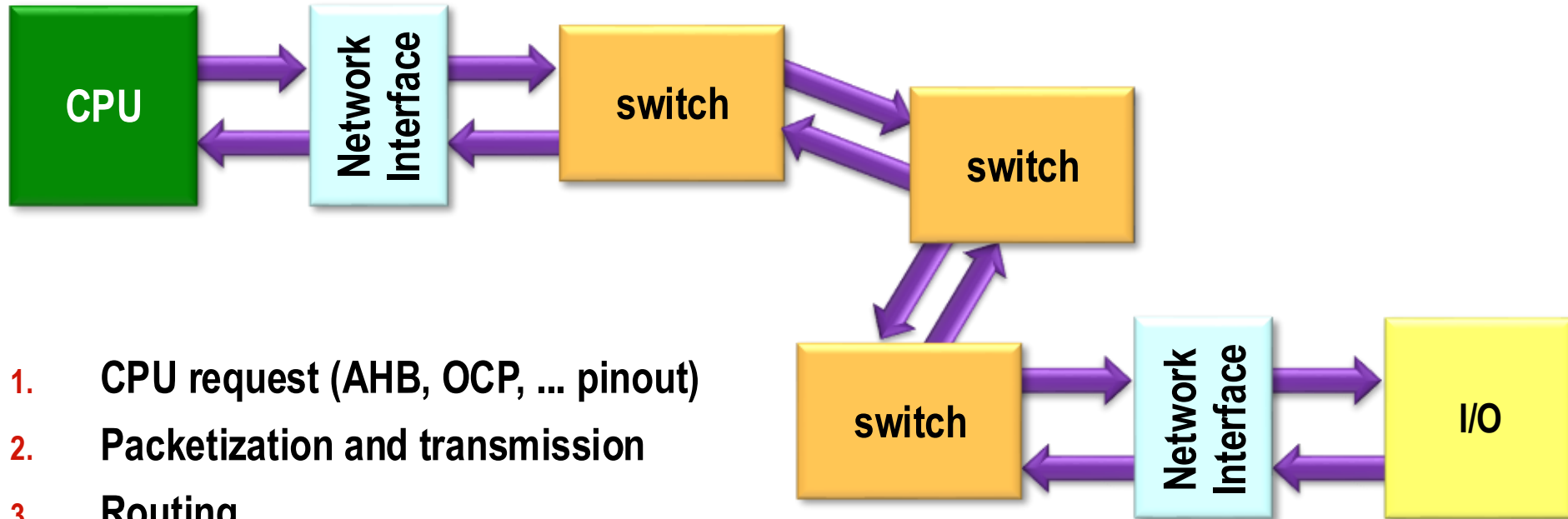
- t Wide or narrow, fast or slow, ..

- u ***Easier design closure***

- s Fewer, shorter, point-to-point wires

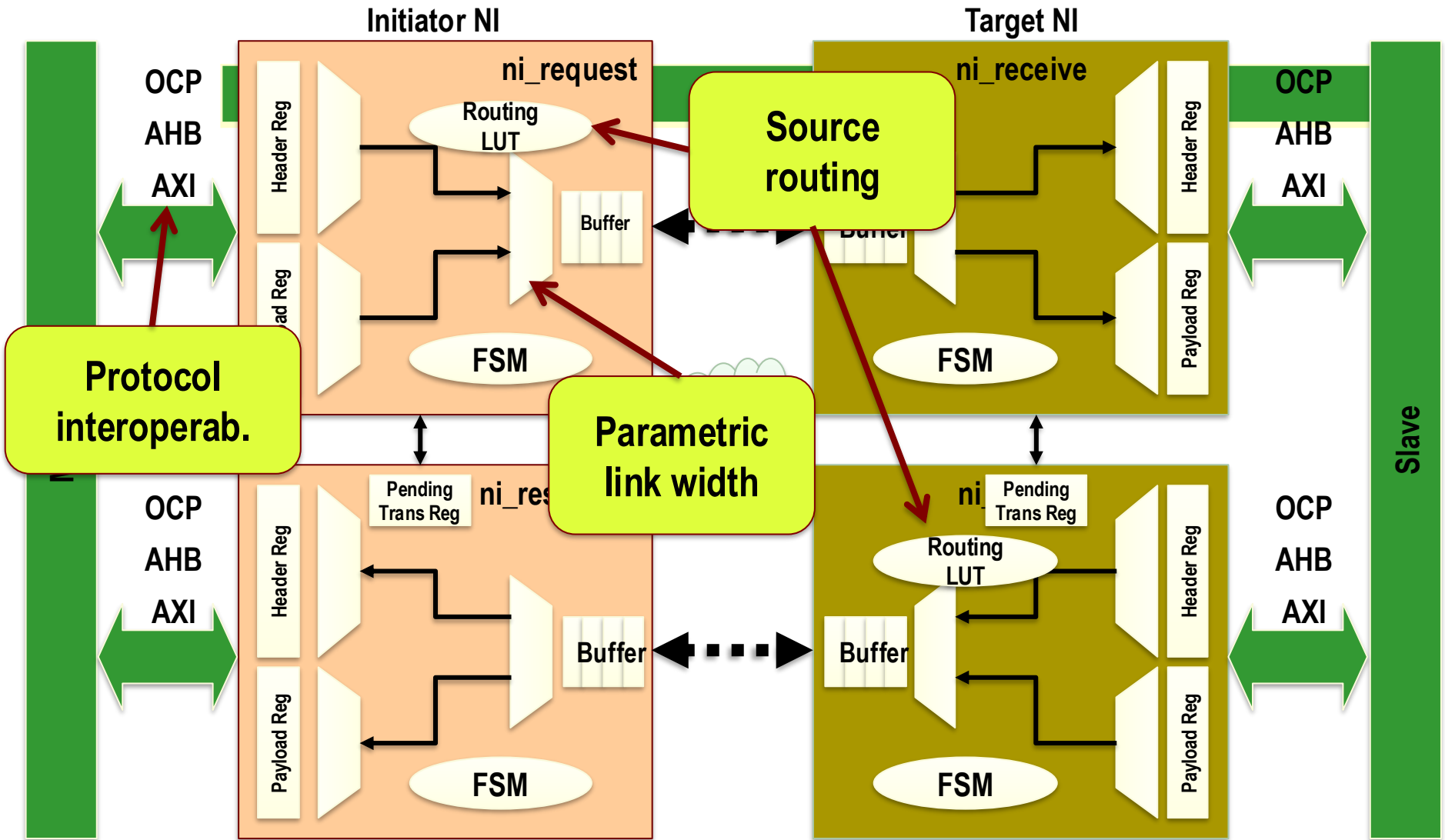
- s Decentralized nature suited to multiple clock/power domains

NoC Operation Example

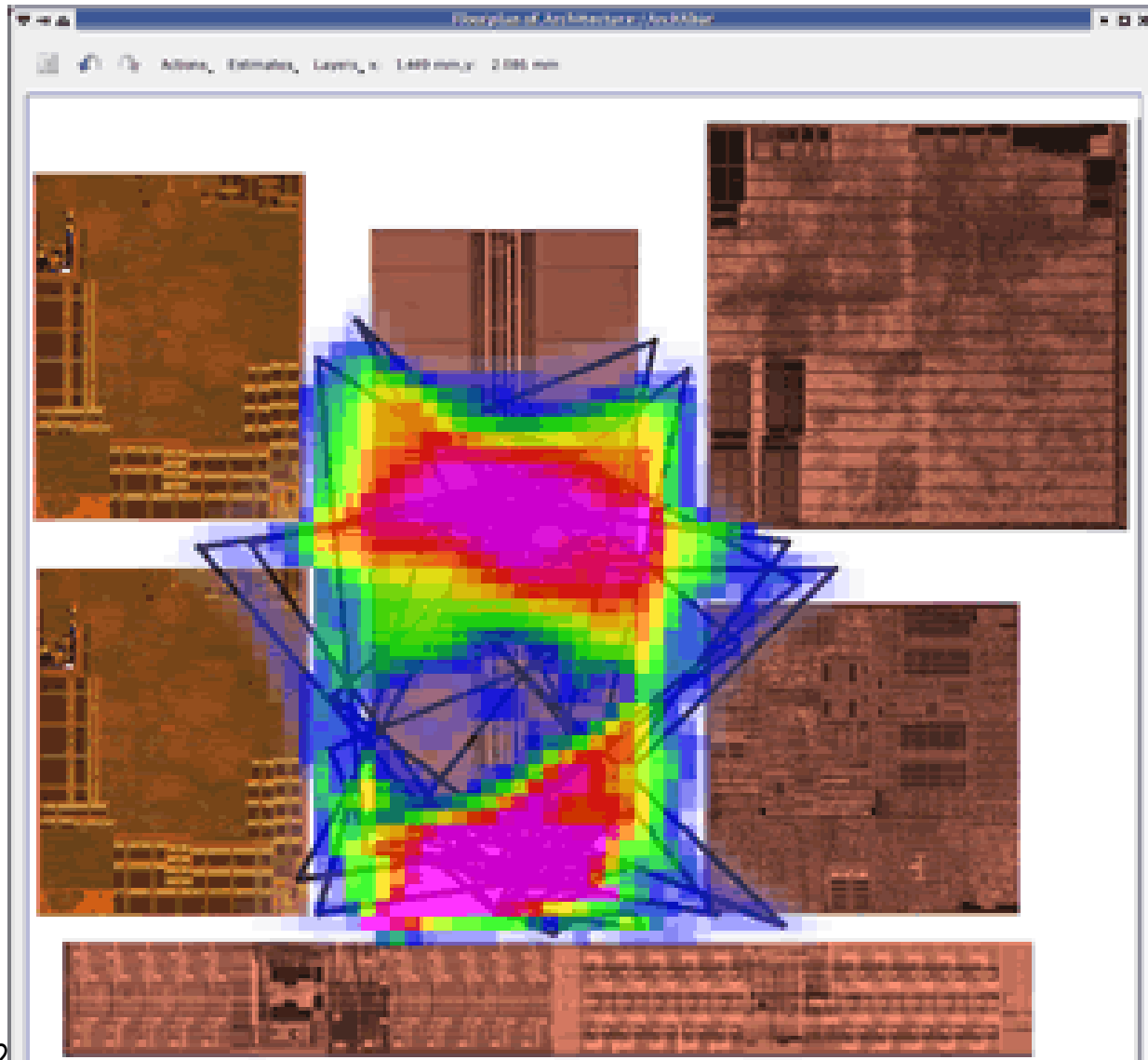


1. CPU request (AHB, OCP, ... pinout)
2. Packetization and transmission
3. Routing
4. Receipt and unpacketization (AHB, OCP, ... pinout)
5. Device response (if needed)
6. Packetization and transmission
7. Routing
8. Receipt and unpacketization

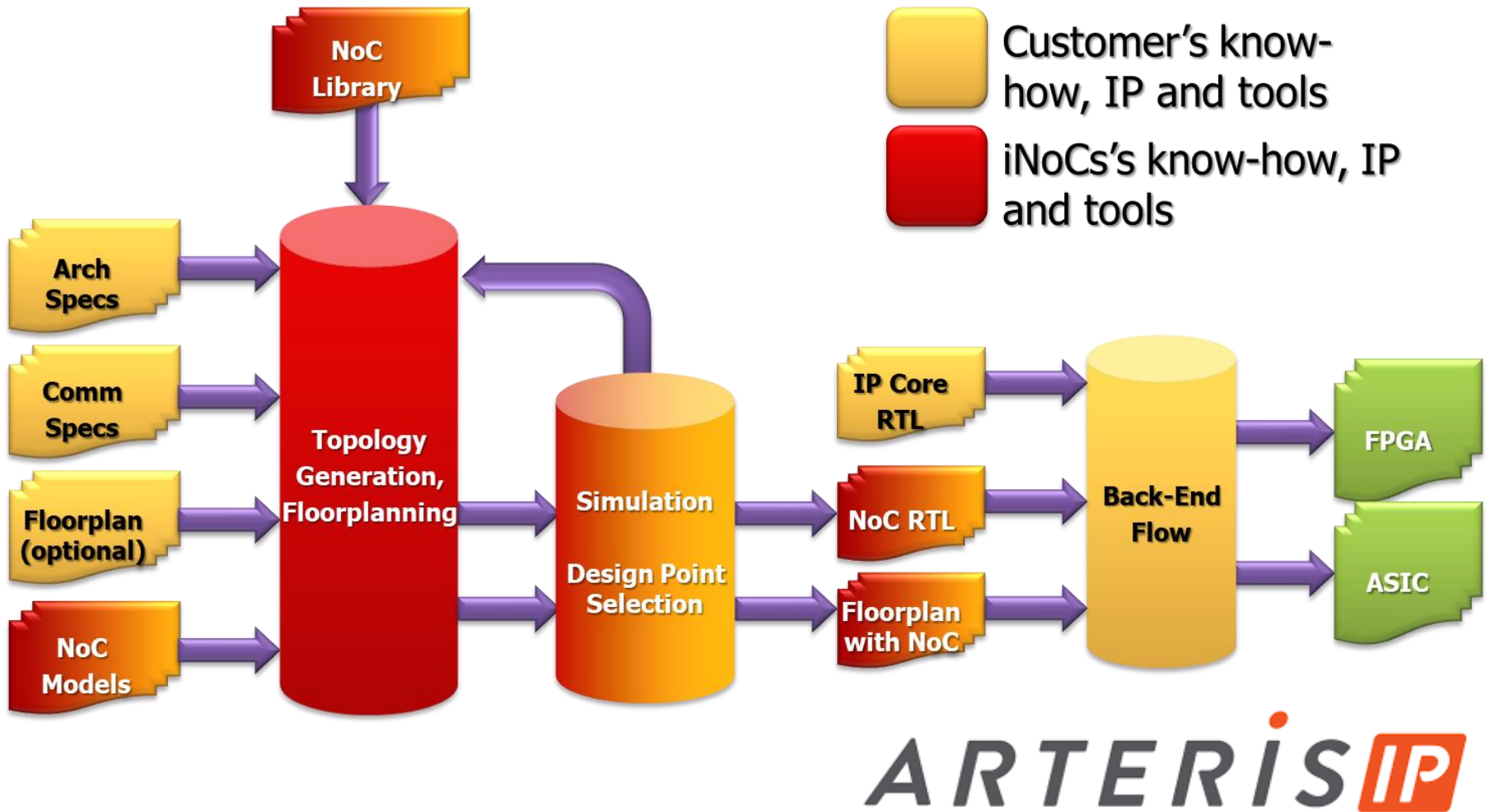
NoC synthesis: xPIPES



Routing congestion is an issue



Layout-aware NoC Synthesis



NoC outlook

- u NoCs have been with us for 20+ years**
- u An unmitigated success in research and products**
- u Further research:**
 - s Chip complexity keeps scaling up and new challenges (e.g. resilience, coherence) become prominent**
 - s NoCs must cover extremely-high-performance as well as extremely-low-power designs, seamlessly**

Summary

- u **High-level synthesis**
- u **Synthesis of hardware units (e.g., accelerators)**
 - s **Behavioral optimization:**
 - t Create abstract models from HDL models
 - t Optimize models without considering implementation parameters
 - s **Architectural synthesis and optimization**
 - t Consider resource parameters
 - t Multiple-criteria optimization problem: area, latency, cycle-time
- u **Synthesis of smart interconnect**
 - s **Networks on chip**