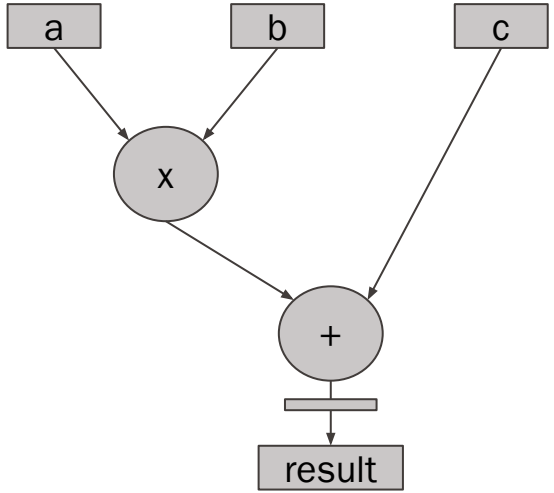
Fusion Compiler Project

- Project to understand and optimize a design with Fusion Compiler (FC)
- Reference design a MAC unit which does:
  - a*b + c
  - a,b, and c are three signed 32b integers
  - result is a signed 32b output
    - yes, it can overflow and for the purpose of this exercise we are ok with it
- Final project requires a PDF answerings the questions that will follow
- Get the project folder at:



/education/classes/2025-2026/CS472/FC_Labs/FC_Labs/labs/project

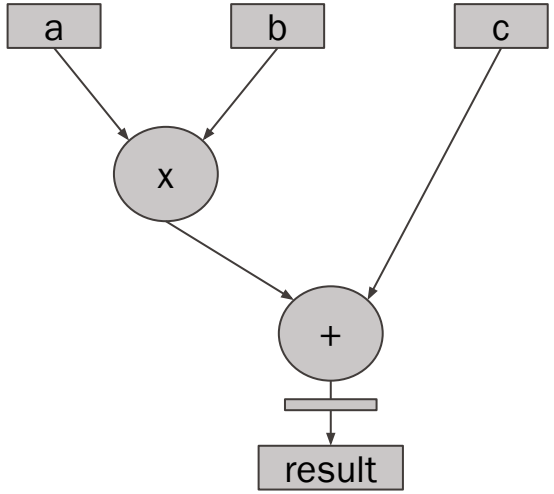
Q1

Given the RTL and the script which contains a 33x33 floorplan
Run the first script:

make run_1

Questions:

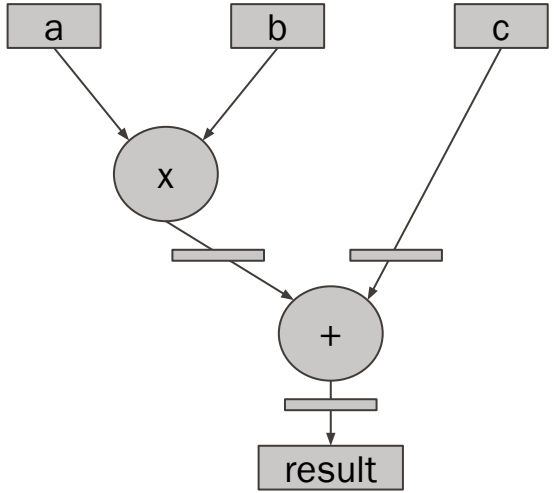
a. **What is the critical path in each compilation step?**
b. Write the chain of cells of the critical path:
   i. **How long it is?**
c. **What is the utilization?**



Q2

Look at the modified RTL mac_unit_2.sv to see how we break the path from the multiplier to the adder as in the Figure. Complete the 2nd script to have a floorplan 36x36 and answers the questions below:

make run_2



Questions:

a. **What is the critical path in each compilation step?**
b. Write the chain of cells of the critical path:
   i. **How long it is?**
c. **What is the utilization?**

Q3 & Q4

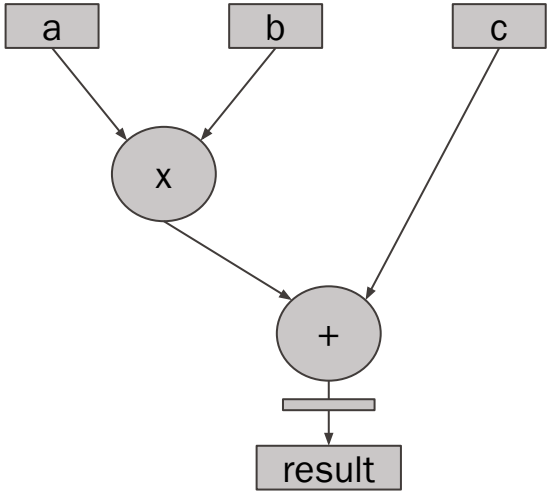
Optimize the floorplan of the **design1** (mac_unit) in project3 and **design2** (mac_unit_2) in project4 to be as small as possible (yet placeable with utilization <100%). Re-run the synthesis of the two design and report a pareto curve graph and table with AREA and LATENCY (where latency is number of cycles to get the valid result * minimum period)

Careful: if you select a too small floorplan, compile_fusion will raise an error

DESIGN	AREA (WxH) [um^2]	LATENCY [ns]
design1		
design2		

Q5

Optimize the floorplan of the design1 (mac_unit) in project5 a to be as fast as 1.5ns (yet placeable with utilization <100%). Re-run the synthesis of the design and compare its LATENCY-AREA against the previous designs.



Questions:

a. **What is the critical path in each compilation step?**
b. Write the chain of cells of the critical path:
   i. **How long it is?**
c. **What is the utilization?**
d. **What is the throughput?**
e. **What is the latency?**

Q6

Modify the floorplan to be as little as possible and and synthesized the mac_unit_3.sv which uses 16b datapath
Complete the 3rd script and answers the questions below:

Questions:

a. **What is the critical path in each compilation step?**
b. Write the chain of cells of the critical path:
   i. **How long it is?**
c. **What is the utilization?**
d. **What is the throughput?**
e. **What is the latency?**
f. **Explain the different architectures with PROs and CONS**
g. **Draw the dataflow graph**

$$A_{32} * B_{32} =$$
$$_{u}AL_{16} * _{u}BL_{16} +$$
$$_{s}AH_{16} * _{u}BL_{16} << 16 +$$
$$_{s}BH_{16} * _{u}AL_{16} << 16 +$$
$$\cancel{_{s}AH_{16} * _{s}BH_{16} << 32}$$

Where s or u means signed or unsigned and 32 and 16 means data width and H or L means higher (31:16) or lower part (15:0)

Report

- Complete and understand the previous scripts
- Write a **PDF report** answering the previous questions:
  - **Max 2 pages**
  - **Each question** is **worth one point**
  - **Deadline Thursday 6th 23:59**
  - **Submission though Moodle**