Introduction to quantum science and technology

Lecture #2 – Adrian M. Ionescu

- Quantum Mechanical effects in nanoelectronic devices
- **Single Electron Transistors: nanofabrication, co-design with CMOS and applications**

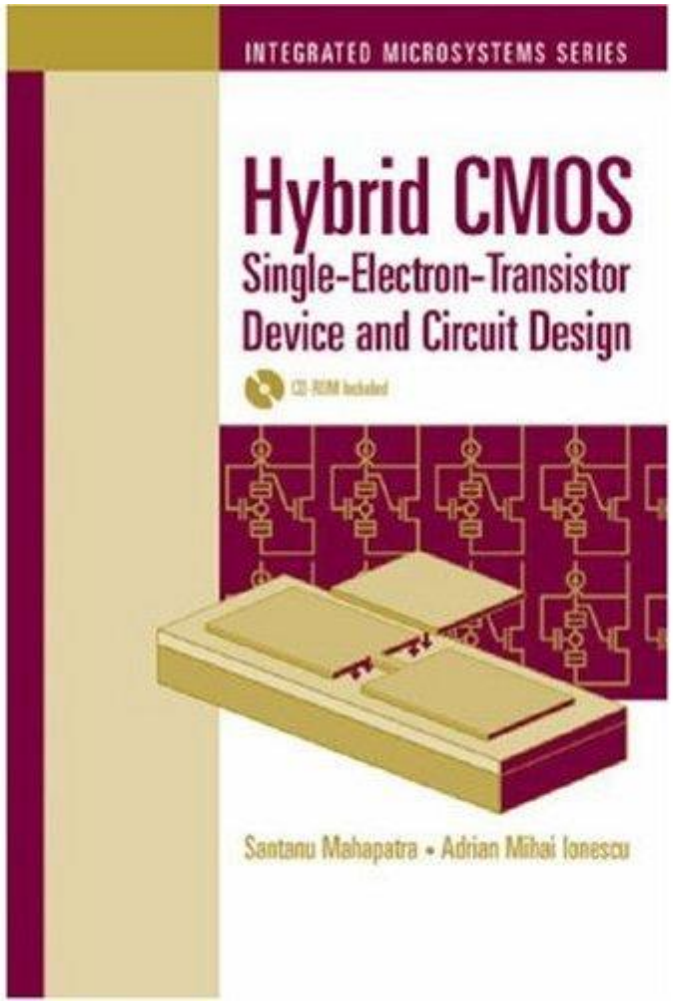
References

THEORY

1. C. Wasshuber, **Computational Single-Electronics**
Springer, 2001.

PRACTICAL DESIGN AND HYBRIDIZATION WITH CMOS

2. S. Mahapatra and A.M. Ionescu, **Hybrid CMOS-SET Single Electron Transistor Device and Circuit Design**
Artech House, Boston, 2006.



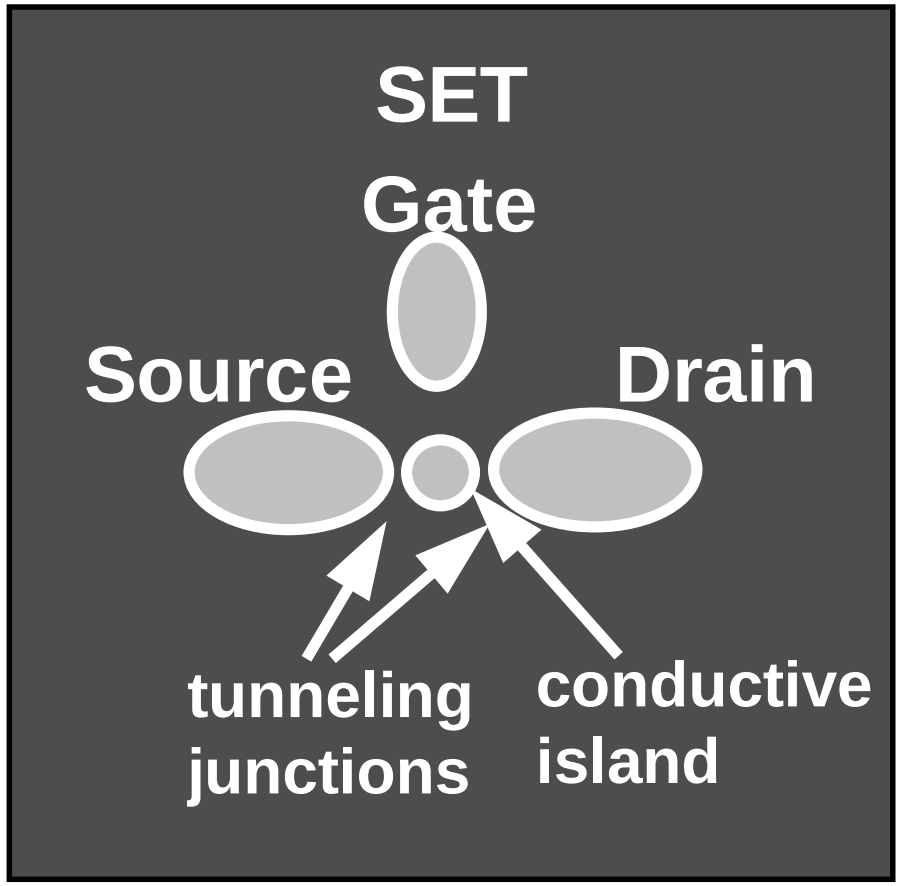
Key questions

- What is a single electron transistor (SET)?
- How SET operates?
- Why we need SETs? Applications?
- What technology should I use to fabricate an SET? Can I do it in an academic clean room?
- Is SET technology compatible with silicon CMOS? Is it possible to co-fabricate them?
- Any benefits in the co-design of SET and CMOS on silicon platforms? Low power? Speed? Other functionalities?

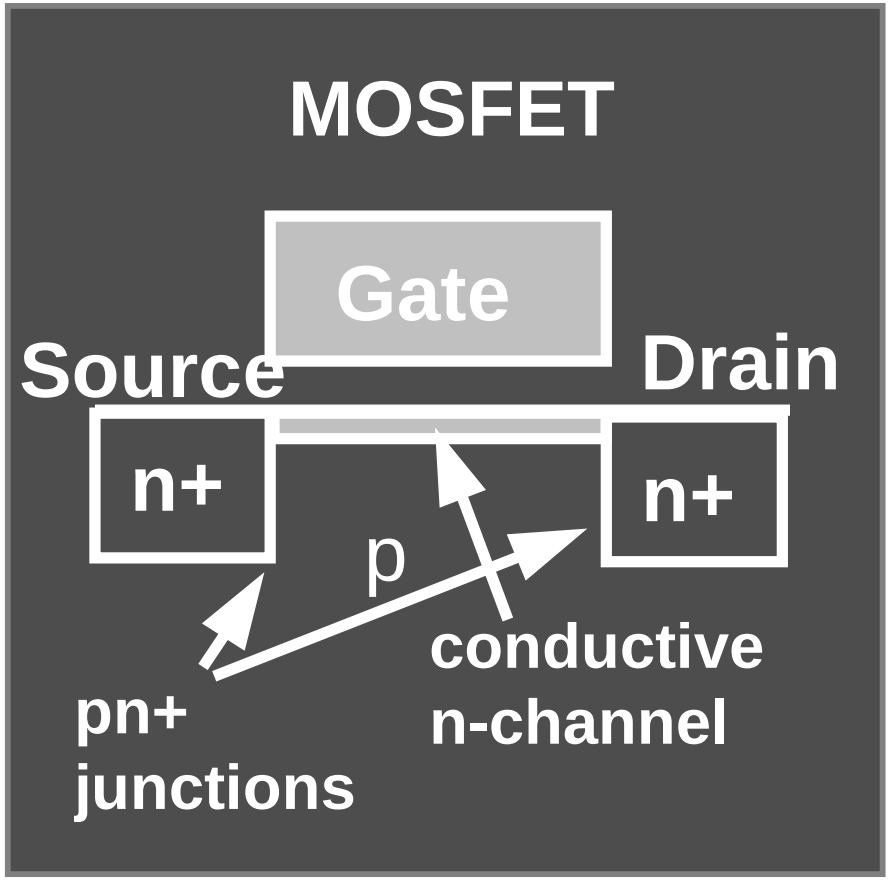
What is Single Electron Transistor (SET)?

SET is a 3-terminal **electronic switch** using **Coulomb blockade**

Single Electron Transistor

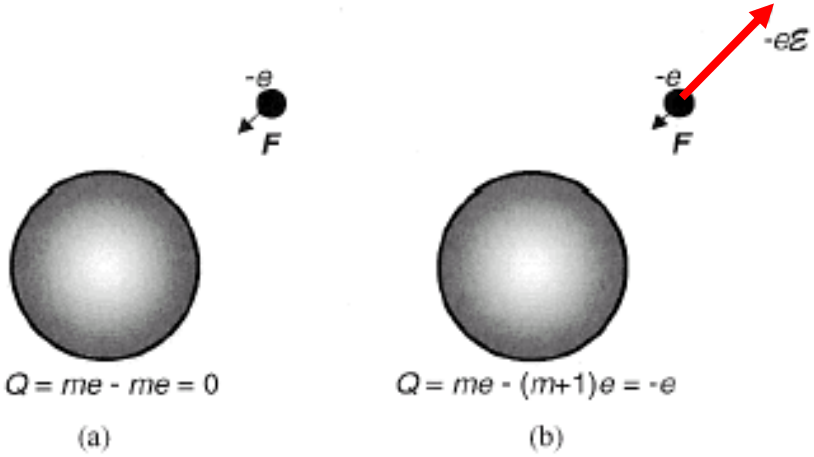


MOSFET



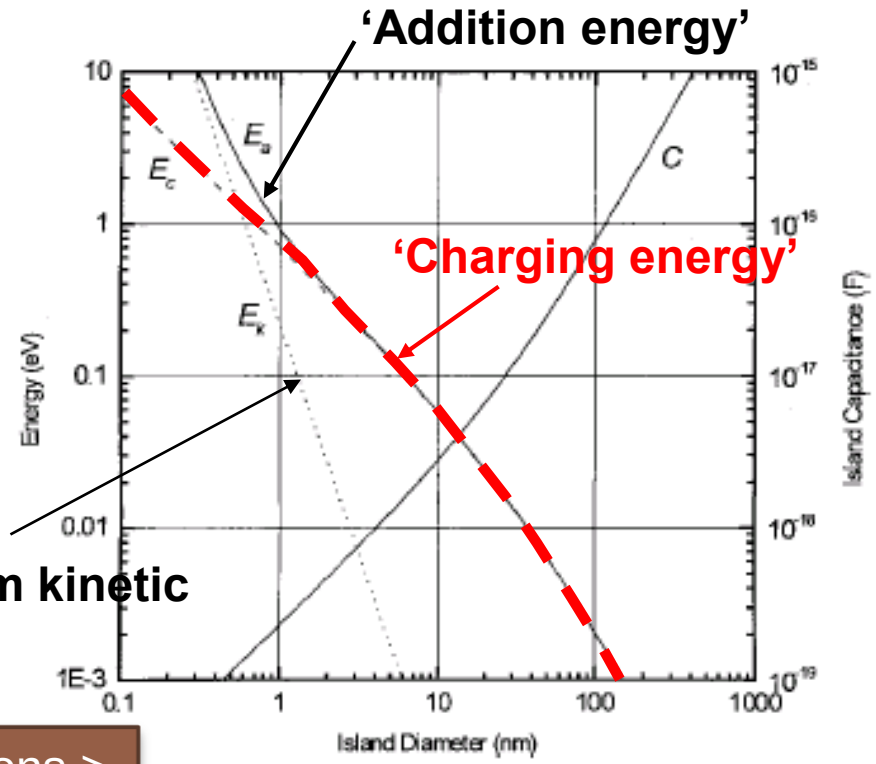
Electrostatics of charged dots: Coulomb repulsion

Repulsion force from charged dot



Neutral

Charge :
-e =1.6 x 10^{-19} Coulomb



For dimensions > 1nm: $E_k << E_c$, no quantization of energy

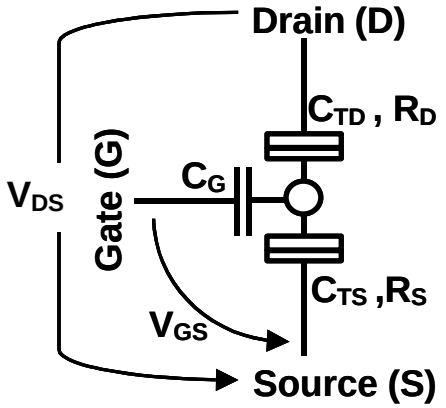
Charging energy :

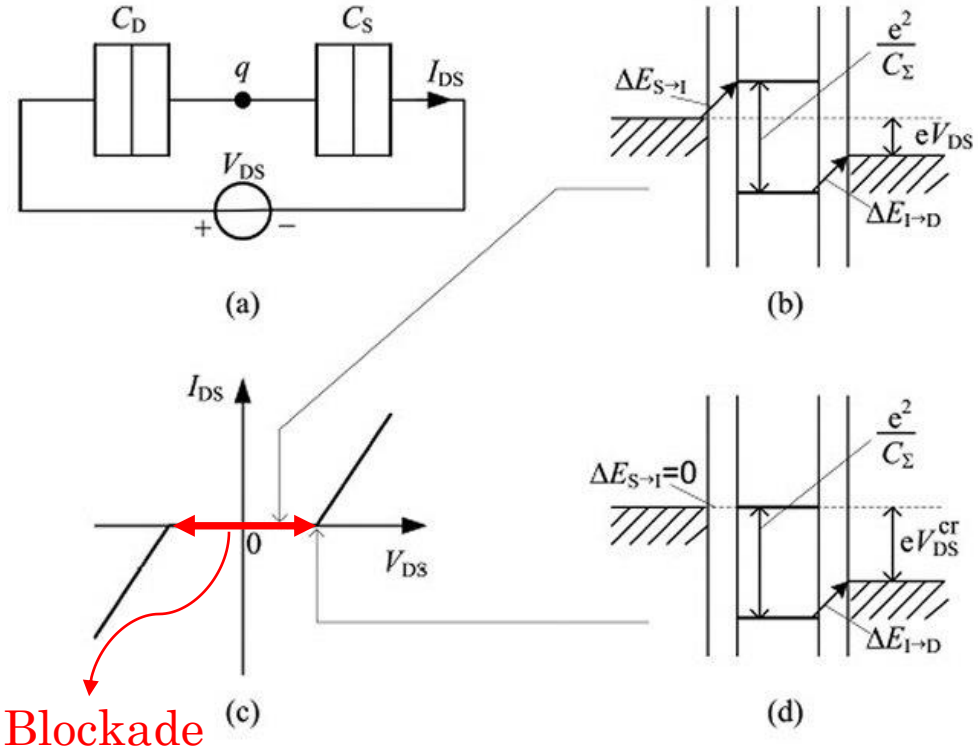
$$E_C = \frac{e^2}{C}$$

How SET operates?

- The key point is that **charge passes through the island in quantized units**. For an electron to hop onto the island, its energy must equal Coulomb energy, $e^2/2C$.
- When both the gate and bias voltages are zero, electrons do not have enough energy to enter the island and current does not flow.
- As the bias voltage between the source and drain is increased, an electron can pass through the island when the energy in the system reaches the **Coulomb energy**.
- This effect is known as the **Coulomb blockade**, and the critical voltage needed to transfer an electron onto the island, equal to e/C, is called the **Coulomb gap voltage**.

Equivalent circuit:





Coulomb Blockade

SET electrostatics

- Potential of the island as a function of the number of electrons for a **SET with two gates**:

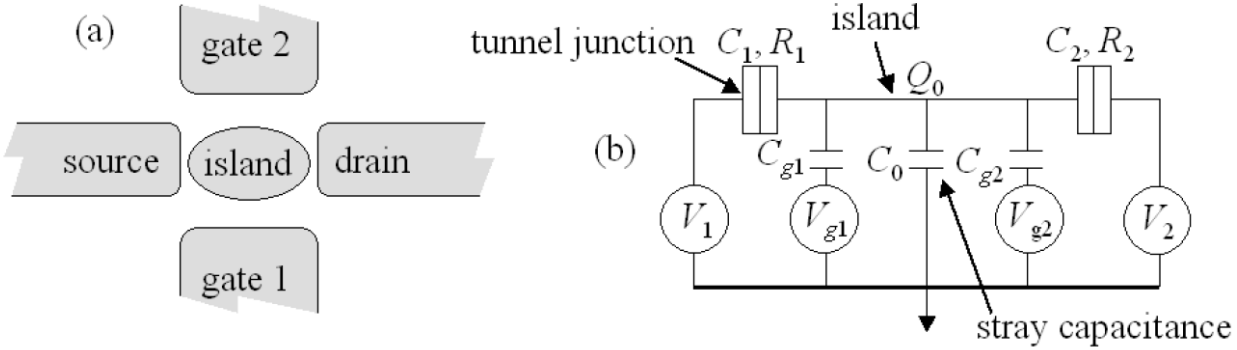
$$V(n) = (-ne + Q_0 + C_1V_1 + C_2V_2 + C_{g1}V_{g1} + C_{g2}V_{g2})/C_\Sigma.$$

- **The energy for an electron to be placed from ground to the island**:

$$\int_0^{-e} V dq = -eV(n) + \frac{e^2}{2C_\Sigma}. \qquad C_\Sigma = C_1 + C_2 + C_{g1} + C_{g2} + C_0.$$

- **Four tunnel events** – if any of these energies is negative tunneling takes place:

$$\Delta E_{1R} = eV_1 - eV(n) + E_c, \quad \Delta E_{1L} = -eV_1 + eV(n) + E_c,$$
$$\Delta E_{2R} = -eV_2 + eV(n) + E_c, \quad \Delta E_{2L} = eV_2 - eV(n) + E_c.$$



How SET works? Orthodox theory

- SET principle (orthodox theory): K.K. Likharev, 1985
- SET first experimental validation: Fulton & Dolan, 1986

Orthodox theory of Single Electron Transistor

- **Tunnel resistance is much higher than quantum resistance:**
  $R_{TD,S} >> R_Q = h/e^2 = 25.8 k\Omega$
- **Quantization of energy is neglected :**
  $E_K << k_B T$ ou $E_K << E_C$
- **Tunneling time is neglected: ~10^{-14} - 10^{-15} s**
- **Co-tunneling (multiple) is neglected**

$$\Delta E \times \Delta t \geq h \rightarrow \frac{e^2}{C} \times R_T C \geq h$$

$$R_T \geq R_Q = \frac{h}{e^2} \cong 25.8 k\Omega$$

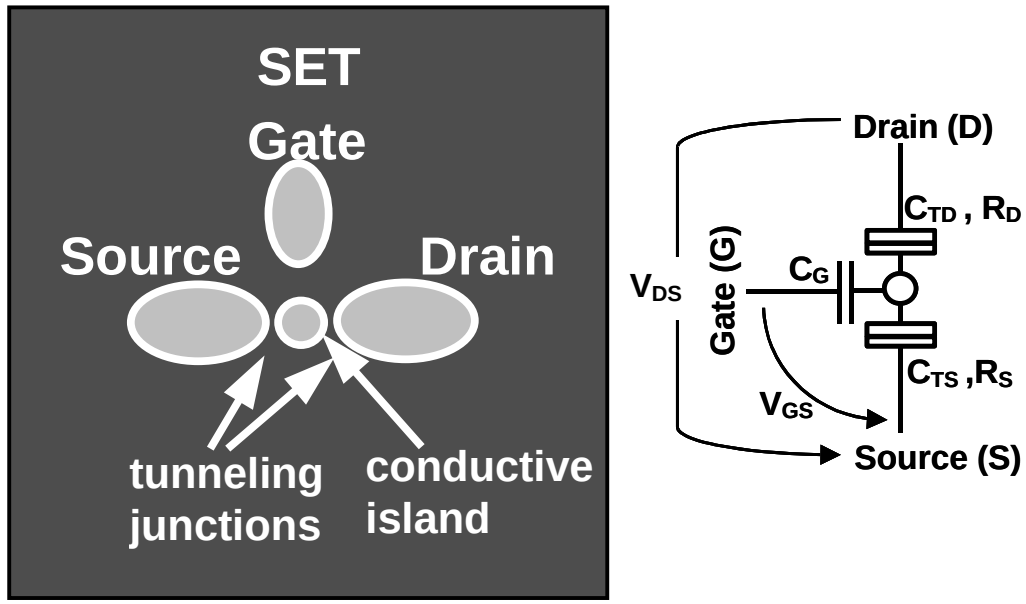
SET is not a real quantum device:

- ❖ charge is discrete
- ❖ energy & current are not

R_Q is not 'real' resistance but a quantum phenomenological resistance

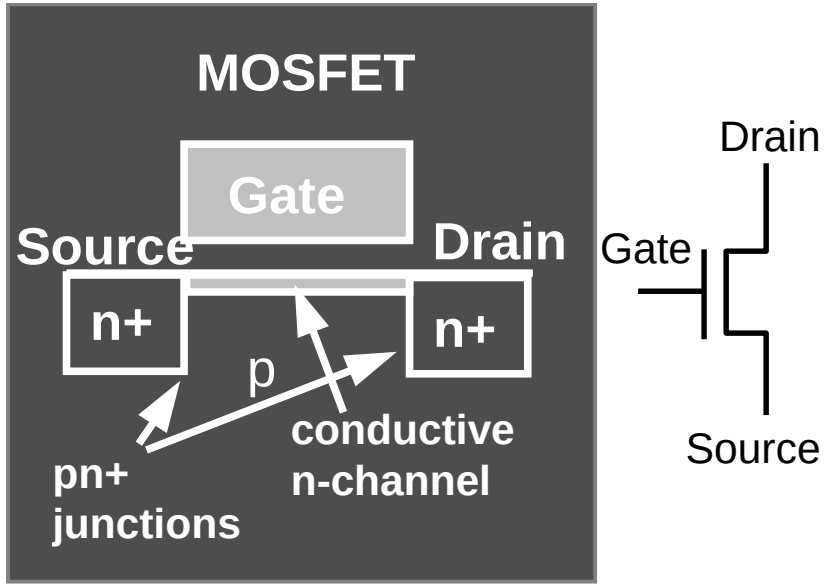
SET versus MOSFET

Single Electron Transistor (SET)



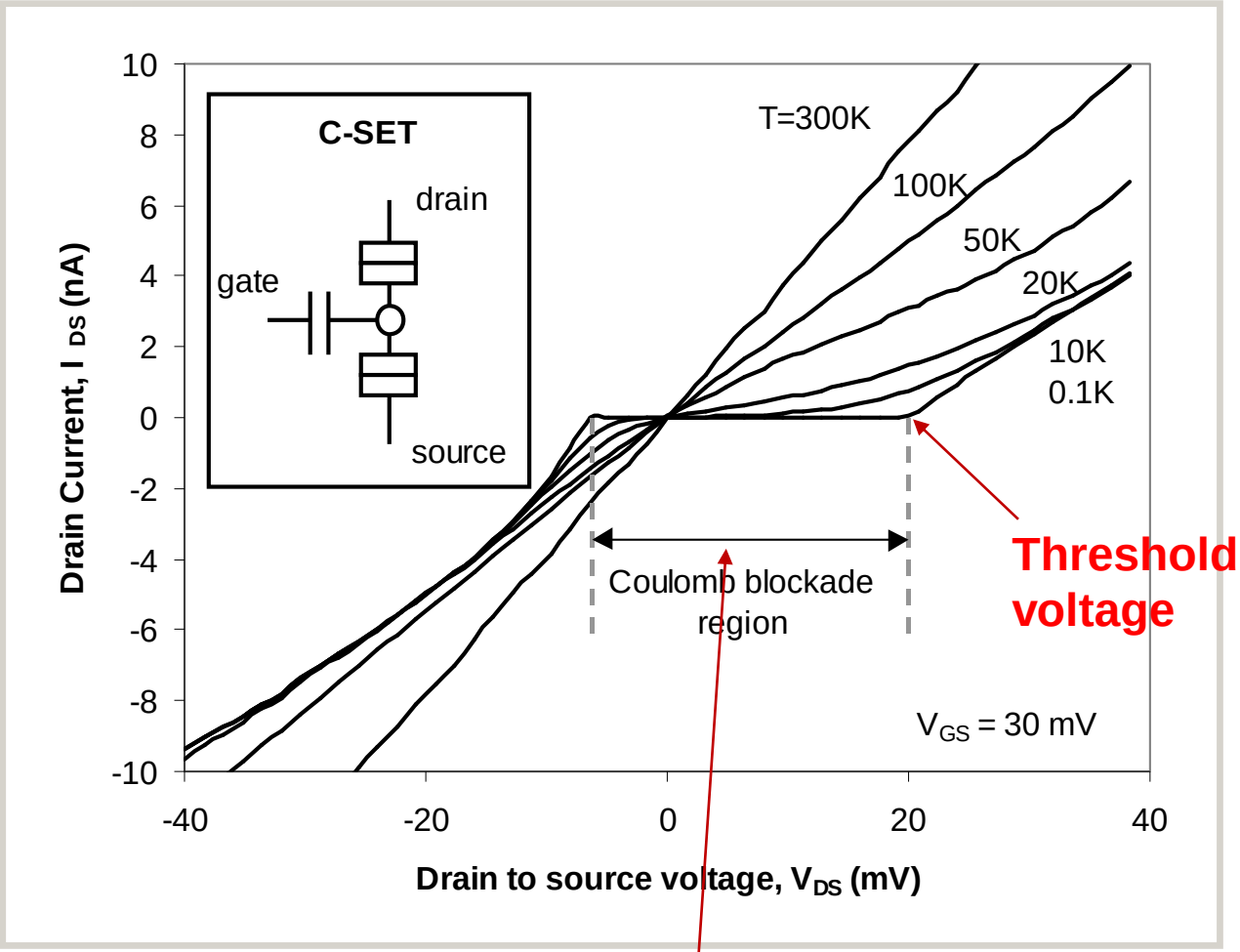
- electron conduction is <u>one by one</u> (!)
- drain & gate control <u>Coulomb blockade (CB)</u>
- needs <u>opaque junctions</u>:
  $R_T > R_Q \sim 26kW$
- needs <u>very small island</u> (~1nm) for room temperature operation

MOS transistor (MOSFET)



- <u>many electrons</u> simultaneously participate to the conduction
- gate controls channel
- <u>junctions highly transparent</u>
- works inherently at room temperature

SET: output characteristics & Coulomb blockade



Threshold voltage

Low V_D, current is zero: device is under **Coulomb Blockade**

Key conditions (criteria for good design & fabrication):

1) Electron localized in the island

$$R_T > h/e^2 = R_Q \cong 26k\Omega$$

2) Charging energy higher than thermal energy

$$E_C = e^2/2C_\Sigma > k_B T$$

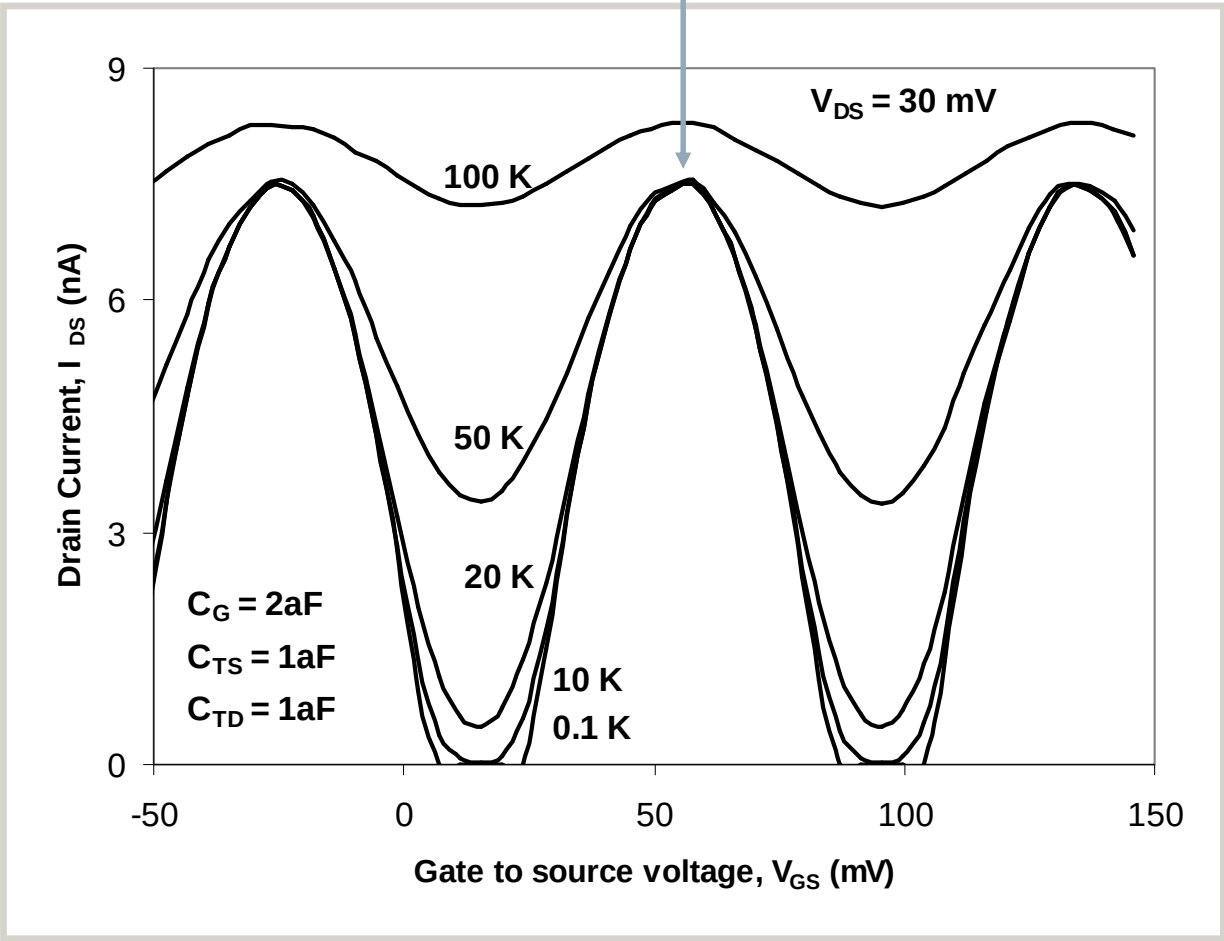
$$E_C >> k_B T$$

$$E_C = (10 \div 40) k_B T$$

SET: oscillating transfer characteristics

$$I_{peak} = V_{DS}/2(R_D + R_S)$$

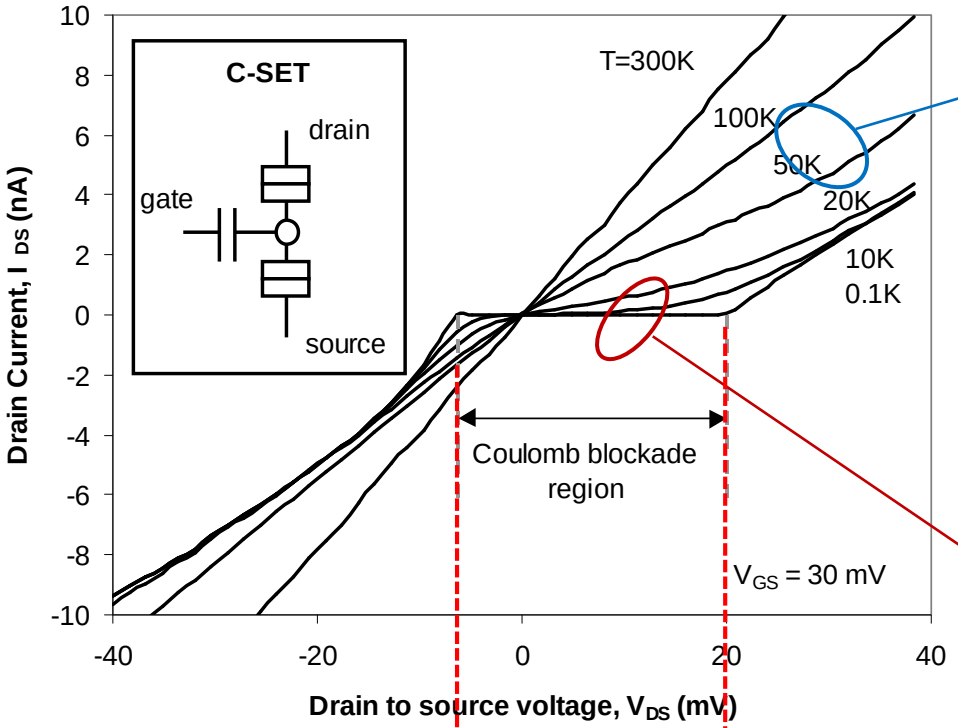
$$V_{peak} = \frac{e}{2C_{G1}} + \frac{C_\Sigma}{C_{G1}}\left(\frac{1}{2} - \frac{C_{TD}}{C_\Sigma}\right)V_{DS}$$



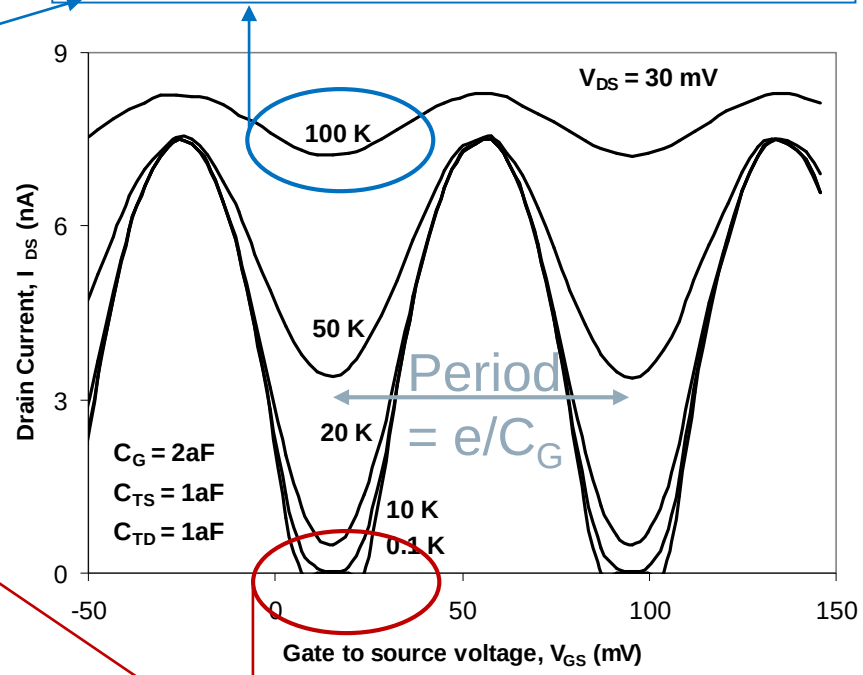
- Current oscillations with V_G resulting in positive and negative values of the transconductance for the same device:
  this is a fundamental difference compared to MOSFET transconductance
- logic can be built with a unique type of transistor (no need of p and n types)

Q: Conditions for room temperature?

SET I-V characteristics: summary



High temperature: CB cancelled



Low temperature: CB works

$$E_C = e^2 / 2C_\Sigma > k_B T$$

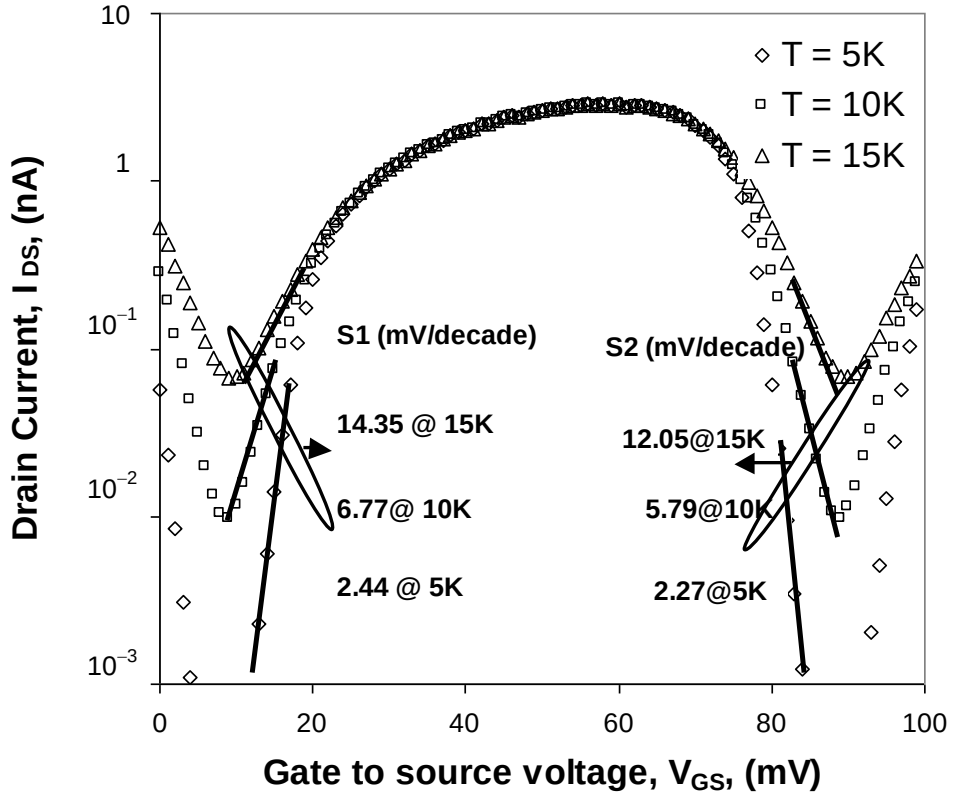
Low V_D: CB works

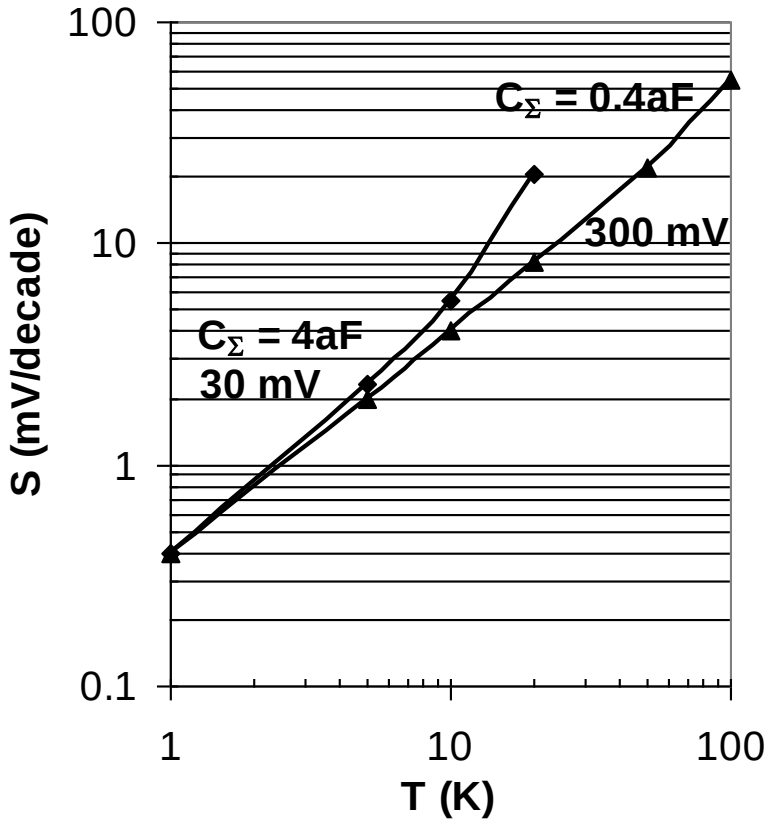
High V_D: CB cancelled

SET has two threshold voltages, in VG and VD!

Is SET a more abrupt switch as Subthreshold Slope?

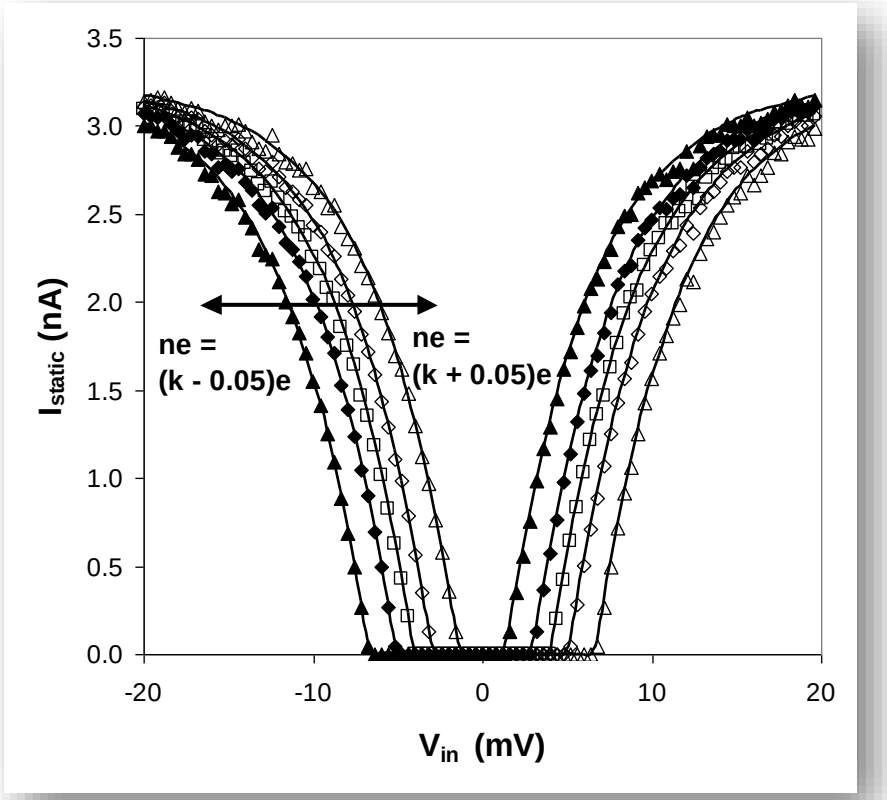
- no easy-to-derive analytical expression of SS for quick comparision
- similations of SET: SS is not better than MOSFET @ room temperature ~ 300K (looks even worse >100mV/decade)
- interesting values for T < 20K, as many issues with MOS at such low temperatures (the slope saturates)



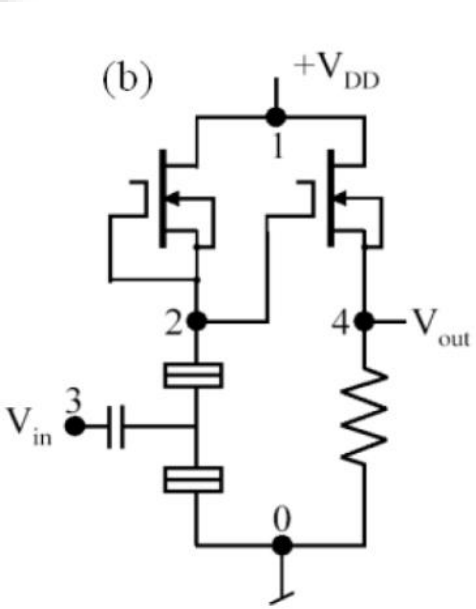


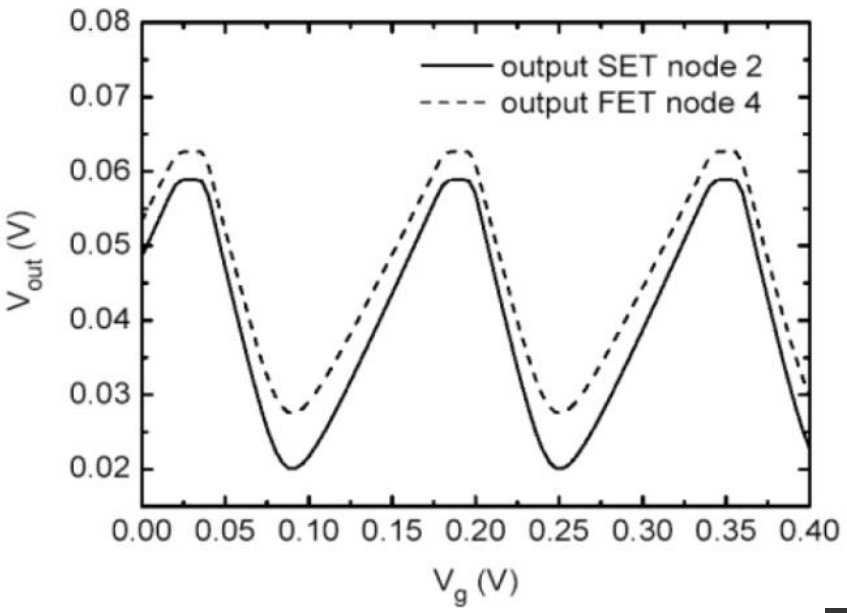
Key issue of C-SET: background charge (BC) sensitivity

- The origin of the background charge problem is the extreme charge sensitivity of SET's. A single charged vacancy or an interstitial ion in the oxide near a SET can be enough to switch the transistor from the being conducting to being nonconducting.
- Needs quasi-ideal (charge-free materials) or adapted circuit design for charge-induced I-V shift compensation.



Charged lock loop that automatically tunes away the background charge (BC).

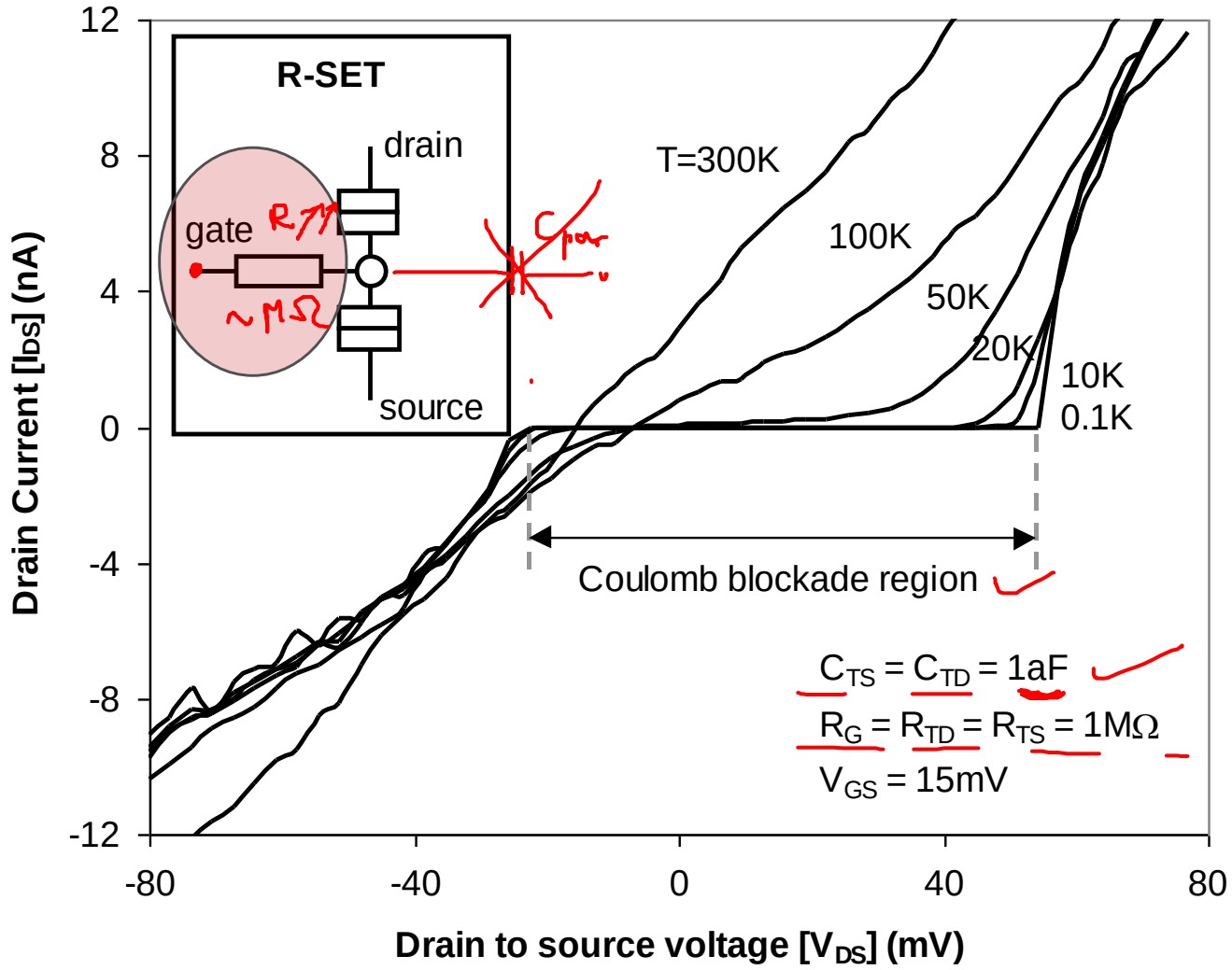




R-SET: no backgroud charge sensitivity

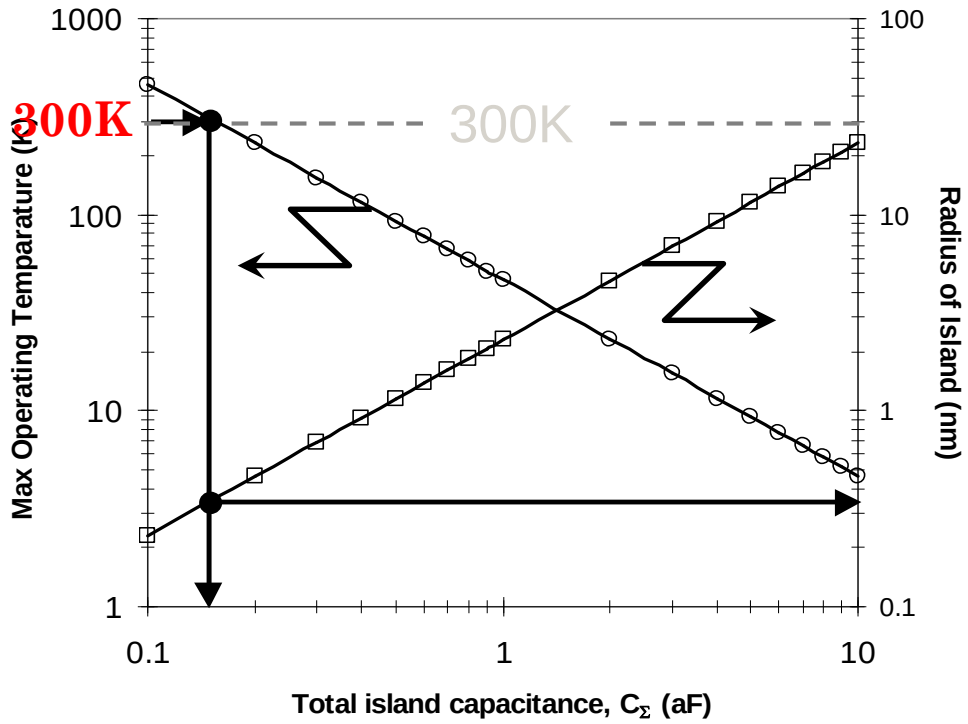
Possible theoretical solution, resistive SET, R-SET:

- *Issues are the resulting gate current and practical implementation of such resistance in nanotechnology.*
- *Never reported in practice.*



Room temperature operation for SET logic

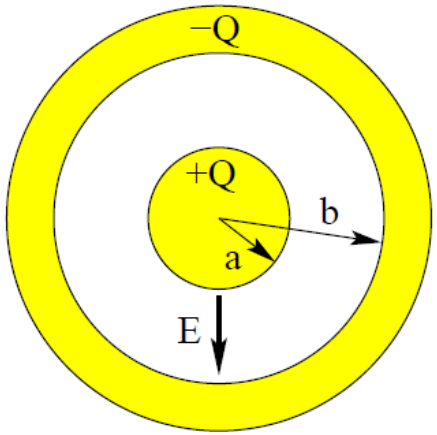
Dimensions needed for Room Temperature (RT) Operation



Sub-1nm Dot size for operation @ T~300K

$$E_C = 40 k_B T$$

$$C \equiv \frac{Q}{V} = 4\pi\epsilon_0 \frac{ab}{b-a}$$



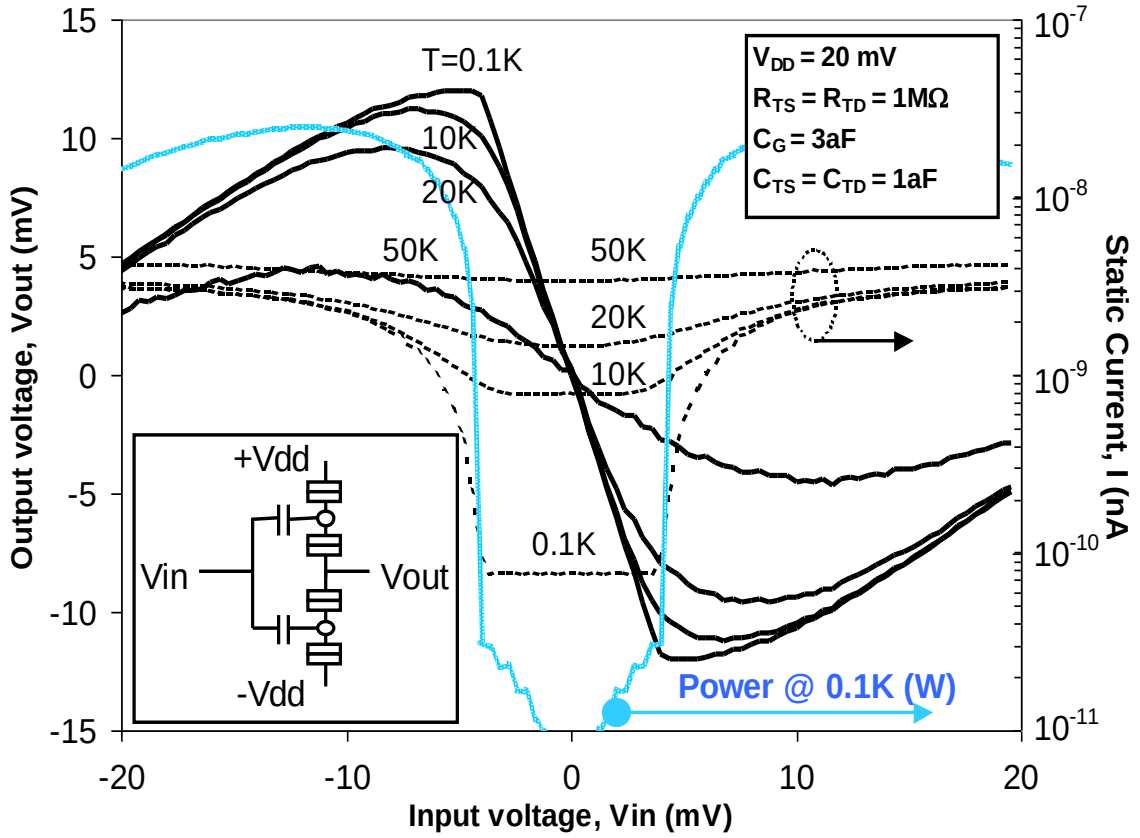
- Replace ε_0 with ε_{SiO2}

Low Power SET logic

Digital SET ICs possible with the same type of SET, achieves ultra low power consumption

- Almost all digital CMOS ICs can be replicated with SET but they lack current drive and speed!
- **SET inverter**
  - **with two identical SETs**
  - power dissipation is essentially static:

    Power ~ 10^{-8}-10^{-9} W
    4-5 decades lower than CMOS!
  - very sensitive to temperature: works under Coulomb Blockade



Key questions: SET fabrication

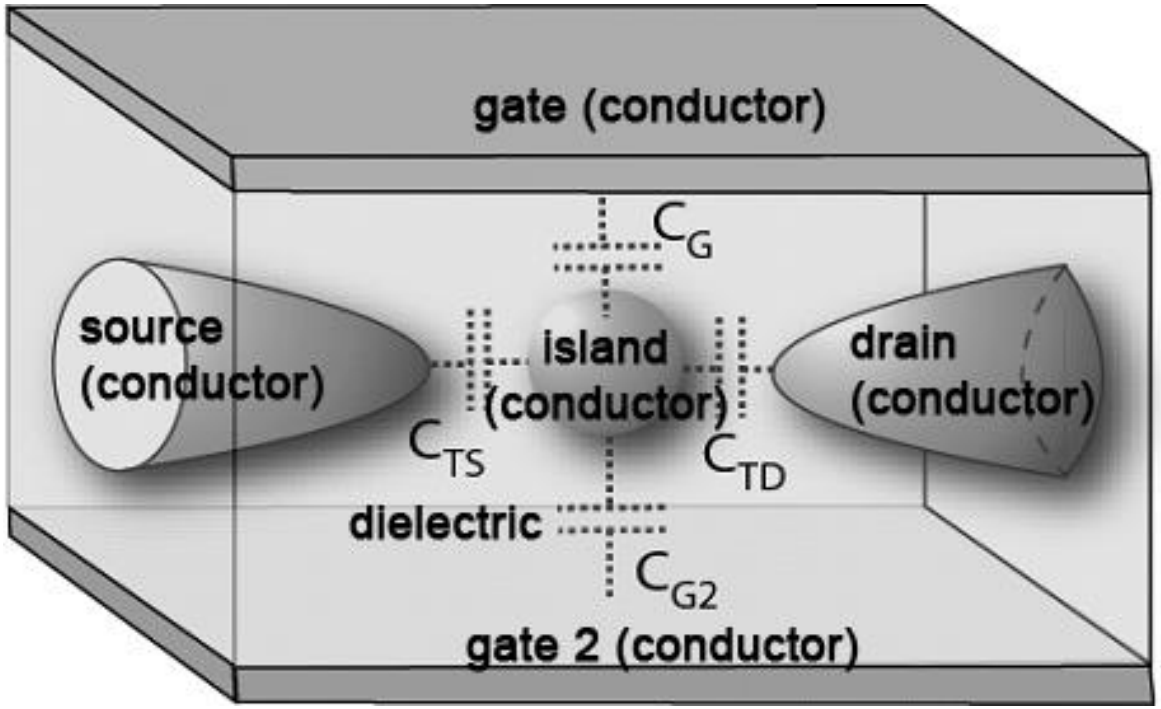
- Q1: What type of nanotechnology should to use for the fabrication of SETs?

- Q2: Which tools and materials?

Two solutions:

1. Top-down fabrication of SETs: metal and silicon SETs.
2. Bottom-up fabrication of SETs.

Single-island Single Electron Transistor

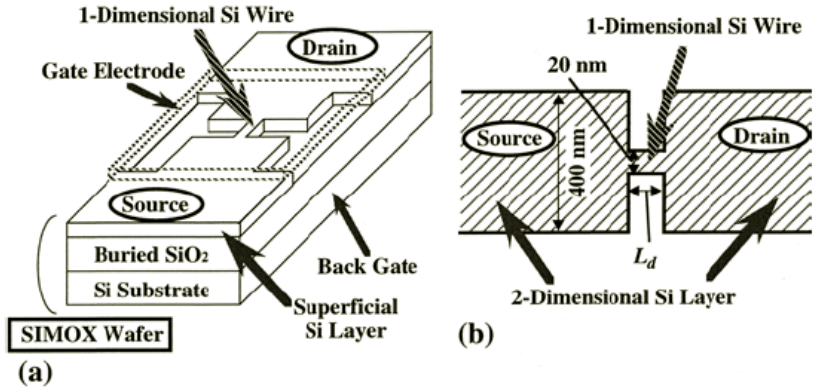


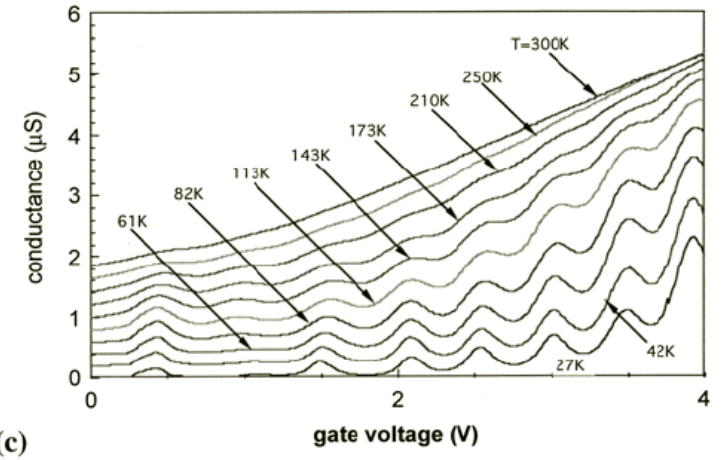
- Materials: conductive island and S, D, G, separated by thin insulating layers.
- Dimensions?
  - < 10nm island
  - ~few nm tunnel oxides.

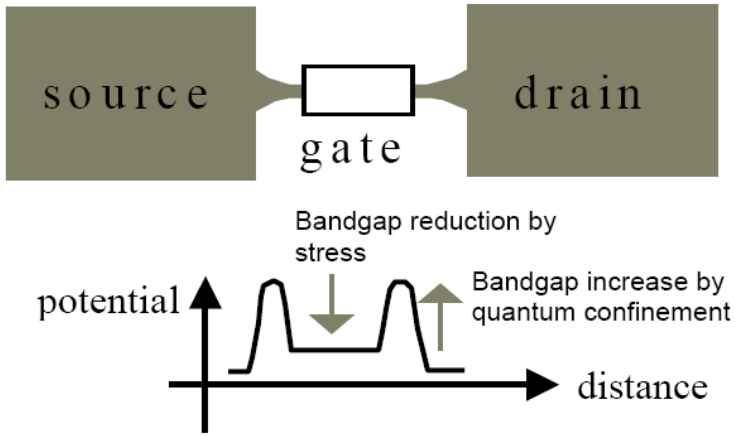
Single-island Single Electron Transistor

PADOX

- NTT research laboratory introduced **PADOX (PAttern Dependent OXidation)** techniques for fabricating SET devices on SOI.
- The process is based on the **thermal oxidation** of a short silicon wire, whose two ends are connected to wide Si layers: building-up stress induces equivalent tunnel junctions!
- Thermal oxidation of silicon is one of the most stable and controlled processes in CMOS technology, PADOX also appears to be a very reliable technology for CMOS-SET co-fabrication.

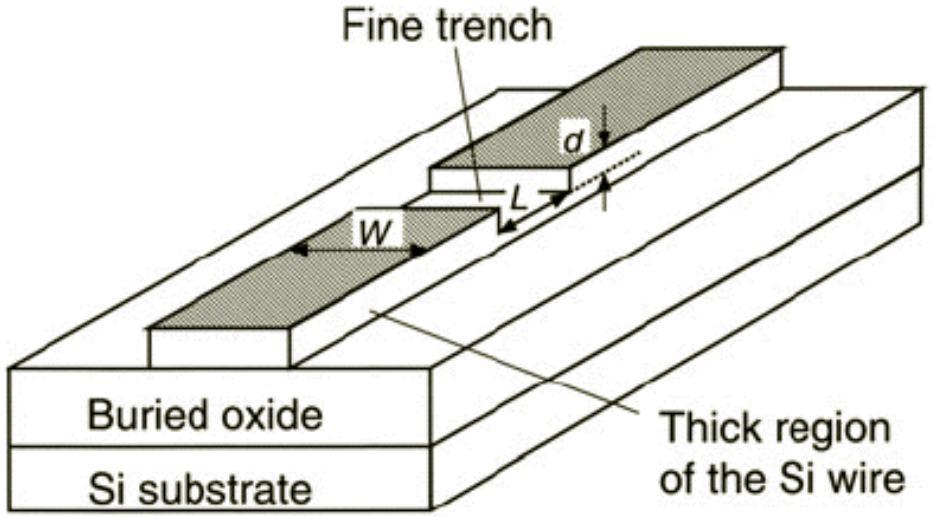






PADOX & V(ertical) PADOX techniques

Trench technique for twin island fabrication by thermal oxidation



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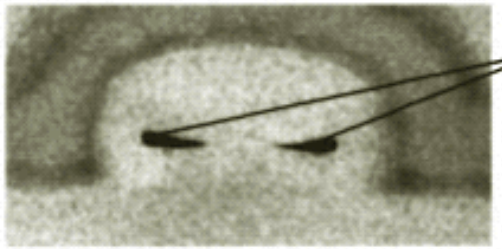
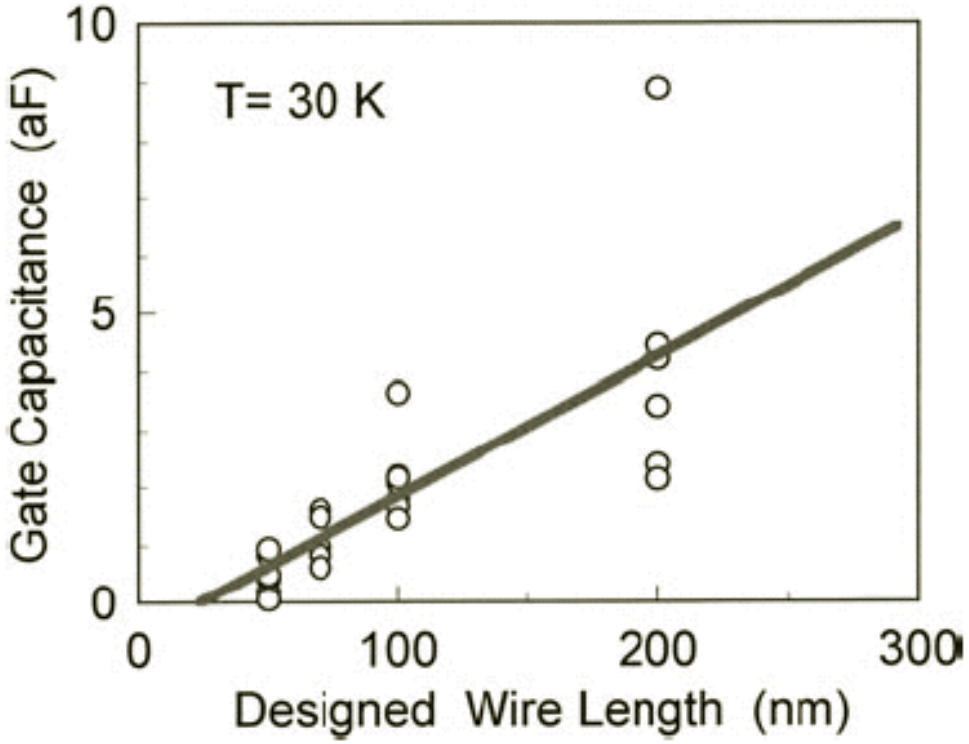


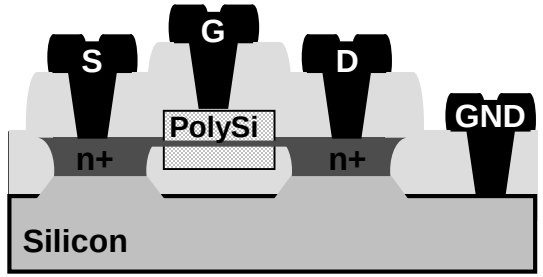
(b)

Realisation of aF capacitances: Operation @ ~30K

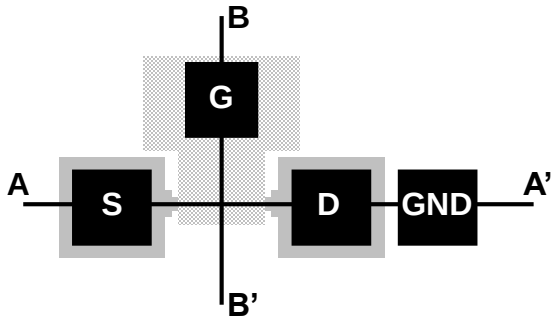


Top-down fabrication of Gate-All-Around Nanowire Single Electron Transistor

- Different channel cross-section shapes and dimensions can obtained with the same process: pentagonal, triangular and circular.
- Technology characteristics: no SOI and no e-beam litho.

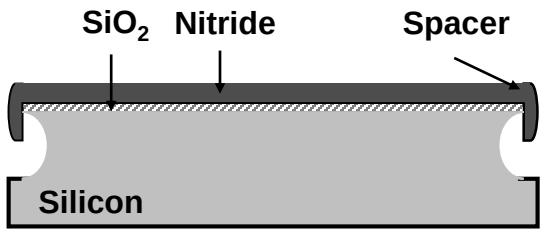


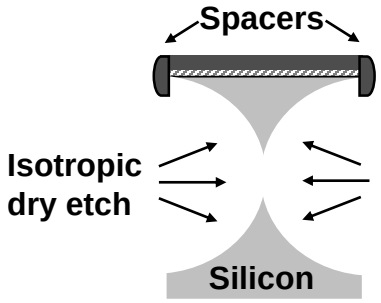
AA' lateral cross section



BB' channel cross section

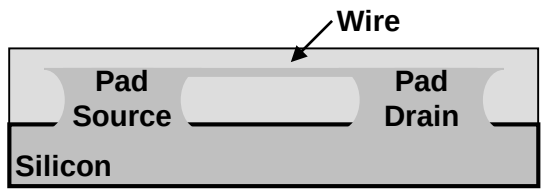
0. 4" Si wafer {100}
Boron p=10^{15}cm^{-3}

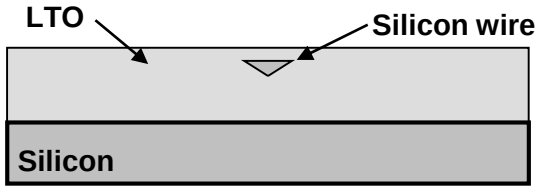


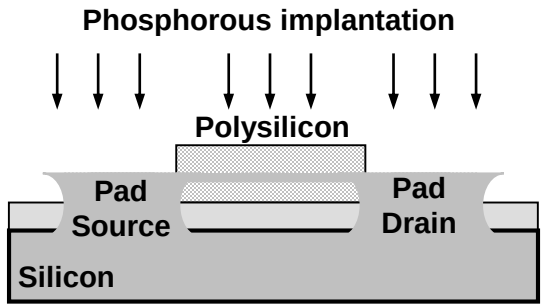


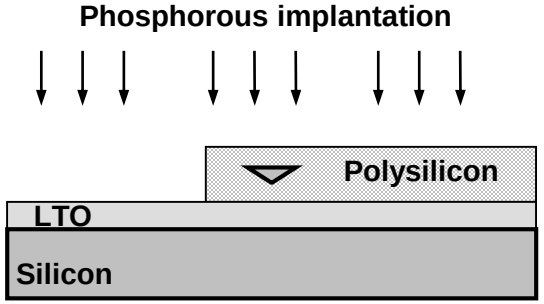
1. 25nm growth SiO_2
100nm LPCVD nitride
Lithography (optical)
Isotropic Si etch
Sacrificial oxidation

Top-down fabrication of Gate-All-Around Nanowire Single Electron Transistor



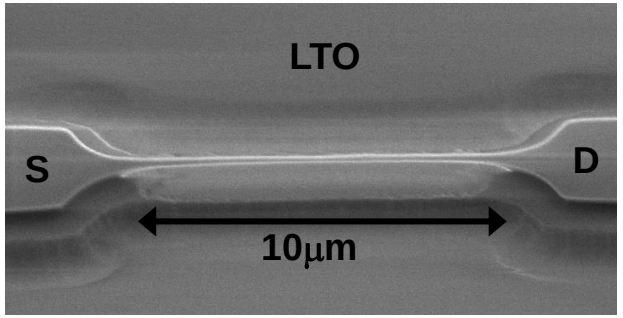






2. **Wire release (BHF)**
   LTO deposition
   Planarization
   Wire release

3. **Gate oxidation (20nm)**
   Polysilicon deposition
   Gate lithography + etch
   Implant + anneal



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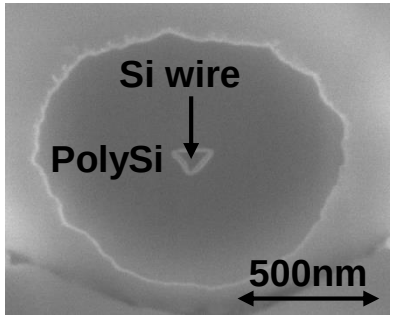
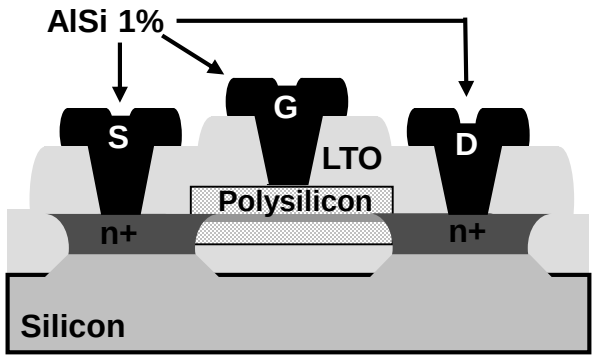


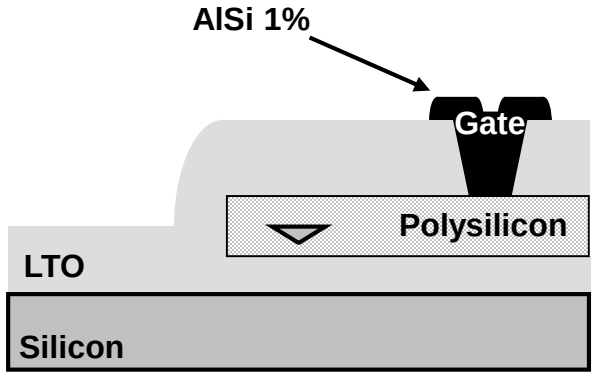
(b)

(a) **Released Si wire**

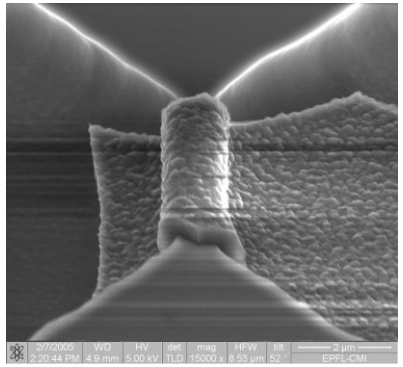
(b) **Triangulair Si wire surrounded by 500nm PolySi**

Top-down fabrication of Gate-All-Around Nanowire Single Electron Transistor

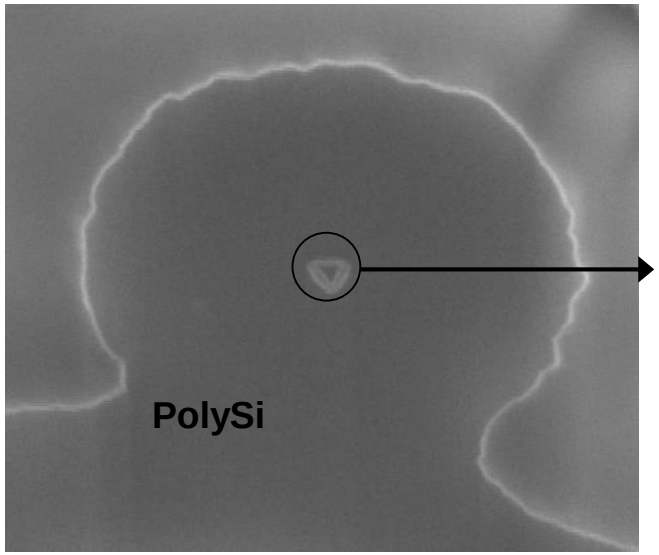


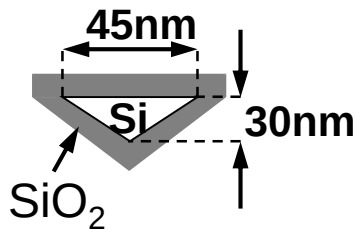


4. LTO passivation
   Contacts opening
   Metal sputtering + etch
   PMA



GAA polysilicon structure after etching

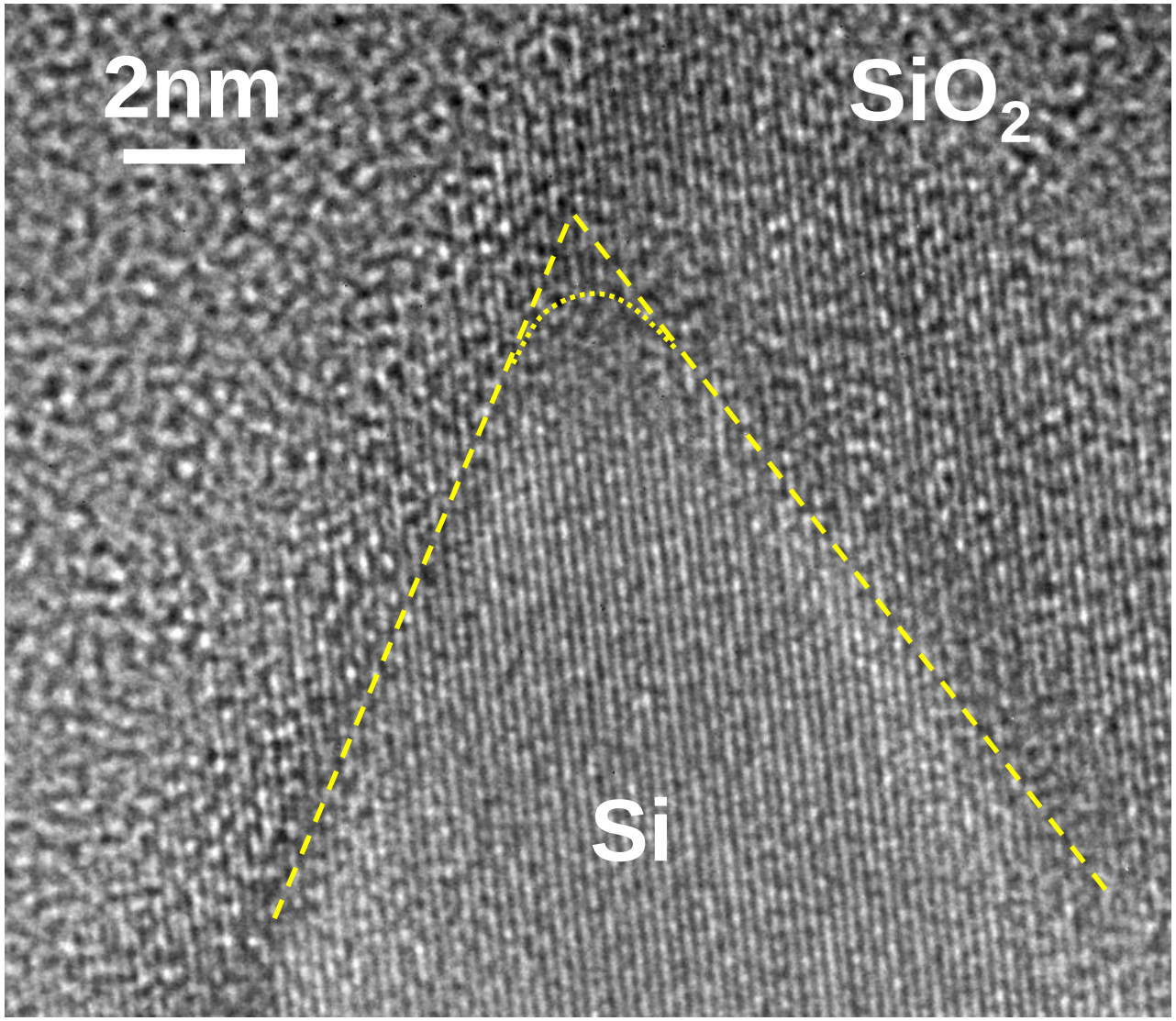




FIB cross section of a triangular wire. T_{ox} is 20nm.

V. Pott et al, Proc. of ESSDERC, pp. 427-430, 2006.

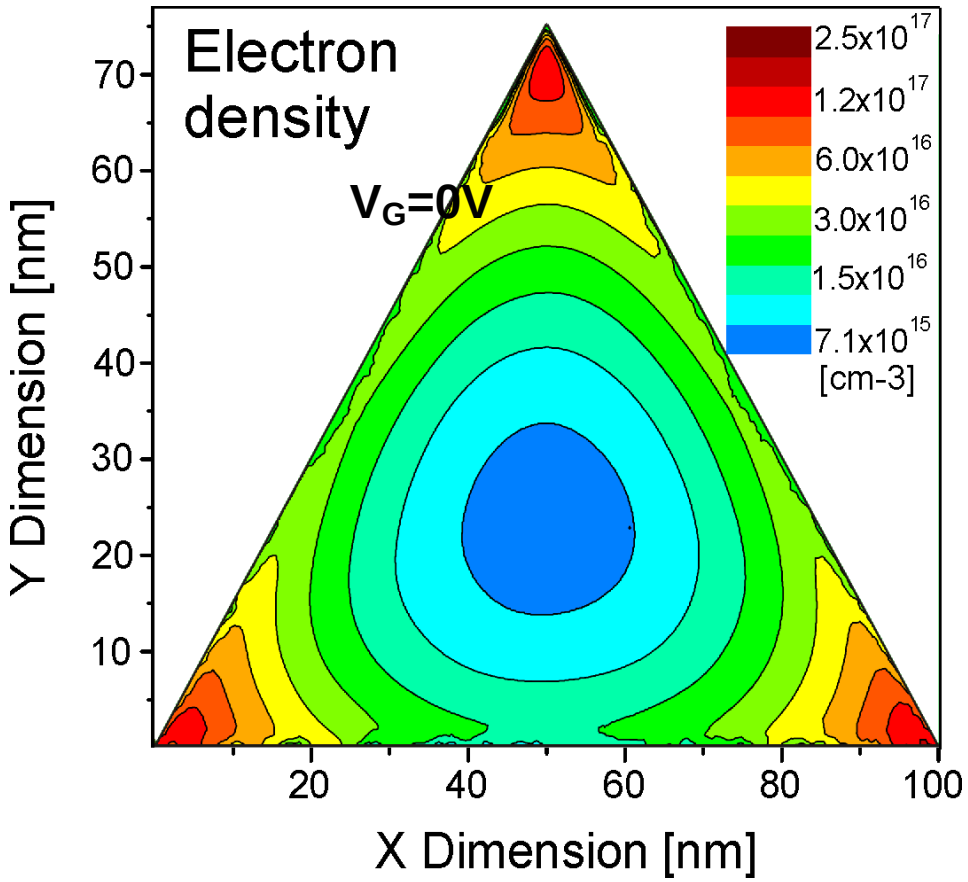
TEM: 1-2nm corner radius



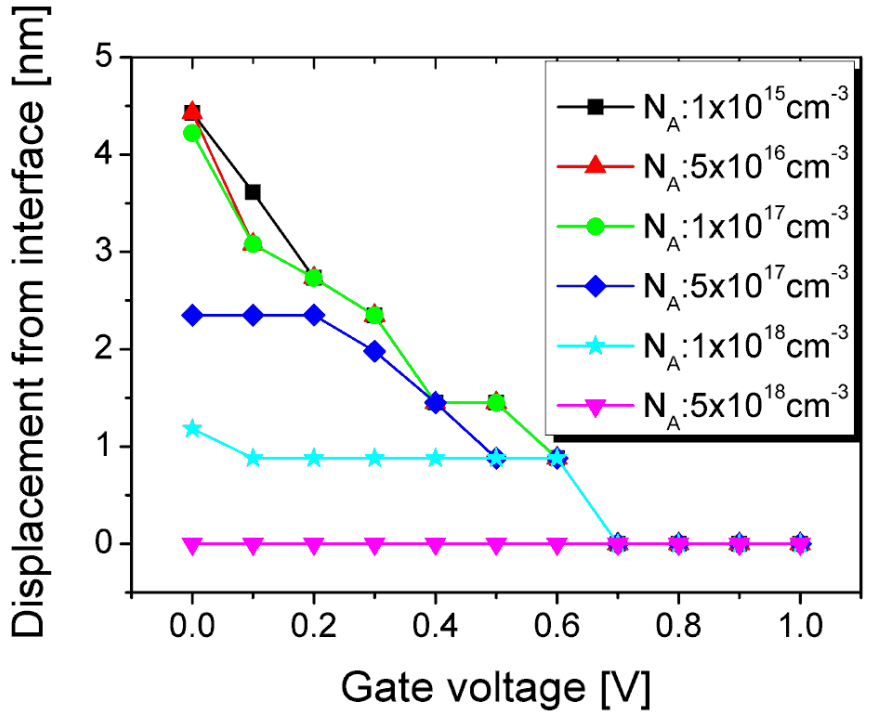
Corner radius: 1 - 2nm

Local volume inversion in GAA NW

Simulation

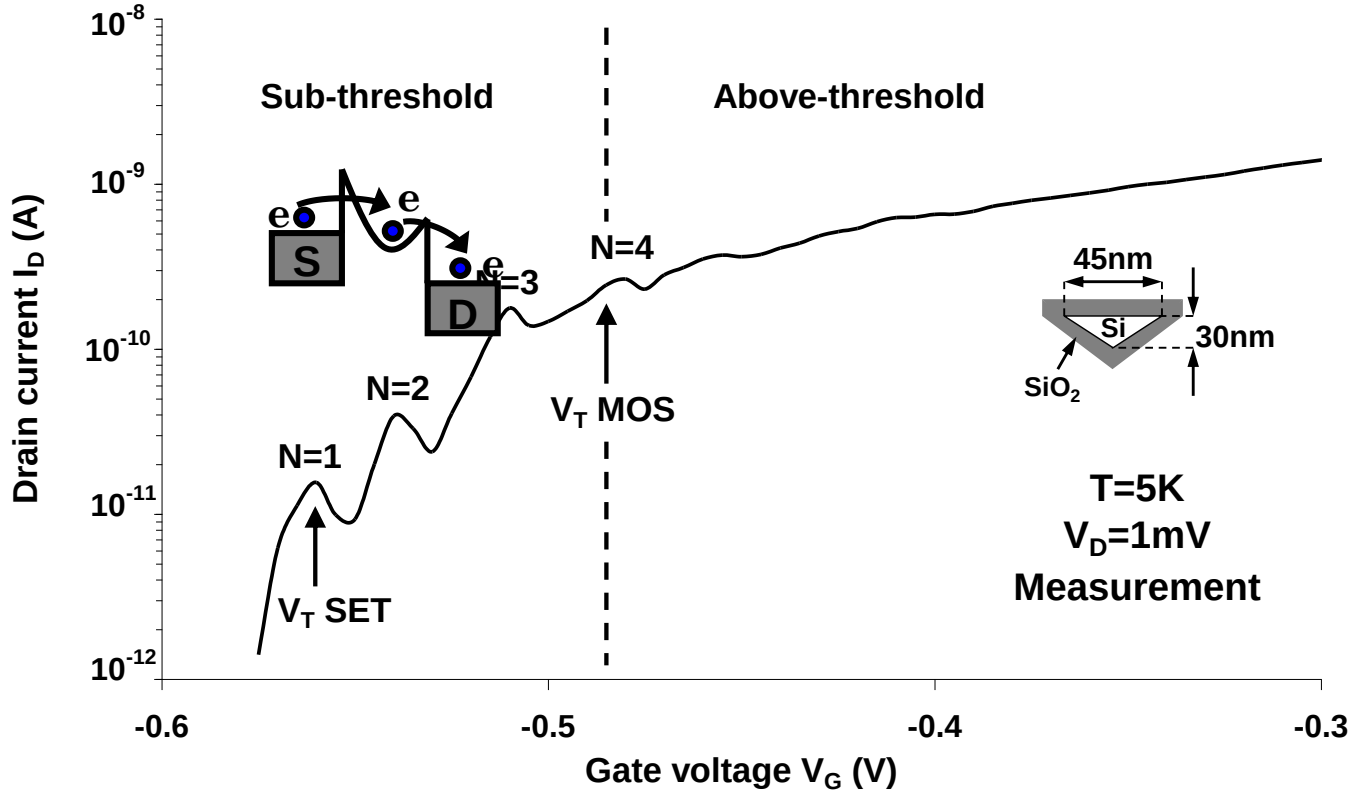


Channel doping:	p-type $10^{17}cm^{-3}$
Gate doping:	n-type $10^{19}cm^{-3}$
Threshold voltage:	0V
Gate oxide thickness:	12nm



- Displacement of a few nm away from Si/SiO_2 interface.
- Important for low channel doping densities ($<5 \cdot 10^{17}cm^{-3}$).
- Displacement decreases with increasing V_G.

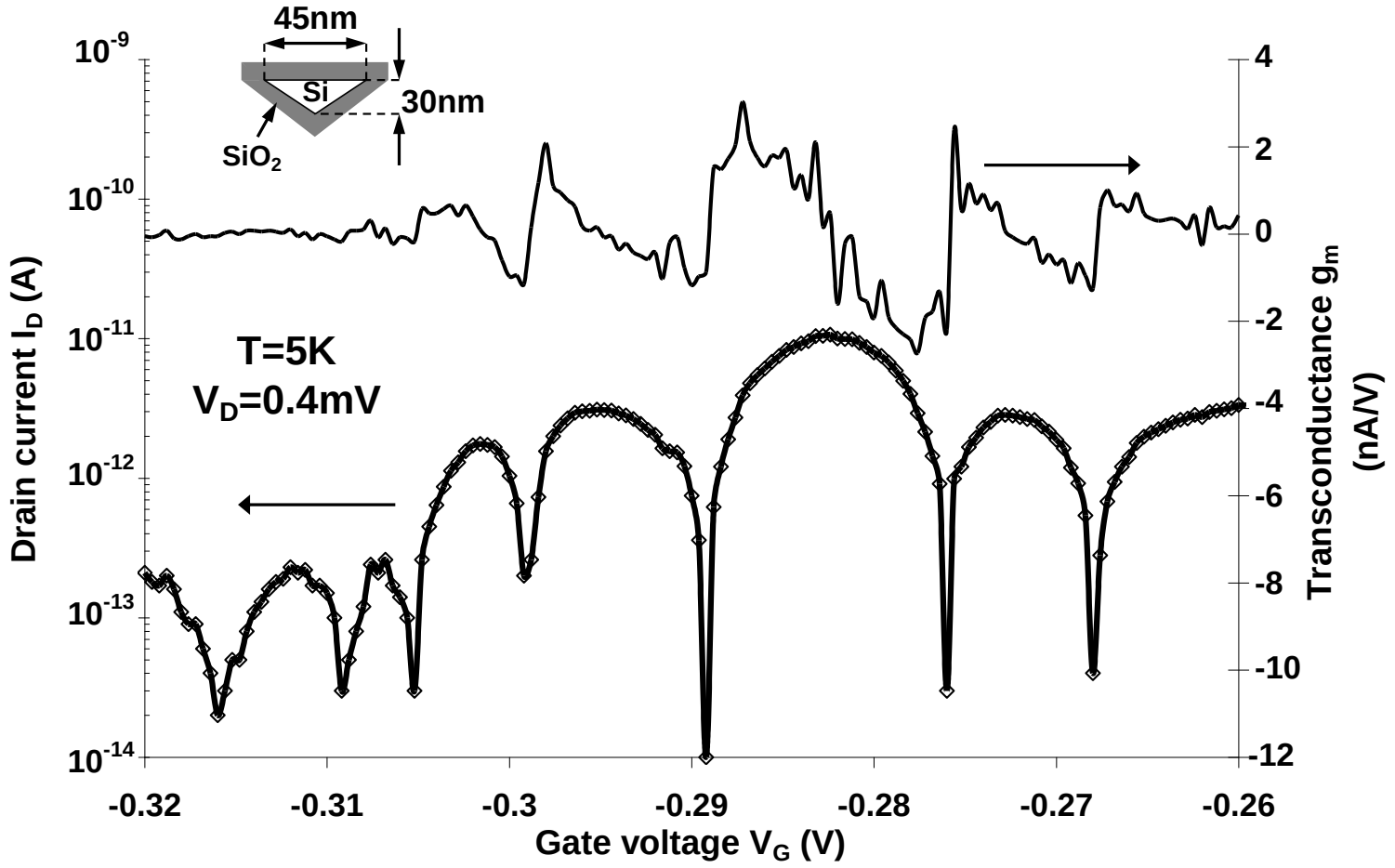
GAA NW SET cryogenic measurement



W_{equiv} = 120nm
L = 1μm
T_{ox} = 20nm
T = 5K

SET oscillations in small devices and at low temperature (<20K)
Depletion to weak inversion: with oscillations
MOS above-threshold: no oscillations

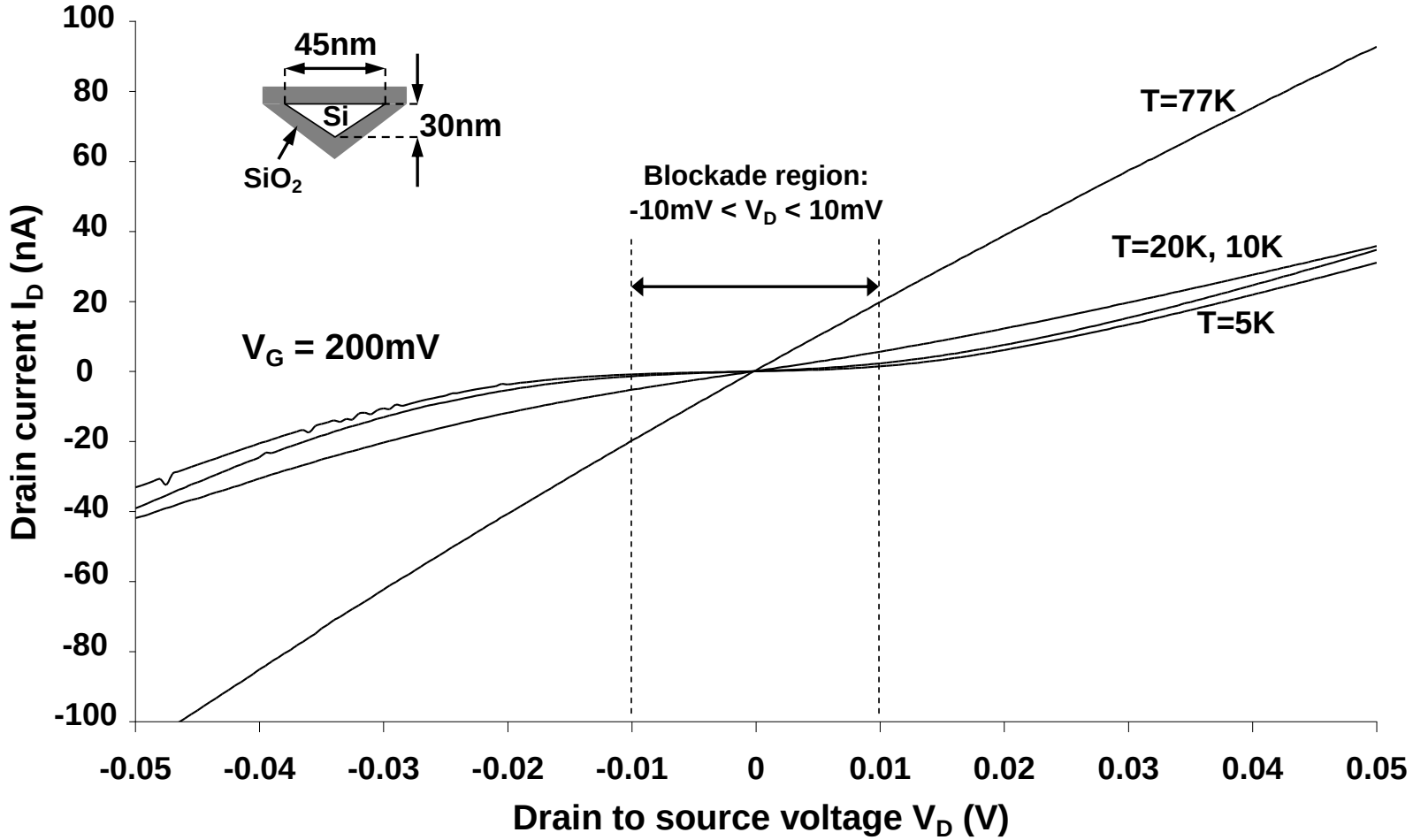
Coulomb oscillations in GAA NW SET



W_{equiv} = 120nm
L = 600nm
T_{ox} = 20nm
T = 5K

7 oscillations observed in weak inversion
I_D peak = 10 pA
CB period ΔV_G = 20mV (Power FFT)
Extracted SET gate capacitance $C_G=e/V_G$=8aF

Coulomb gap in GAA NW SET

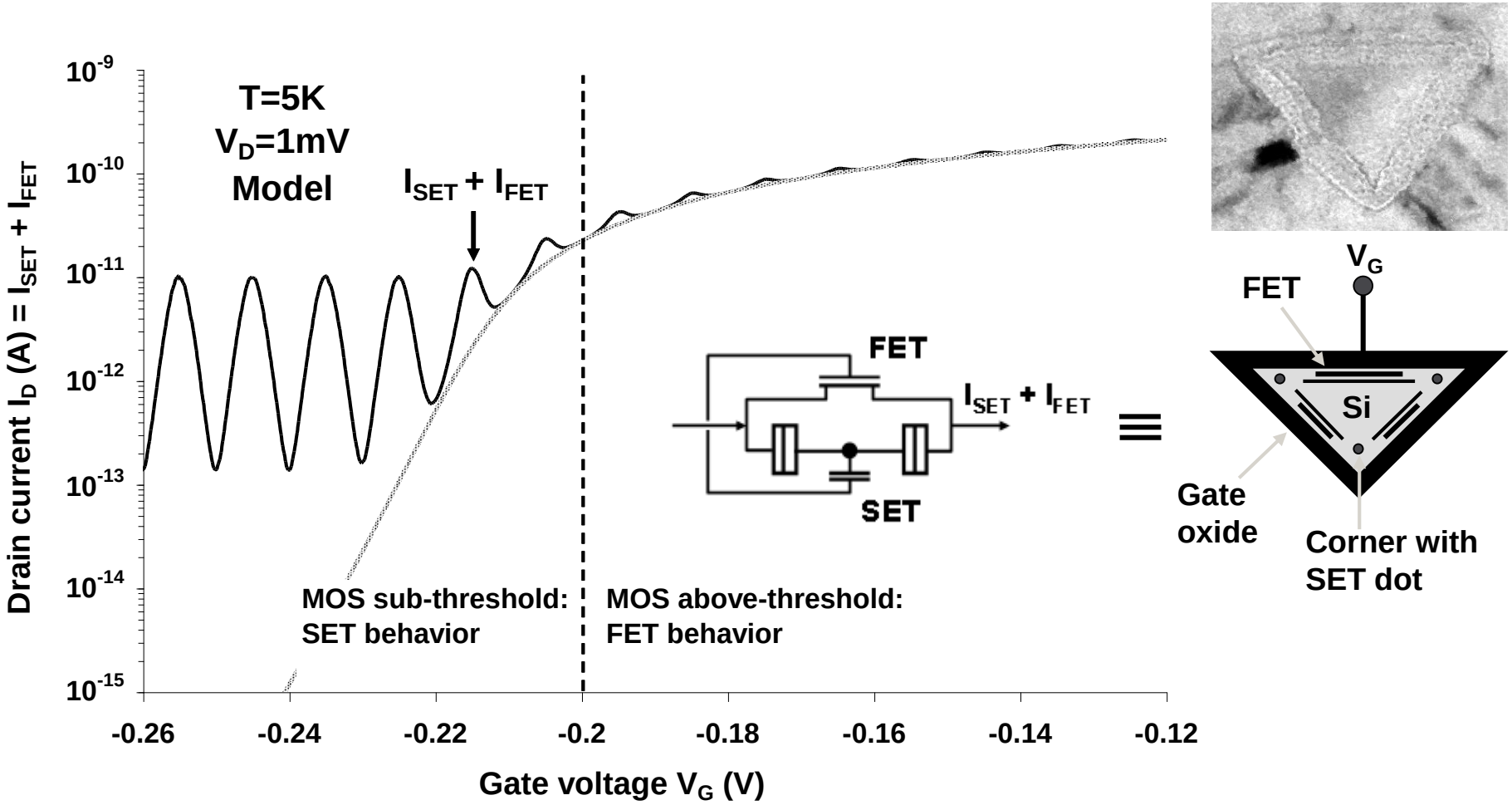


Silicon nanowire biased in weak inversion

Coulomb gap of 20mV centered at V_D=0

Linear characteristics (no Coulomb Gap) at T=77K

Macro-modeling

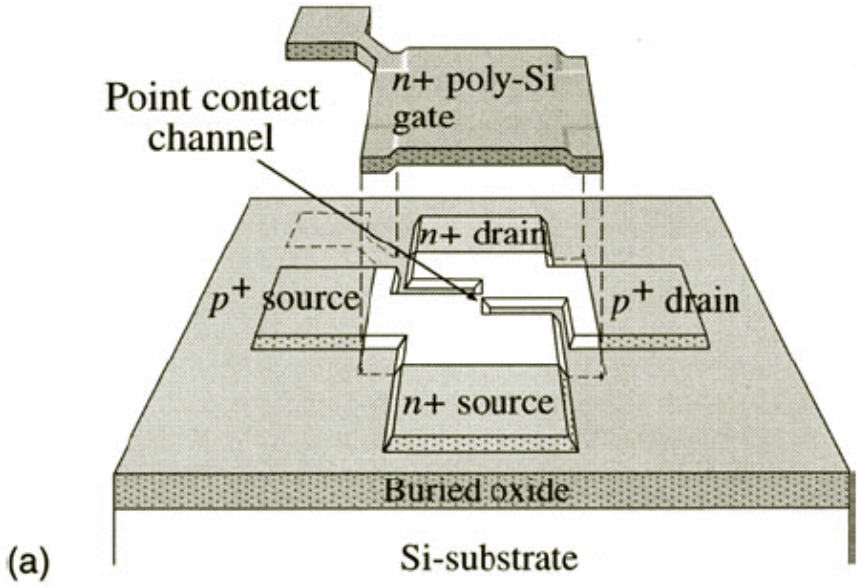


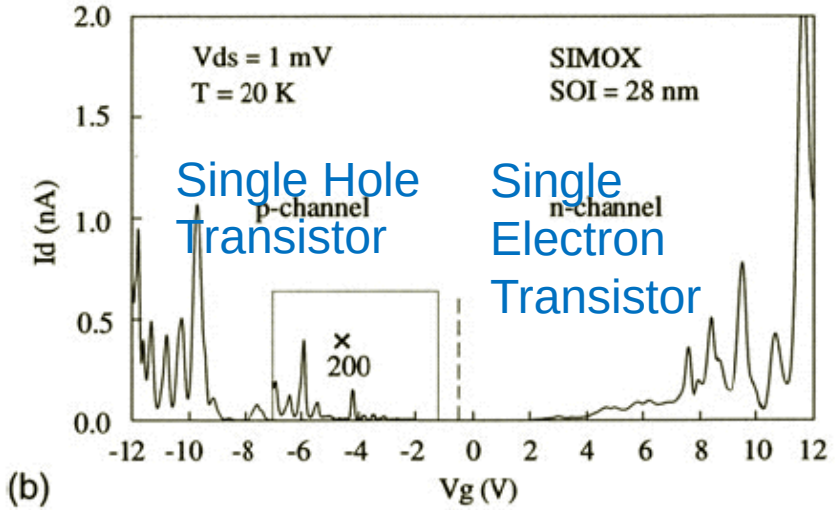
I_D-V_G simulation based on $I_{NANOWIRE}$=I_{SET}+I_{FET}

SET: based on orthodox theory (MC simulator) → A. M. Ionescu et al, *EDL*, vol. 25, iss. 6, pp. 411-413, 2004.

FET: based on EKV modeling → J. M. Sallese et al, *Sol. St. Elec.*, vol. 47, pp. 677-683, 2002.

Single Island SET: point contact transistor





- very narrow point contact MOSFETs are fabricated on SOI wafer using electron beam lithography and anisotropy etching technique. The width of the constricted point contact channel is less than 30 nm.

- When the positive bias is applied to the gate, the electrons are induced in the channel and device operates as normal SET. In contrast, when a negative bias applied, the device acts as a SHT (Single Hole Transistor).

Motivation for hybrid SET-CMOS

CMOS and SET and highly complementary as functionality and performance: **co-design can offer added value for new applications**.

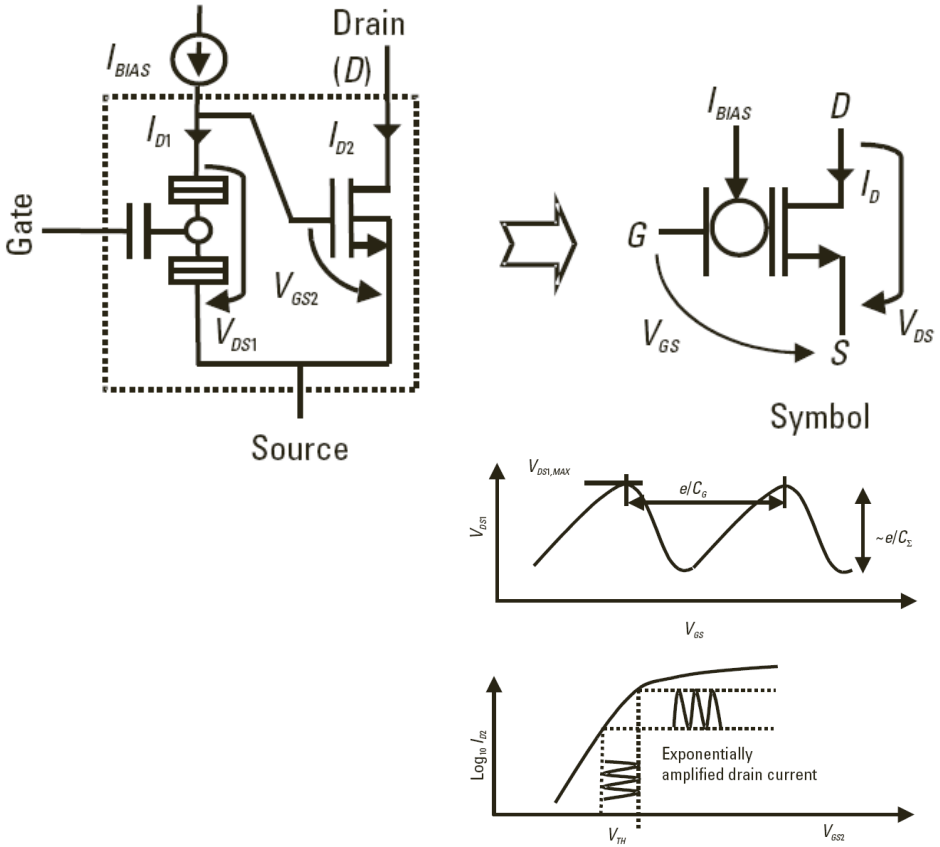
Comparison Between Advantages and Limitations of SET and CMOS Technologies

	SET	CMOS
Advantages	Nanoscale feature size	High gain and current drive
	Unique Coulomb blockade oscillation characteristics	High speed
	Ultralow power dissipation	Very matured fabrication technology
Limitations	Low current drive	Sub-10-nm physical limits
	Lack of room temperature operable technology	Power density
	Background charge effect	

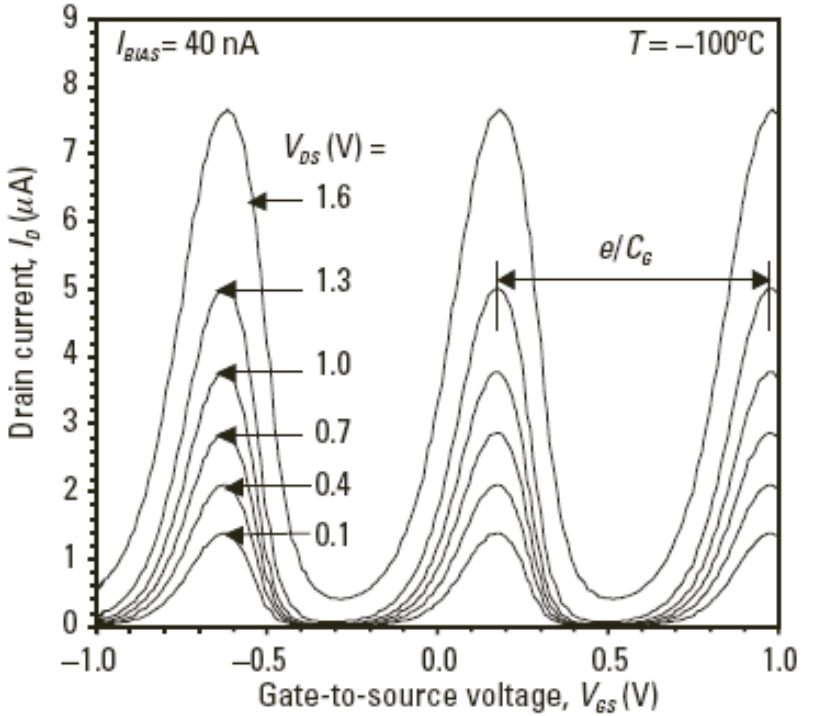
Example of hybrid CMOS-SET circuit

SETMOS: How does it work? We amplify the oscillations of a constant current biased SET by a MOSFET (co-integration is required):

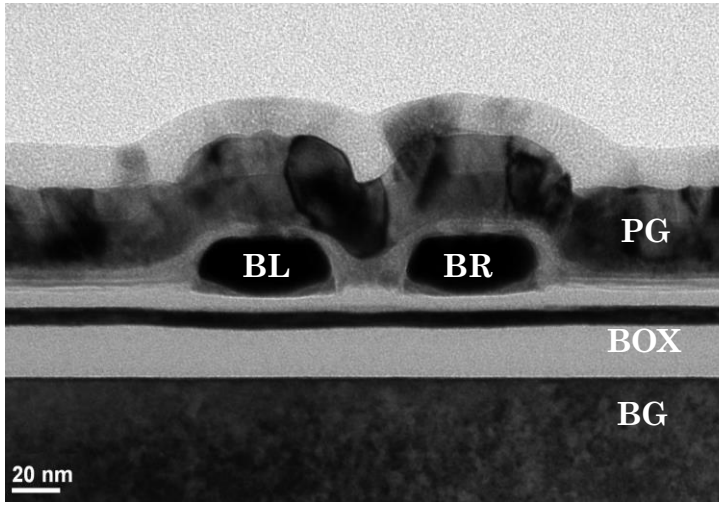
- period dictateed by the SET
- current peaks dictated by the MOSFET amplification
- Hybrid operation principle

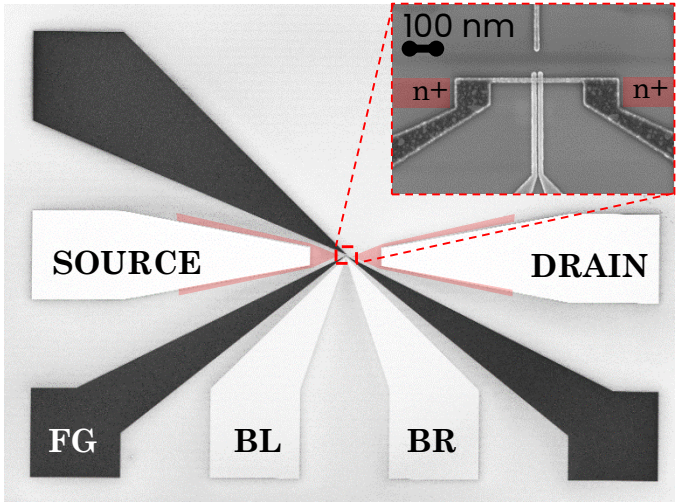


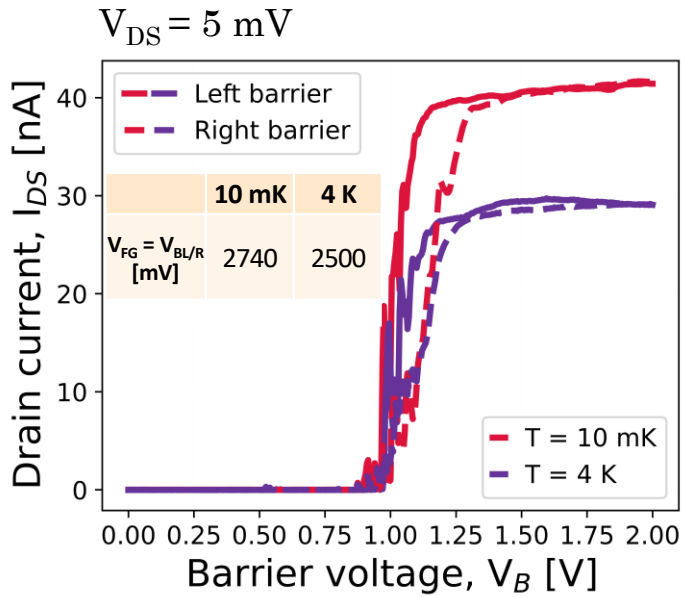
- Oscillations with peaks @ microAmp range enable new apps: (i) negative differential resistance Ics, (ii) oscillators, (iii) analog amplification @ very low current.
- Cryogenic operation is needed for the SET



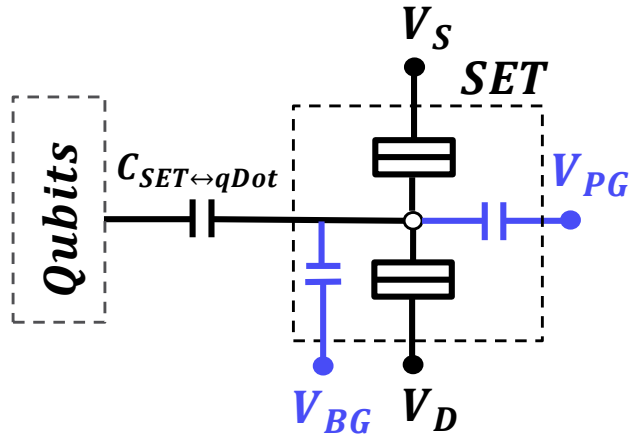
A solution for the SET-FET co-integration: Multi-Gate FD-SOI SET





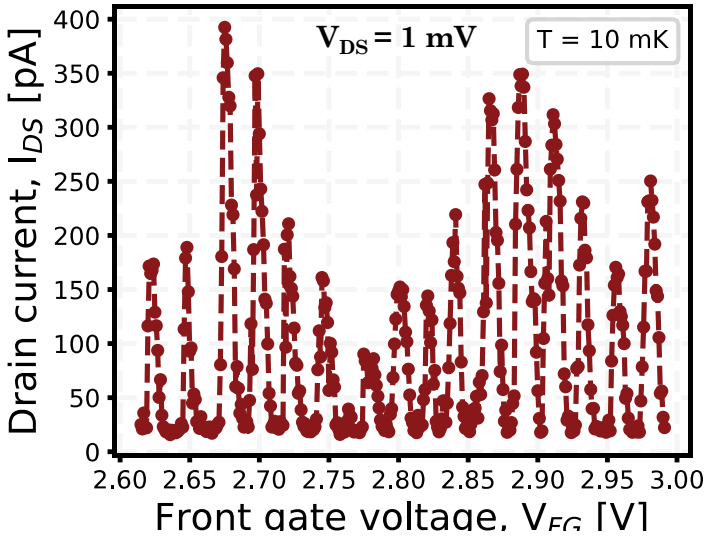


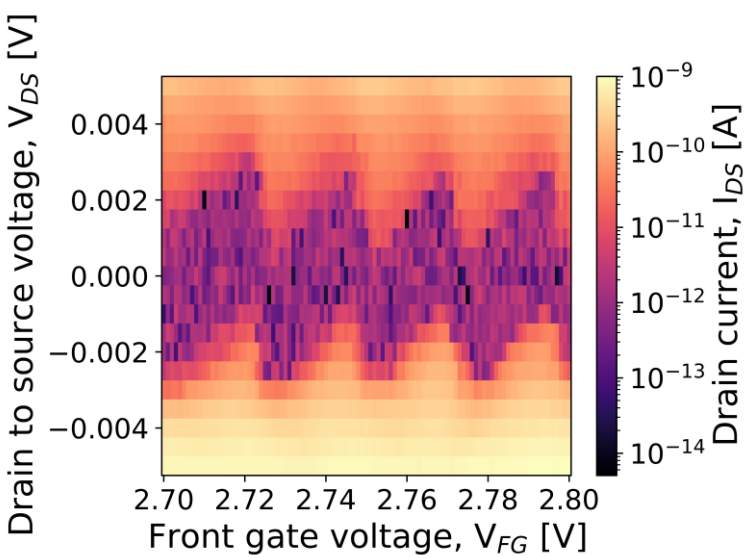
- Simple patterning of top-gates through lithography
- Complete vertical ***depletion*** through barrier gates
- ***Volume inversion***
- **Optimal candidate for hybrid CMOS/quantum circuits**
  - Low power consumption (FD-SOI)
  - Threshold tunability through ***back-gate bias***

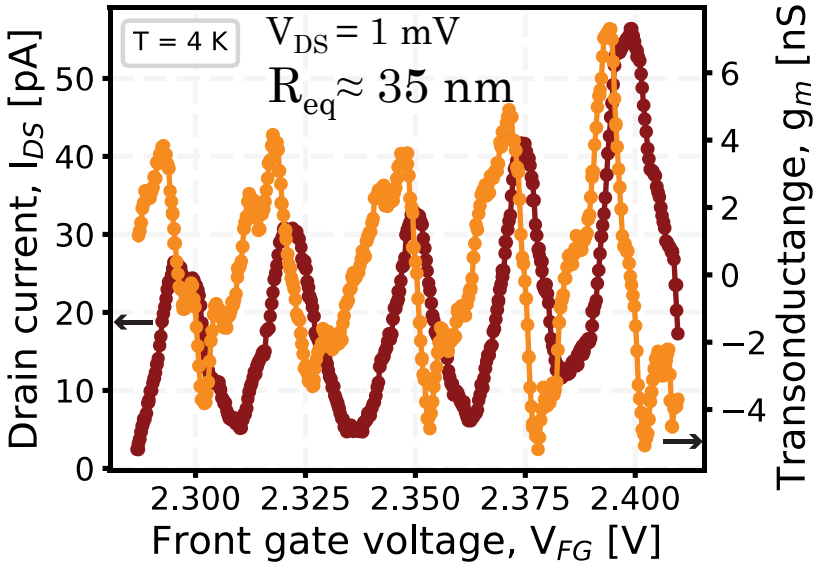


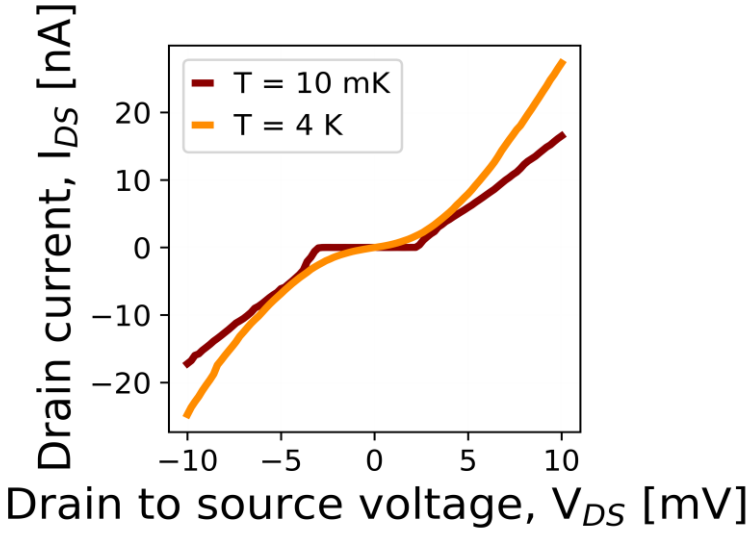
F. Bersano, ESSCIRC, 2022, pp. 49-52.

Multi-Gate FD-SOI SET/FET characteristics







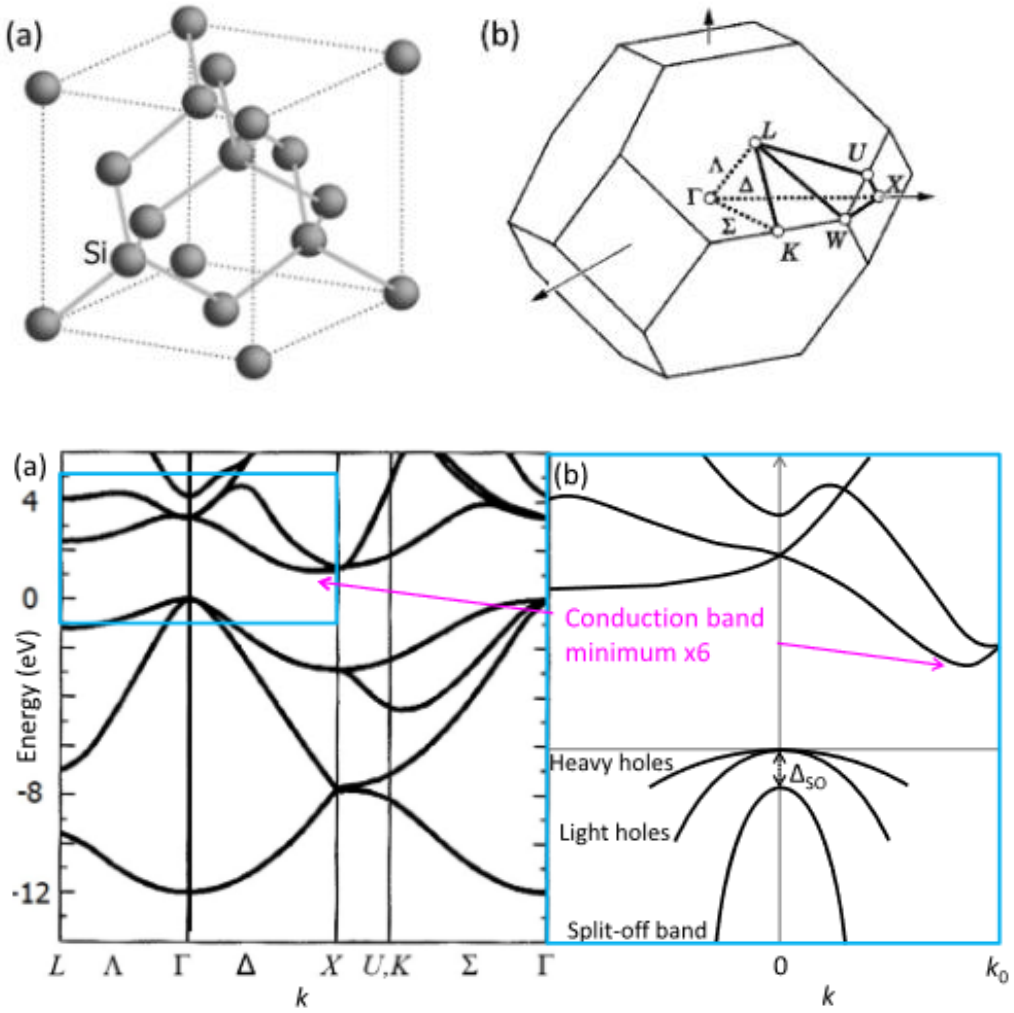


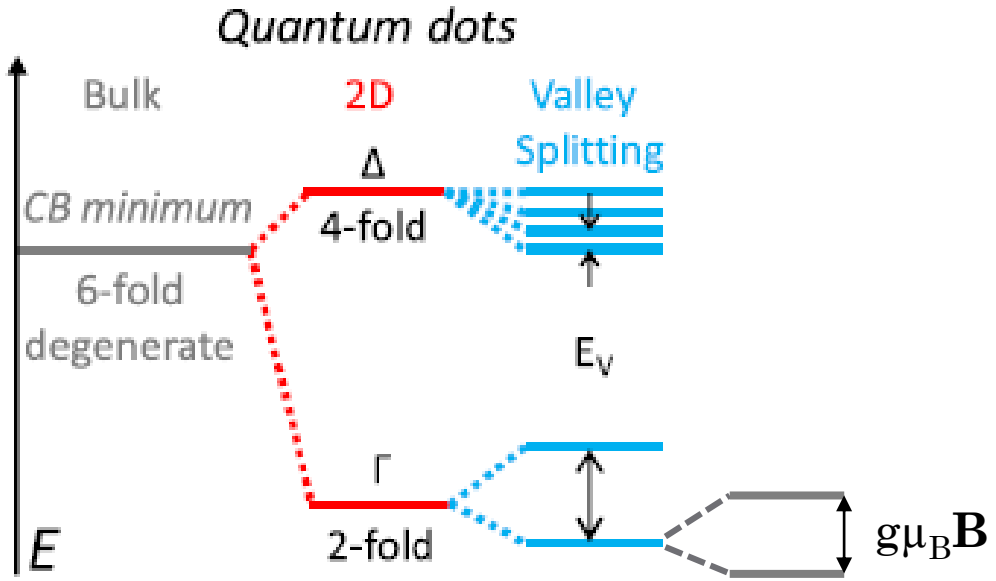
- ❑ Stable peaks with periodicity dictated by **gate capacitance** (dimensions of the dot and dielectric)
- ❑ Broader peaks at 4K compared to mK
- ❑ SOI enables the engineering of a **back-gate**

F. Bersano, ESSCIRC, 2022, pp. 49-52.

From Quantum Dots to Spin Qubits

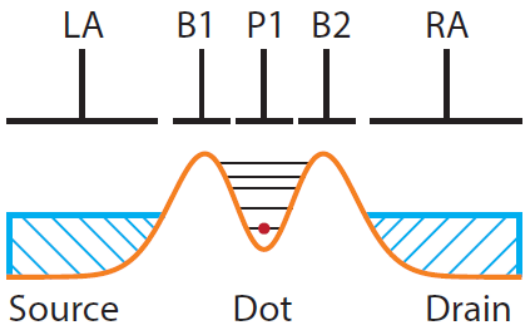
Let's take the example of Silicon.



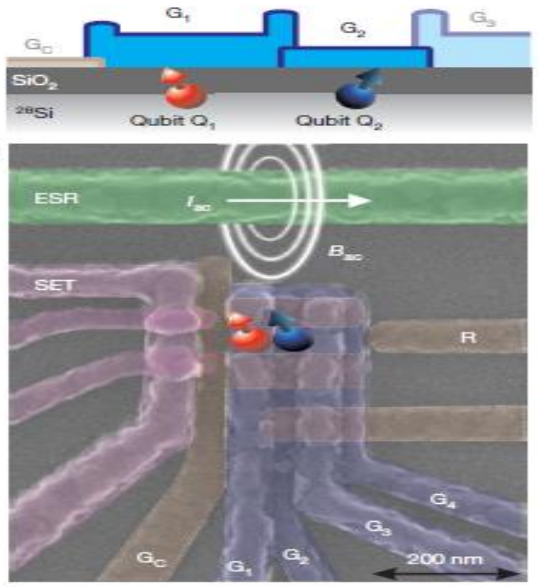


- Valleys degeneracy it split by quantum confinement
- Isolation of a 2 levels system given by quantum confinement and Zeeman splitting
- But can we use the same materials engineered for CMOS also for spin qubits architectures?

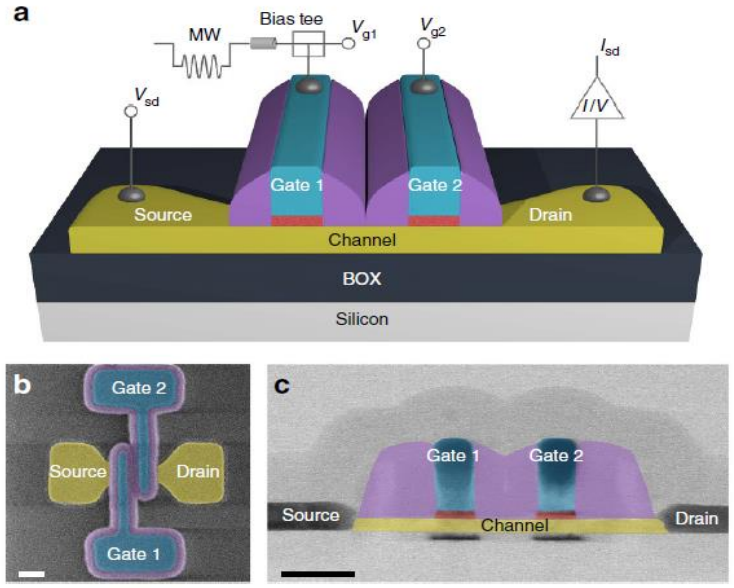
Example of spin qubit architectures



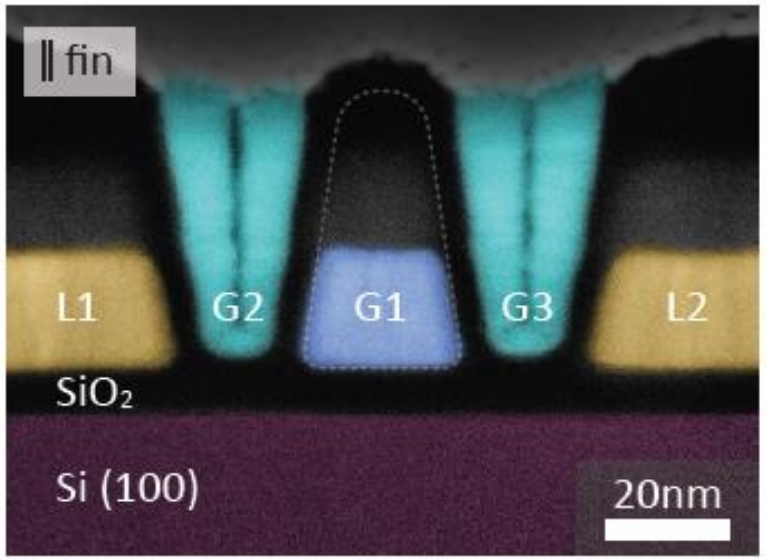
- Inspired by FET technologies
- Confinement along x,y,z given by electrical gates and semiconductor geometry (planar, finFET, nanowires…)
- Quality of interfaces and materials are very important for the coherence of the quantum state and the definition of a “clean” 2-levels system.
- Most of spin qubits architectures implement SETs, why?



Veldhorst et al., 2015



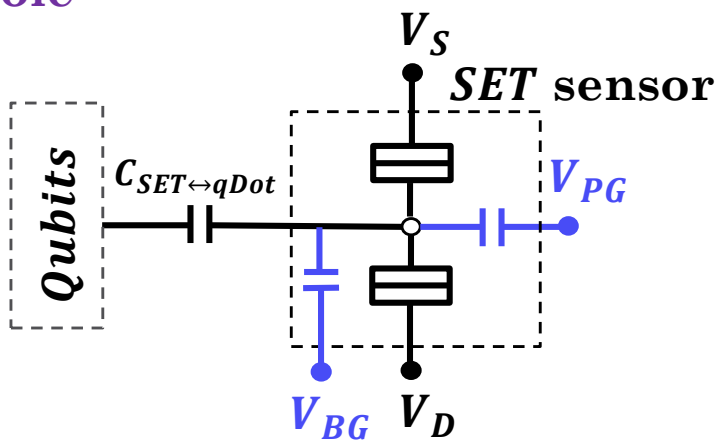
CEA LETI, 2016

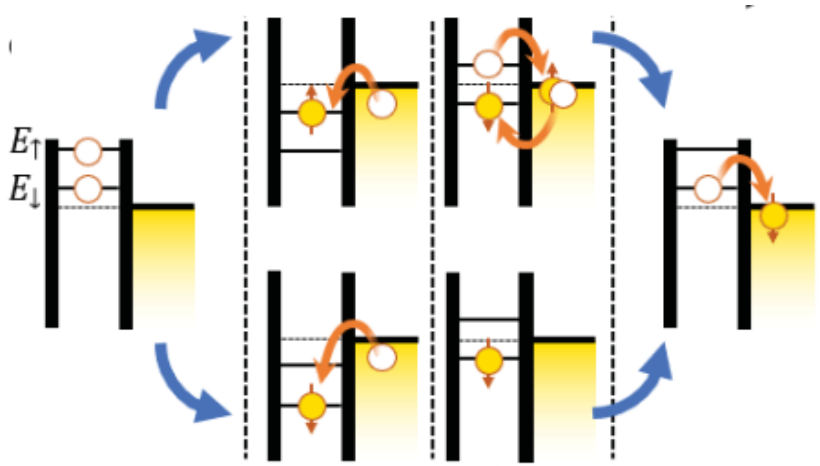


Geyer et.al, 2020

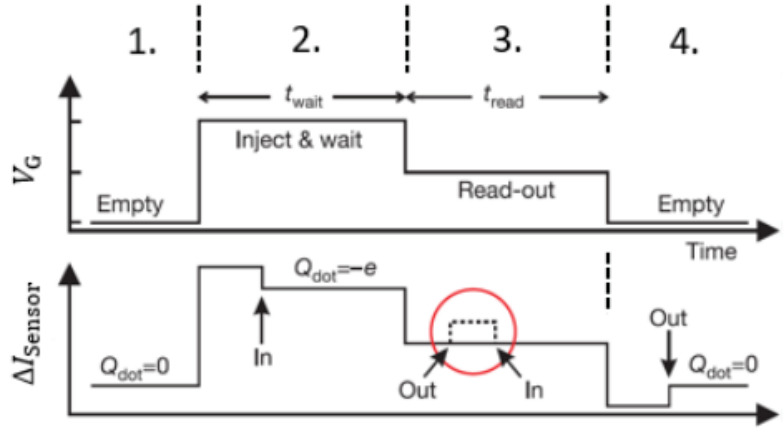
Qubits readout via an electron reservoir and SET capacitive coupling

Elzerman protocol : one of the simplest way to readout the spin state of an electron/hole



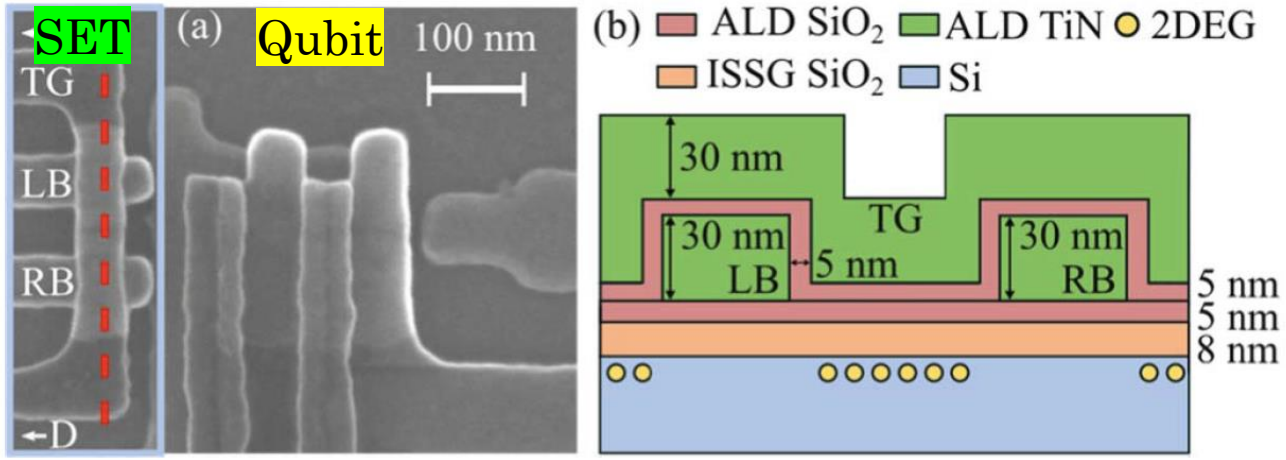


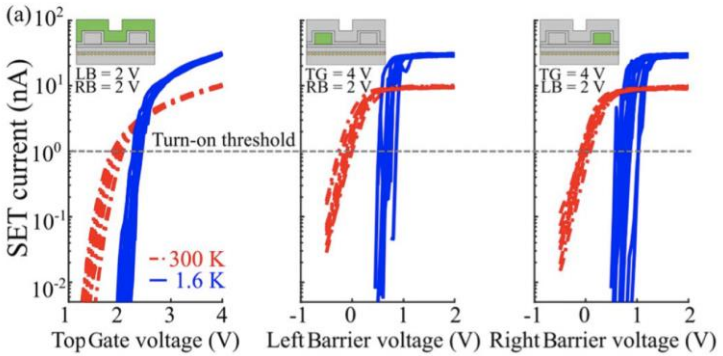
- Readout based on the detection of charge transport through a pair of quantum dots
- Single Electron Transistor is used as an "electrometer", very sensitive to charge fluctuations
- The same architecture is used for other readout protocols

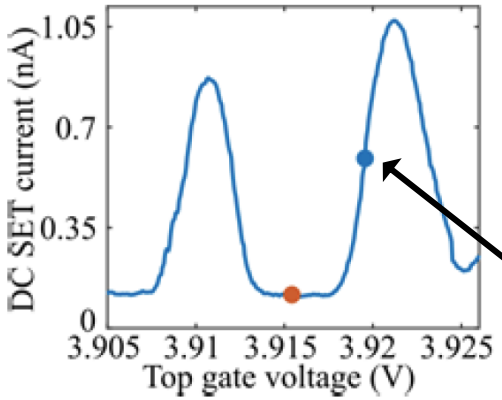


Michael Allan Fogarty. Spin-based quantum computing with silicon mos quantum dots. 2018.

SET for readout in Quantum Computing with spins





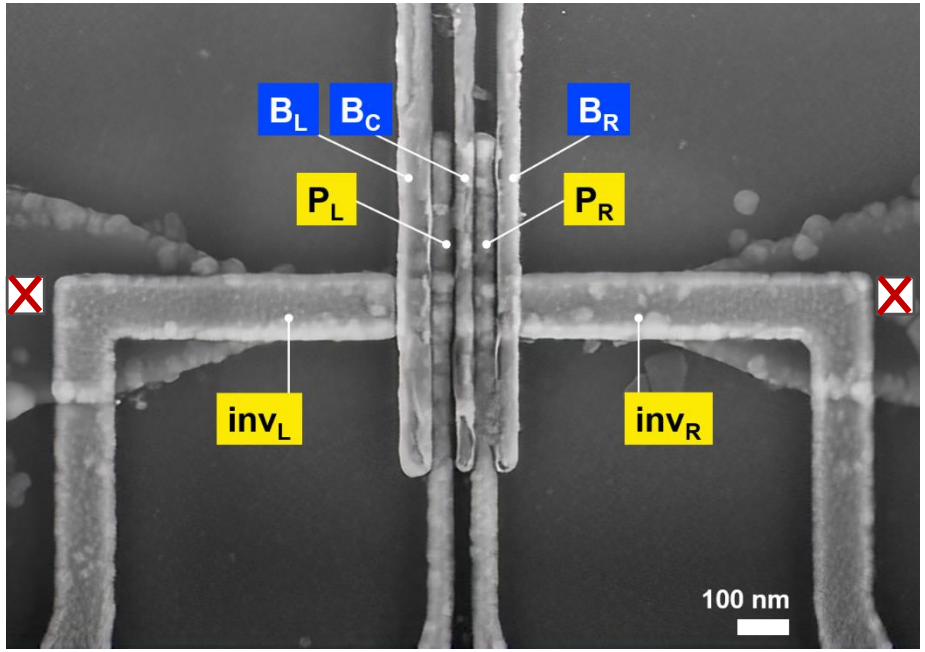


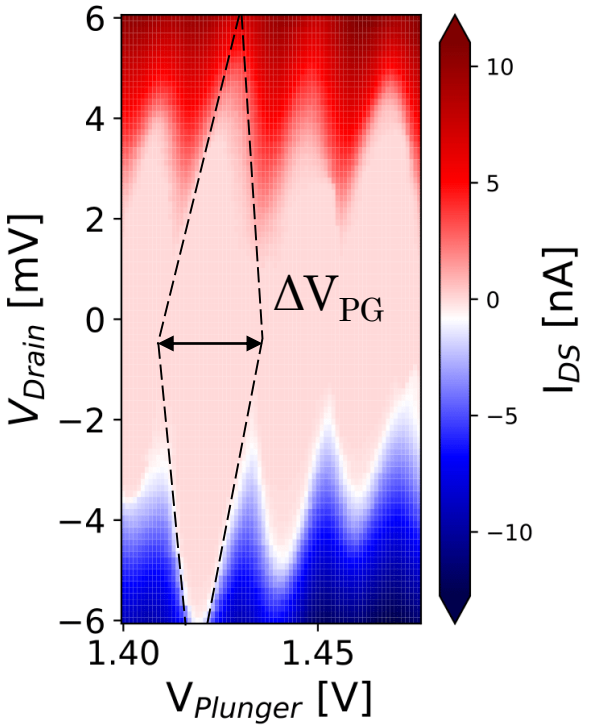
- Prototype spin qubit device in a 300 mm process, using state-of-the-art, CMOS-compatible process steps
- Dots with charging energies of 1-2 meV and sizes of around 46 nm
- Well-formed single-electron transistors with a feature size of 50 nm, individual electron controllability and show multi-gate control uniformity from room-down to low-temperature.
- SET used as a **charge sensor** to readout the state of spin qubits

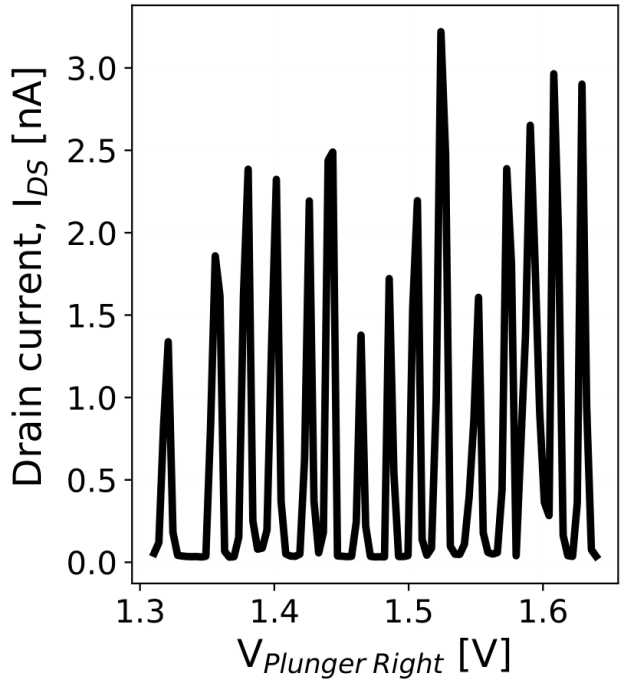
Maximum sensitivity is given for the optimal $\frac{\partial I_{SET}}{\partial V_G}$

Dumoulin et al, IEEE EDL, 2020.

Quantum dots on ultra-thin SOI nanowires for enhanced electron spin qubit control



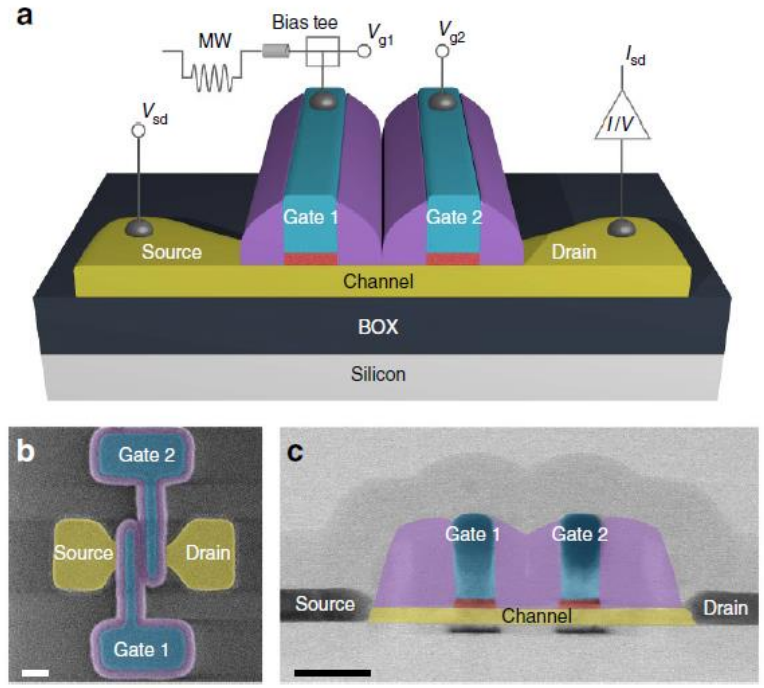




- Based on ***Coulomb blockade*** for electrons
- Same process flow as the SET adapted for spin qubit devices
- SOI nanowire to optimize quantum confinement in 2D

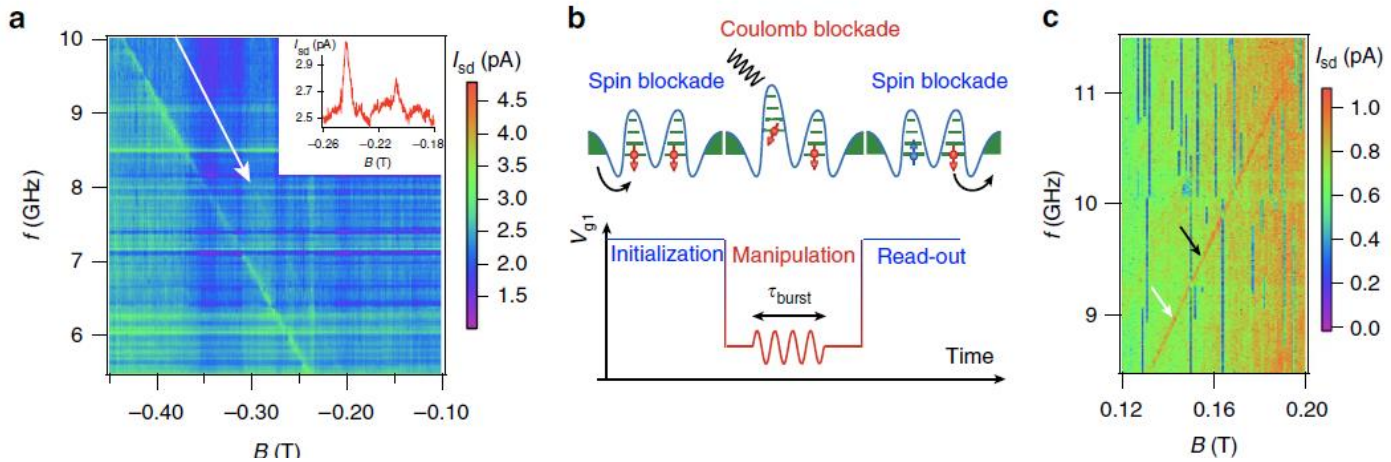
Bersano, F., et al., 2023, June. IEEE Symposium on VLSI Technology and Circuits (pp. 1-2).

A CMOS silicon spin qubit (with holes)



Electrically driven coherent spin manipulation.

a) 3D schematic of a silicon-on-insulator nanowire FET with two gates, gate 1 and gate 2. Using a bias tee, gate 1 is biased with a static gate voltage V_{g1} and to a 20 GHz-bandwidth line, used to apply the high-frequency modulation necessary for qubit initialization, manipulation and read-out. (b), (c) Colorized device views.

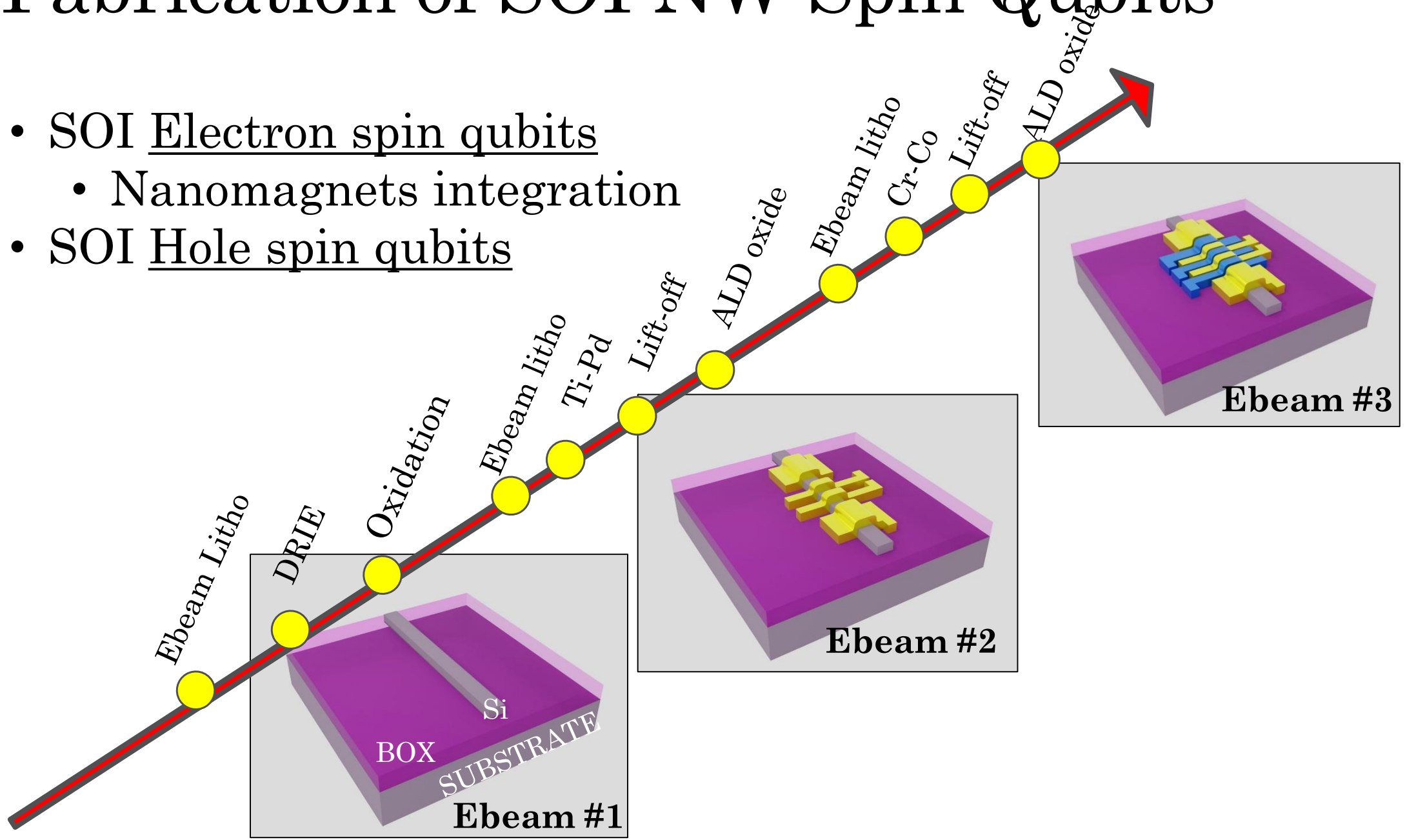


(a) Color plot of the source-drain current Isd as a function of magnetic field B and frequency. Electrically driven hole spin resonance is revealed by two enhanced current ridges. The barely visible upper ridge is indicated by a white arrow.

Maurand, R., et al. Nature communications 7.1 (2016)

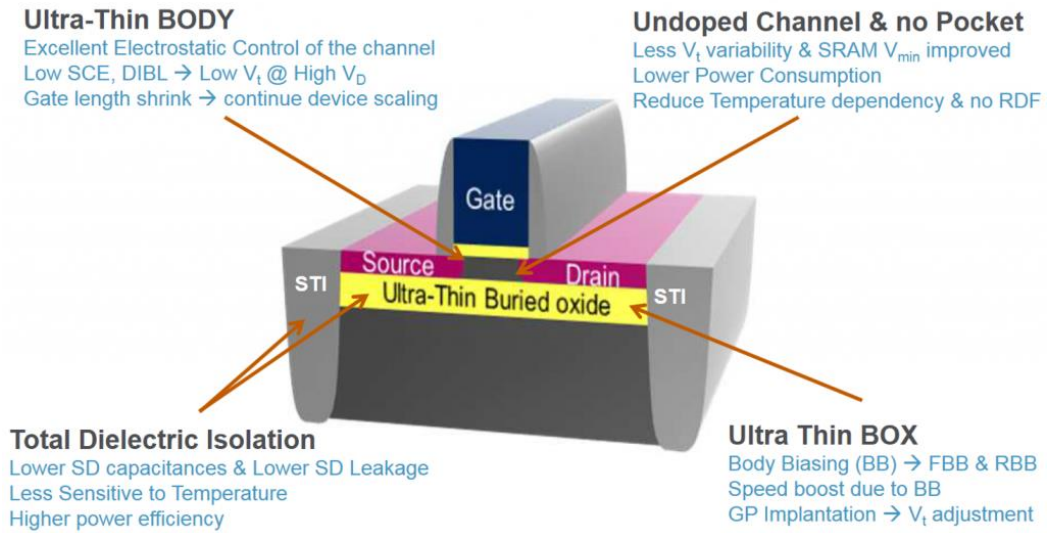
Fabrication of SOI NW Spin Qubits

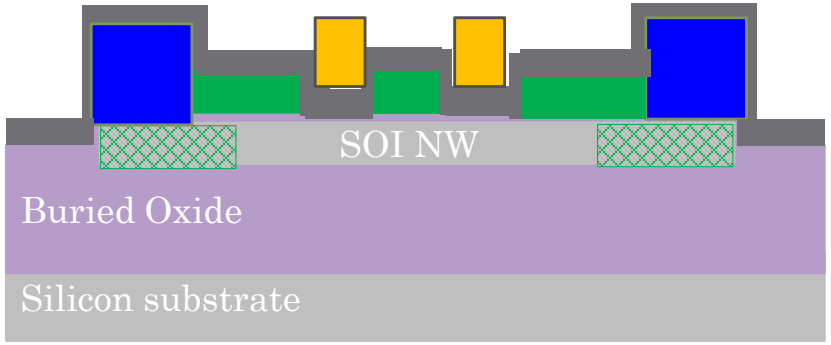
- SOI <u>Electron spin qubits</u>
  - Nanomagnets integration
- SOI <u>Hole spin qubits</u>



Fabrication of SOI NW Spin Qubits

FD SOI MOSFET





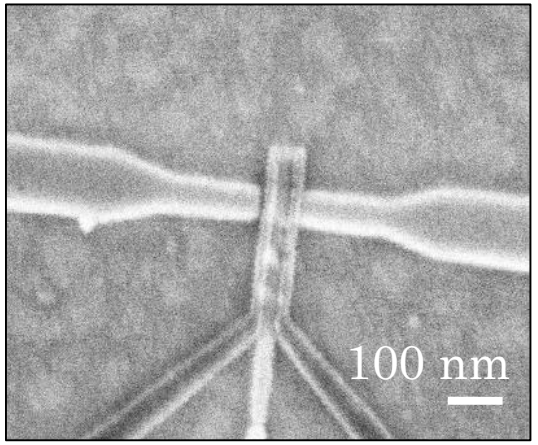
Ti/Pd: first metallization layer

Cr/Co: second metallization layer

Ti/Pt: third metallization layer

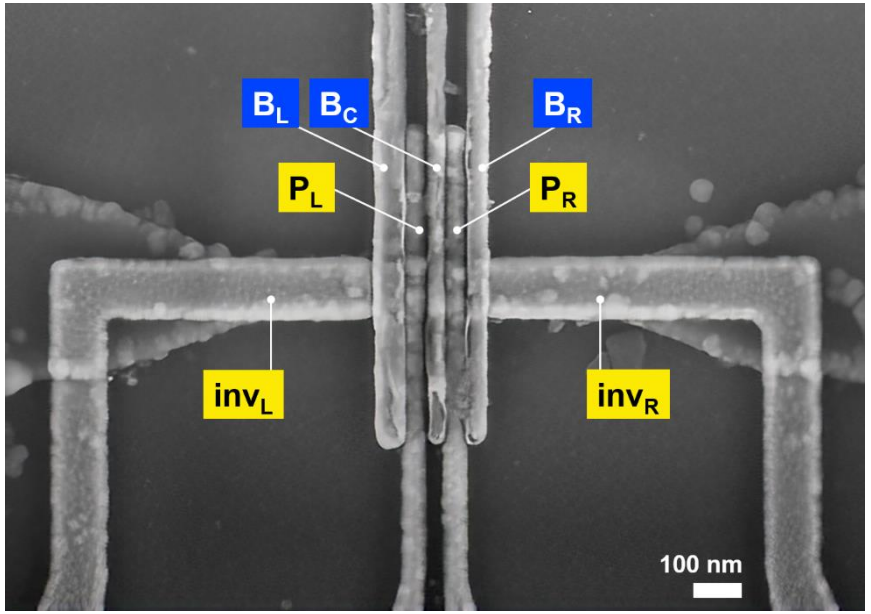
Possible advantages of FDSOI electron/hole spin qubits:

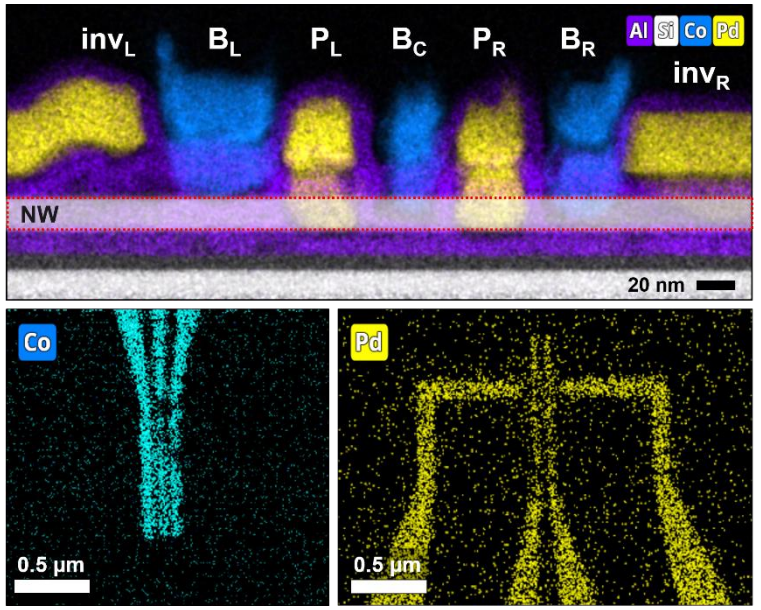
- Device-to-device isolation
- Low doping
- Back-gate



SEM picture of a single dot NW device after patterning the metal layers.

Spin Qubit Architectures





Bersano, Fabio, et al. "Quantum Dots Array on Ultra-Thin SOI Nanowires with Ferromagnetic Cobalt Barrier Gates for Enhanced Spin Qubit Control." *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, 2023.

SEM/EDX picture of a double dot FDSOI NW device.

In a practical spin qubit device, it's typical to require two quantum dots, as this configuration allows for the manipulation and coupling of individual electron spins to perform quantum operations. Additionally, a ferromagnetic component is integrated to provide the necessary magnetic field control for these electrons. This ferromagnetic element generates a localized or slanting magnetic field, which is essential for enabling electron dipole spin resonance (EDSR) and for achieving precise spin manipulation through electric fields.

Conclusions

- **SET** is a unique nanoscale device working with **discrete charge tunneling**; periodic transfer characteristics under **Coulomb blockade** (orthodox theory)
- island ~ **1nm for room temperature operation**
- **SET fabrication is very challenging**: nano-scale features, defect-free materials, possible by both **top-down** and **bottom-up** techniques
- PADOX (Pattern Dependent Oxidation) technology was proposed for single island silicon SET fabrication with most successful results – SET logic operation a few tens of K
- multiple-island SET by **ultra-thin nanograin materials** is easier for room temperature SET but the electrical characteristics are more irregular and are only suited for memory applications and not for logic circuits
- use in **metrology**
- **co-integration of SETs with CMOS for new hybrid functions: hybrid ICs**
- New timely and trendy direction: **SET AS SUPERSENSITIVE QUBIT READOUT @ CRYOGENIC TEMPERATURE**