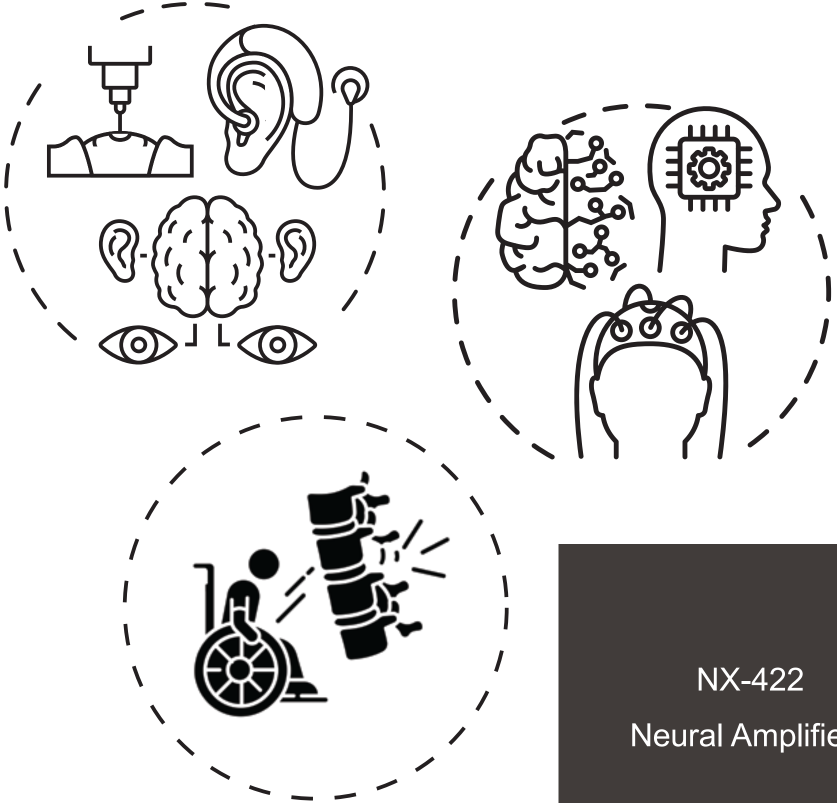


Neural Interfaces

NX-422

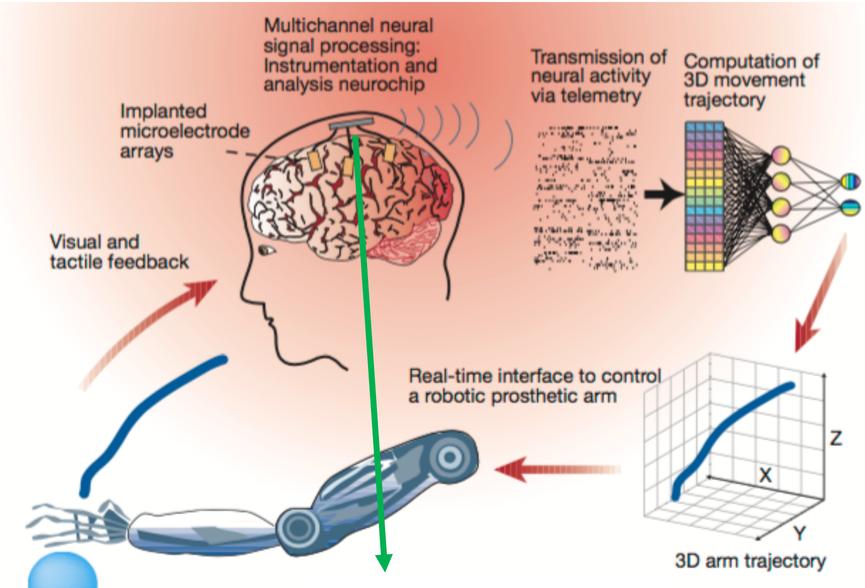
Neural Amplifiers

Mahsa Shoaran

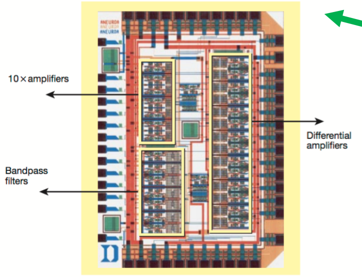
IEM and Neuro-X Institutes

Recap: Two Types of Neural Interfaces

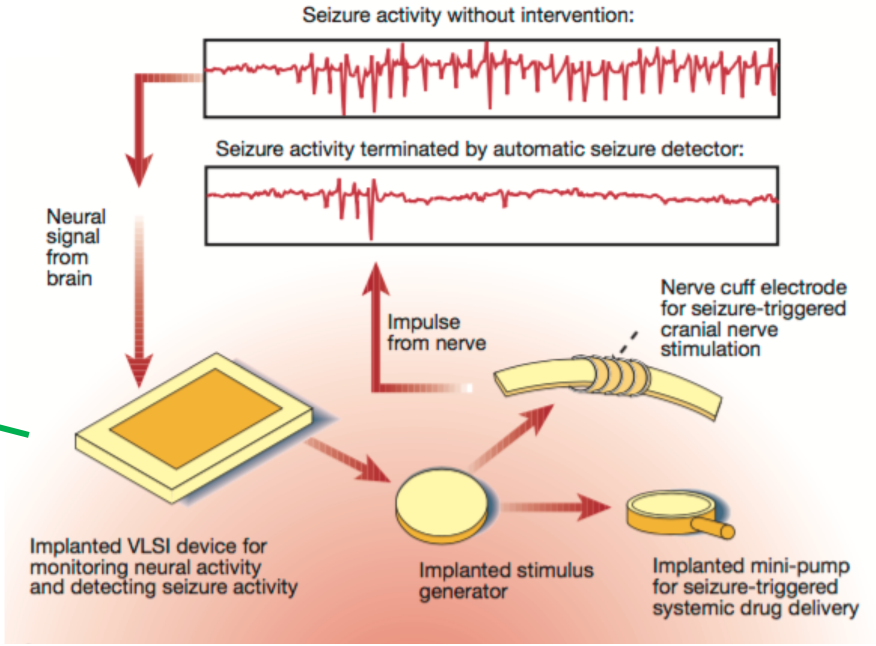
1) Brain-Machine Interface



A microchip for recording and processing brain signals



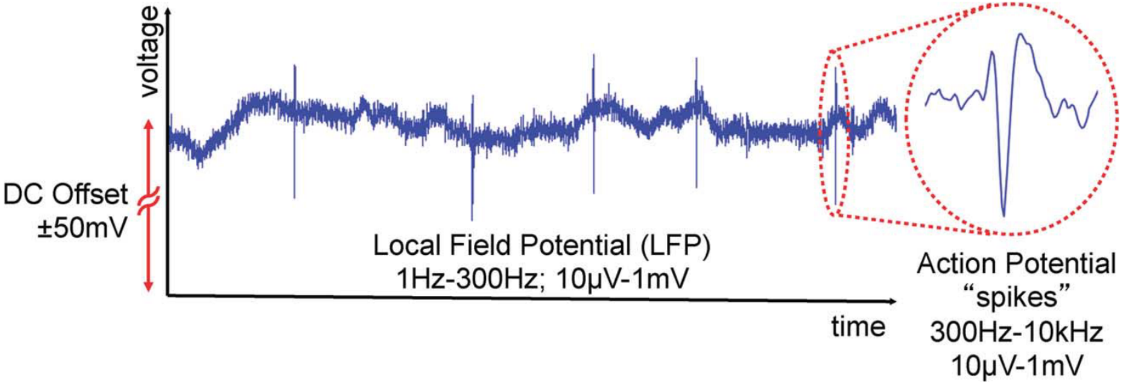
2) Closed-loop Neuromodulation



Recap: Local Field Potentials (LFPs)

- < 300 Hz : **Local Field Potentials (LFP)**
- 300 – 10kHz : **Single-Unit Activity (AP or “spikes”)**

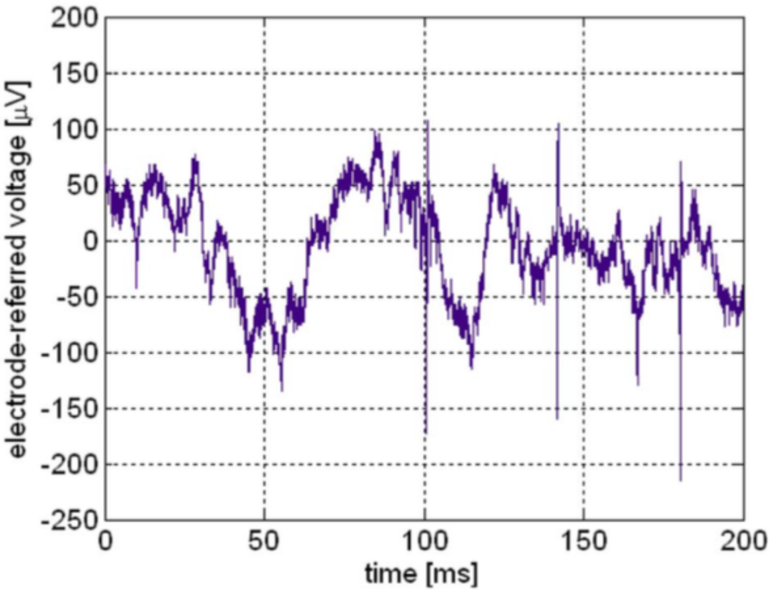
- Local Field Potential (LFP) – electrical activity of all cells **averaged over some spatial neighborhood**
- **High-pass filtering** gives **spikes**

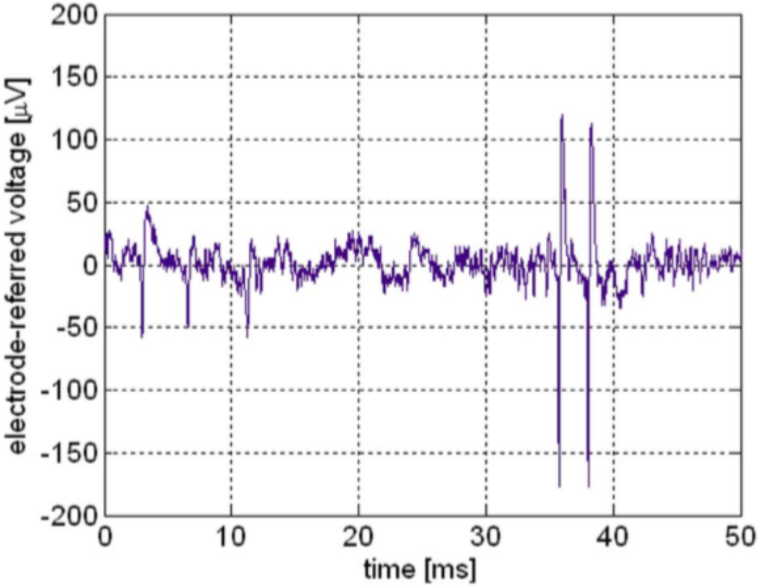


Spike/LFP Recording

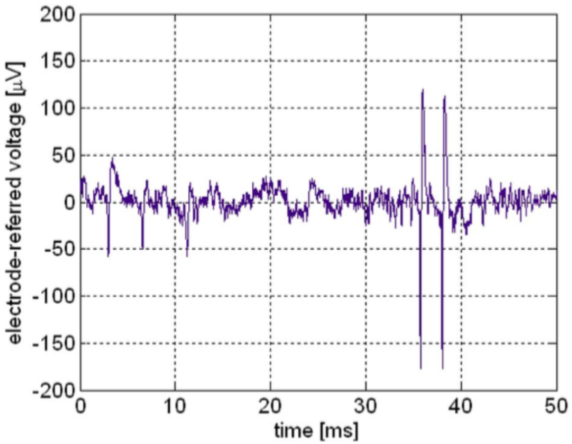
High-pass filter at 300Hz

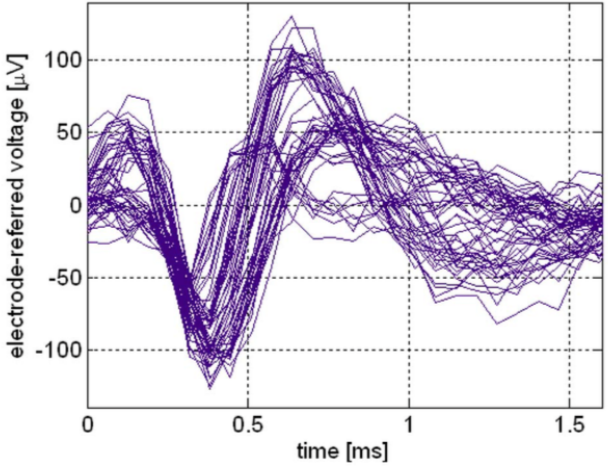
Both Spikes and LFPs → **Spikes**



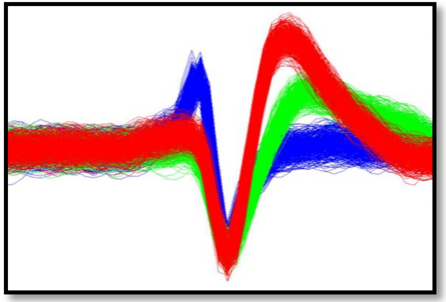


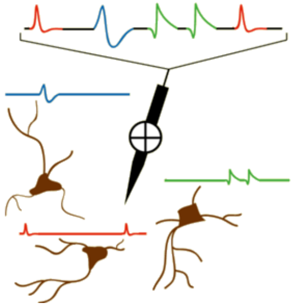
Spike Sorting



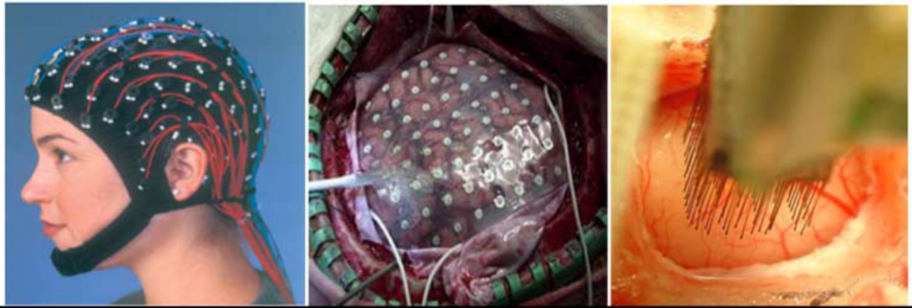


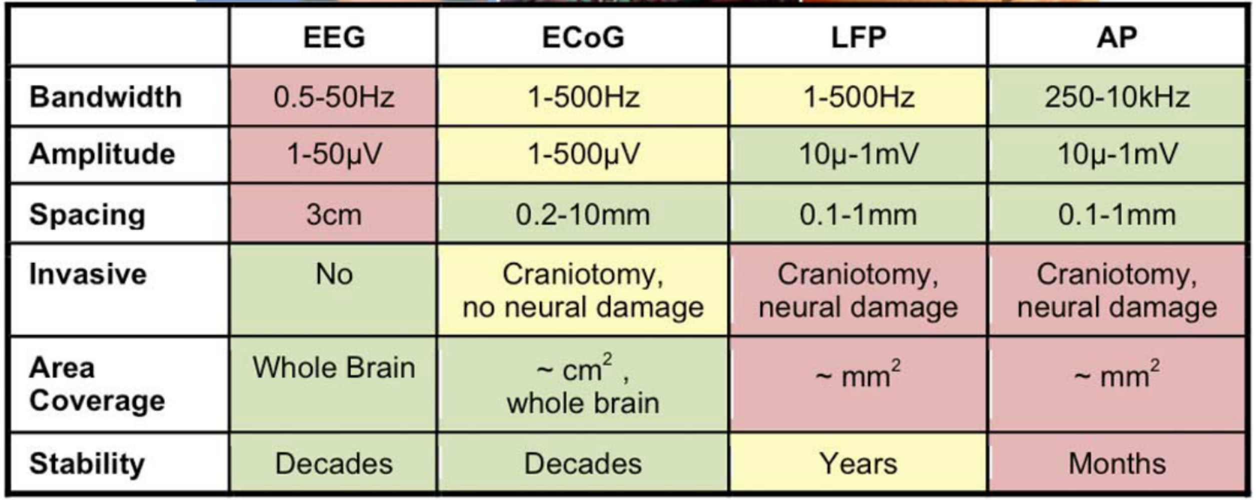
Spike Sorting





Comparison: EEG, ECoG, LFP, and AP

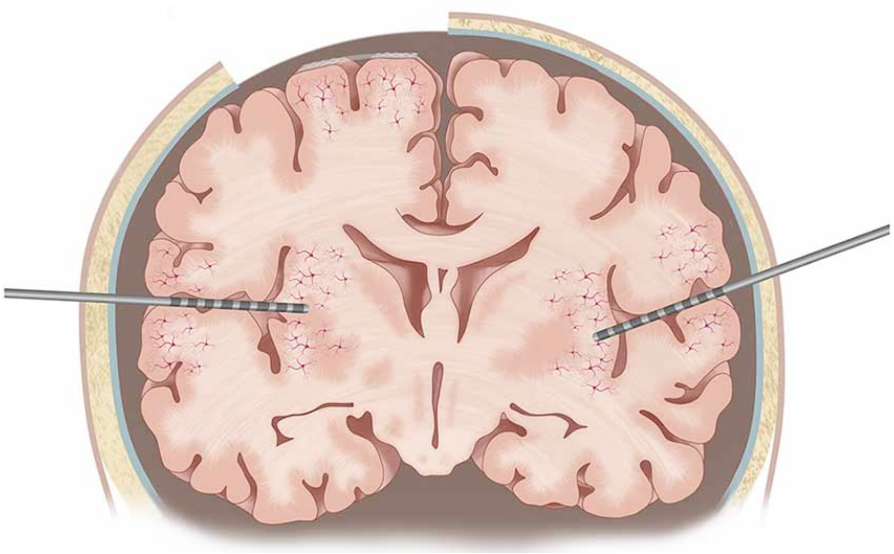




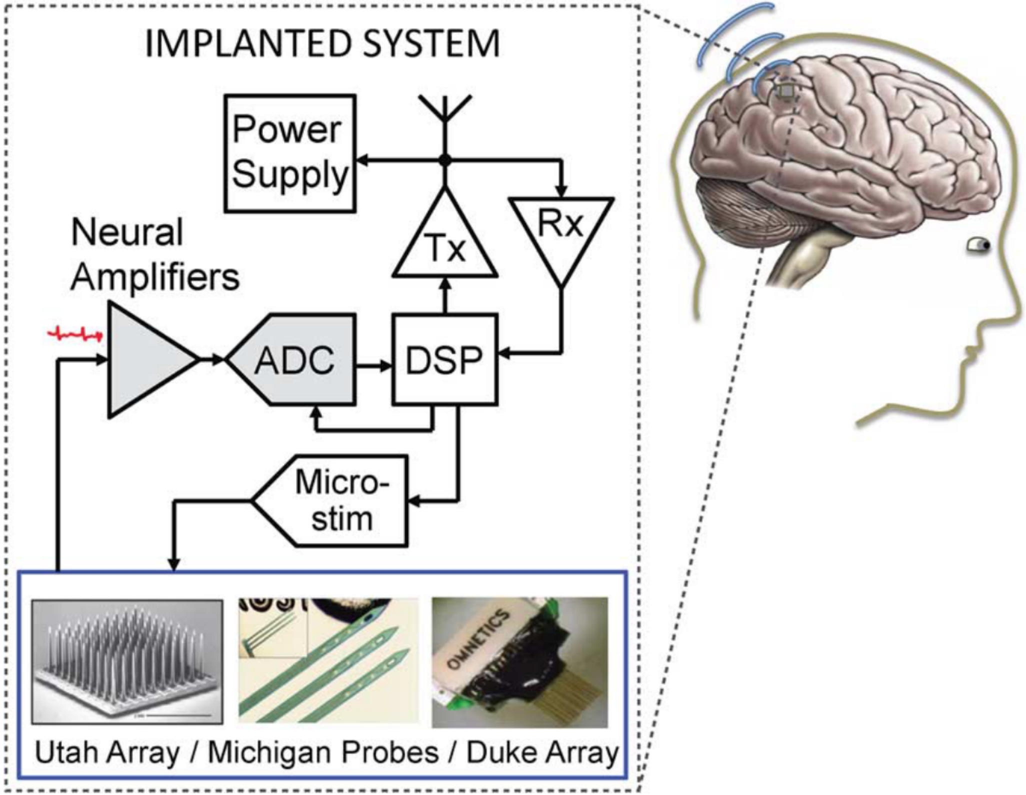
	EEG	ECoG	LFP	AP
Bandwidth	0.5-50Hz	1-500Hz	1-500Hz	250-10kHz
Amplitude	1-50µV	1-500µV	10µ-1mV	10µ-1mV
Spacing	3cm	0.2-10mm	0.1-1mm	0.1-1mm
Invasive	No	Craniotomy, no neural damage	Craniotomy, neural damage	Craniotomy, neural damage
Area Coverage	Whole Brain	~ cm^2 , whole brain	~ mm^2	~ mm^2
Stability	Decades	Decades	Years	Months

R. Muller et al., JSSC 2015

Stereo EEG (sEEG)



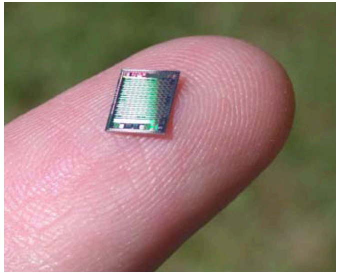
Circuit Block Diagram of a Neural Interface



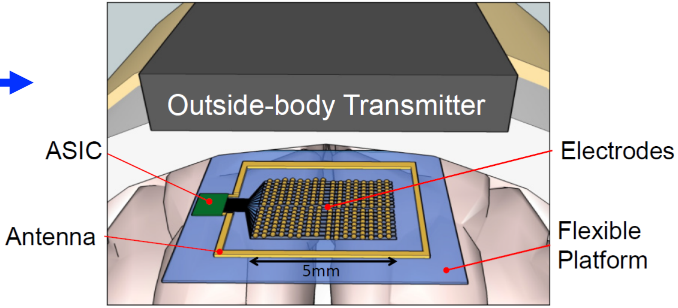
R. Muller et al., JSSC 2012

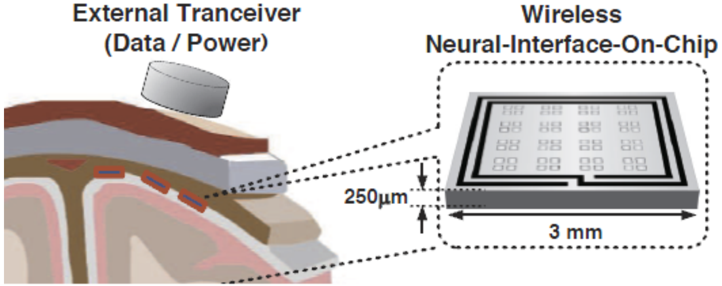
Cortical and Intracortical Systems

IC or ASIC

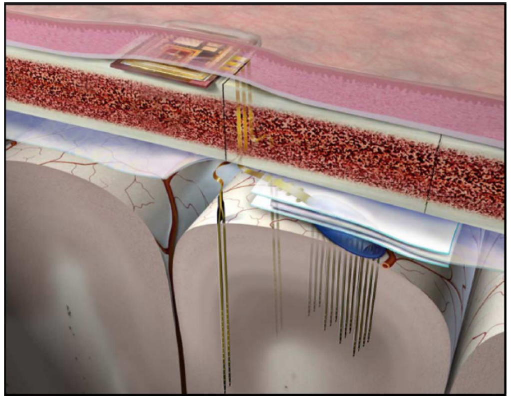


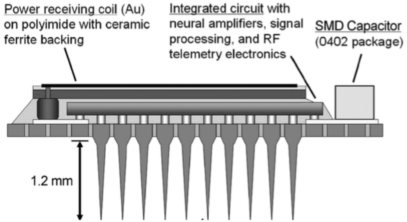
Cortical or ECoG-based systems

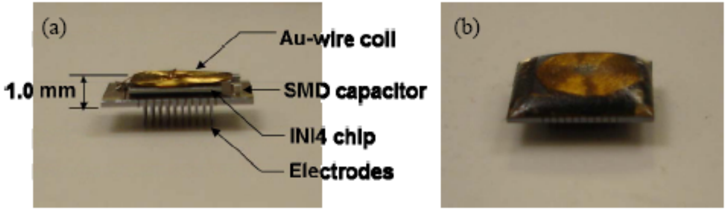




Intracortical systems

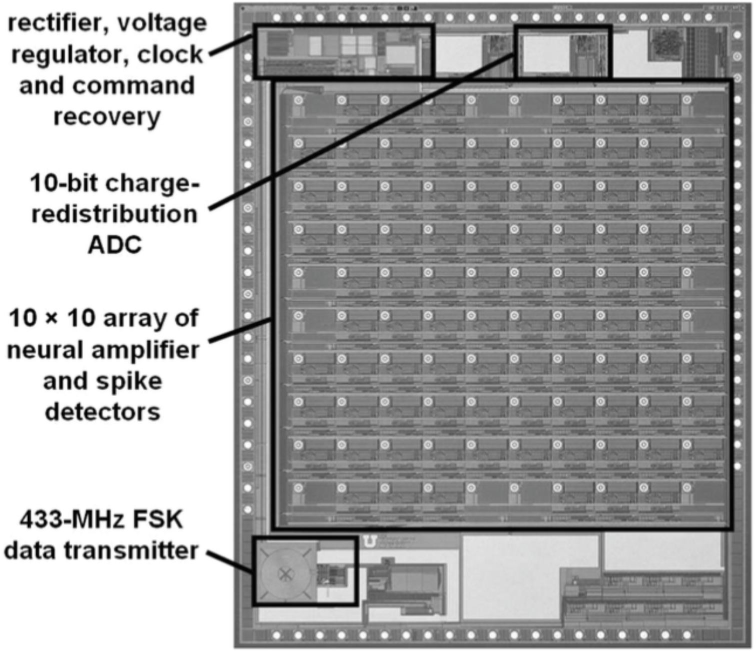






Neural Recording IC

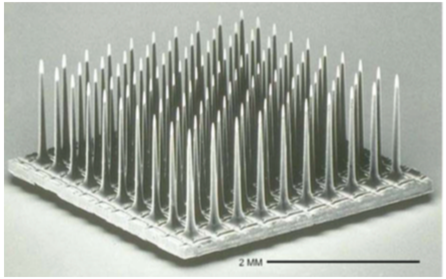
- Microchips include **amplification, filtering, digitization, compression, processing: feature extraction/spike detection/classification, wireless power and data telemetry, bias generation, stimulation, ...**
- Power and area are highly limited

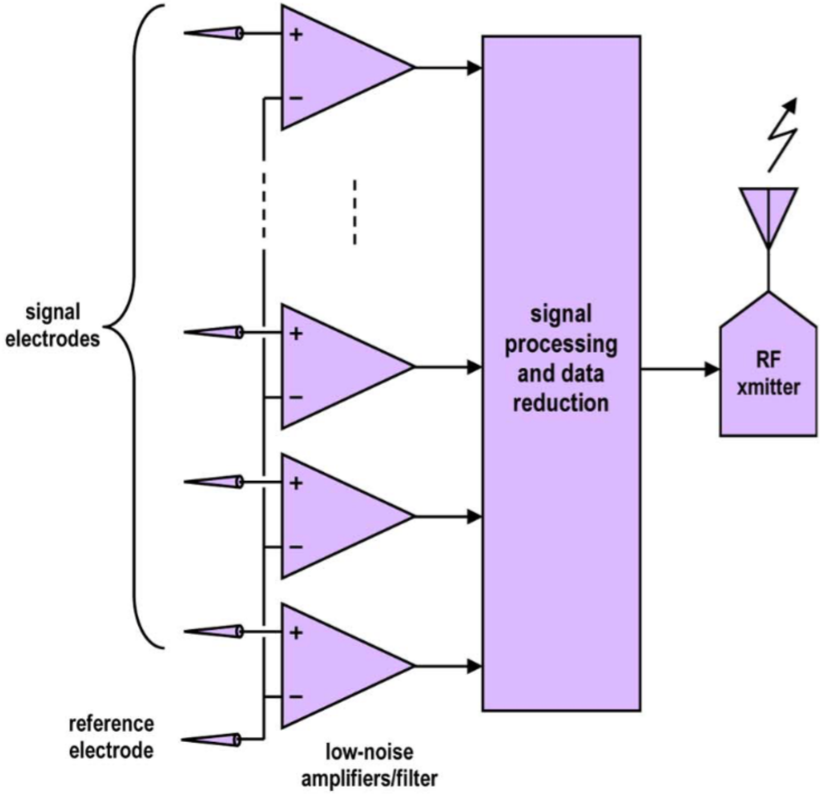


Die photo of 4.7 mm x 5.9 mm chip

R. Harrison, JSSC 2003

Low-Noise Neural Amplifier





R. Harrison, Proceedings of the IEEE, 2008

Design Requirements for Neural Amplifier

1. Sufficiently low input-referred noise to resolve spikes as small as 10 μV in amplitude
2. Sufficient dynamic range to record spikes or LFPs as large as 1–2 mV in amplitude
3. Much higher input impedance than the electrode-tissue interface
4. Amplify signals in the frequency bands of interest (roughly 300 Hz–10 kHz for spikes and 1–300 Hz for local field potentials)
5. Block DC offsets present at the electrode-tissue interface to prevent saturation of the amplifier

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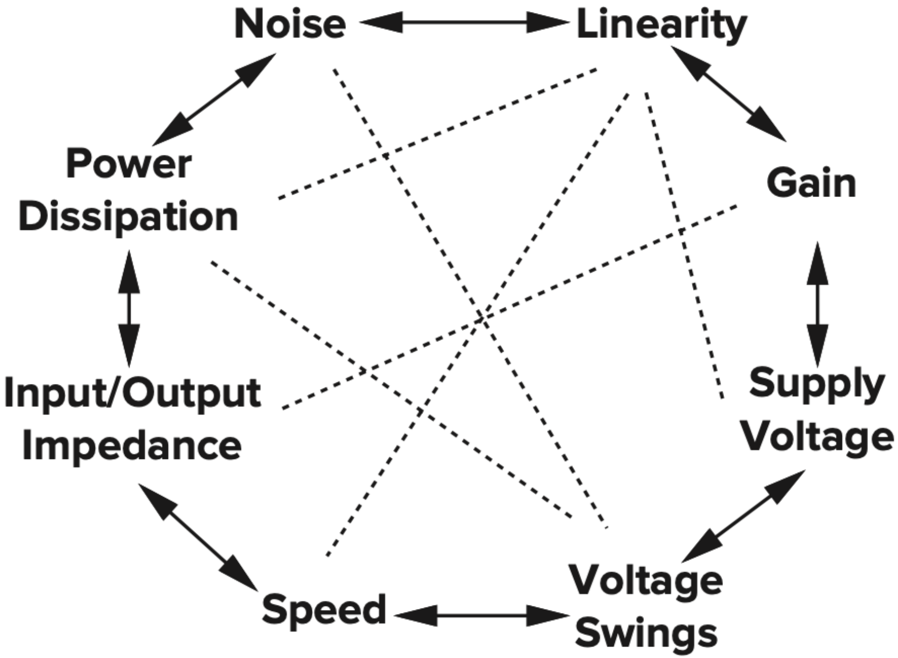
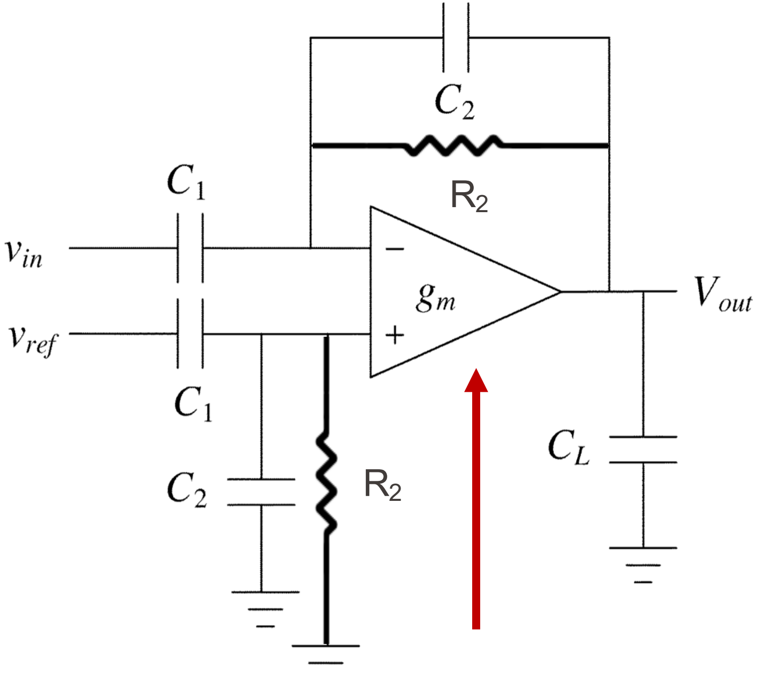
4. Amplify signals in the frequency bands of interest (roughly 300 Hz–10 kHz for spikes and 1–300 Hz for local field potentials)
5. Block DC offsets present at the electrode-tissue interface to prevent saturation of the amplifier
6. Consume little silicon area and use few or no off-chip components to minimize size
7. High common-mode rejection ratio to minimize interference from 50/60 Hz power line noise, and a high power-supply rejection ratio if power supply noise is significant (e.g., from ac inductive power links);
8. Consume low power to limit the chronic heating of surrounding tissue to less than 1ºC.

…

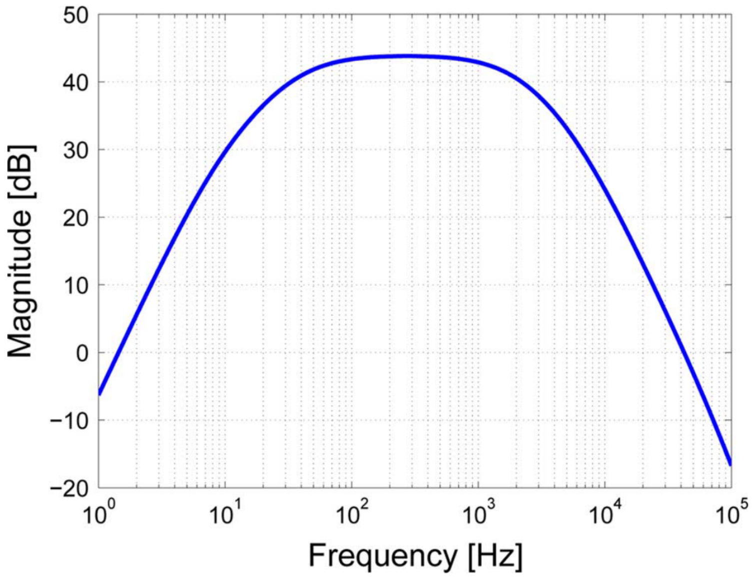
Design Trade-offs



Neural Amplifier: Capacitive Feedback Architecture



OTA:
Operational Transconductance Amplifier

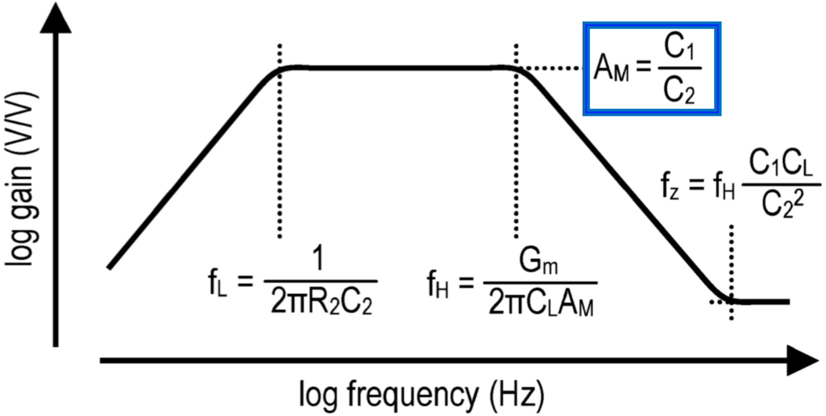

Amplifier Gain versus Frequency

M. Shoaran et al., TBioCAS 2014

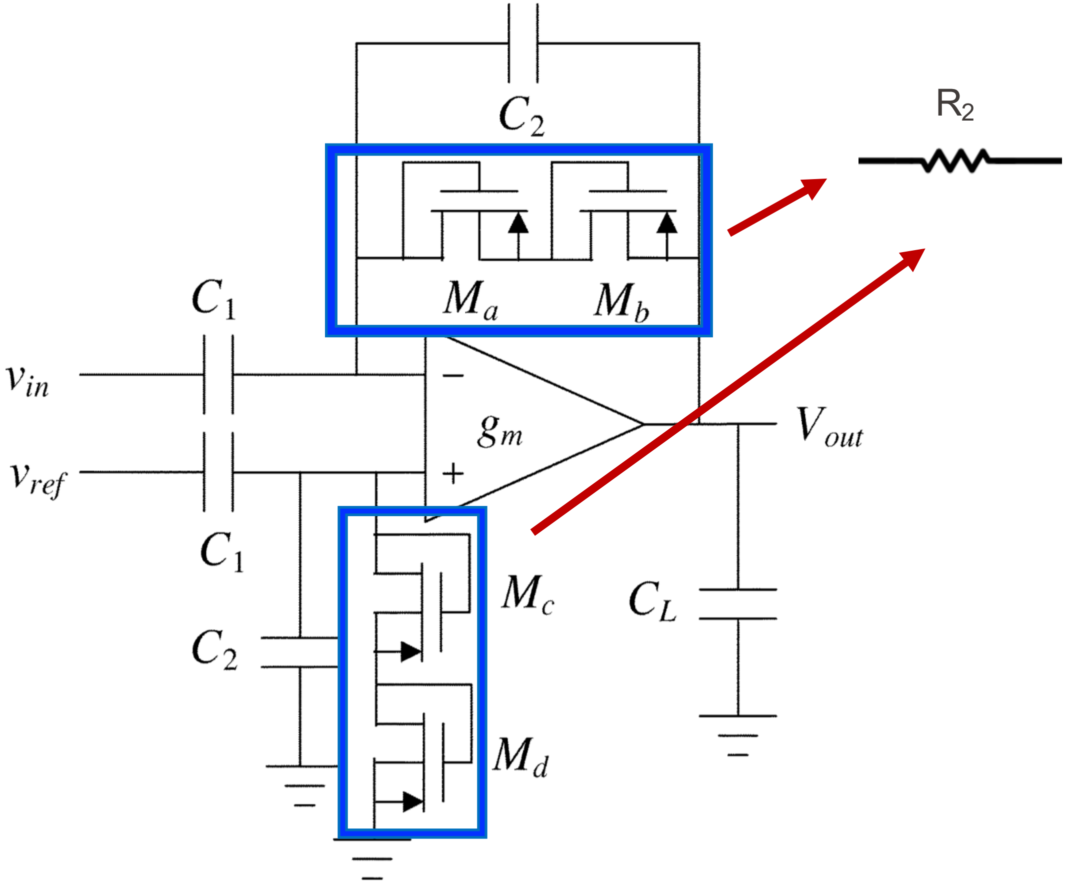
Neural Amplifier: Transfer Function

$$\frac{v_{\text{out}}}{v_{\text{in}+} - v_{\text{in}-}} = \frac{C_1}{C_2} \cdot \frac{1 - sC_2/G_m}{\left(\frac{1}{sR_2C_2} + 1\right)\left(s\frac{C_LC_1}{G_mC_2} + 1\right)}$$

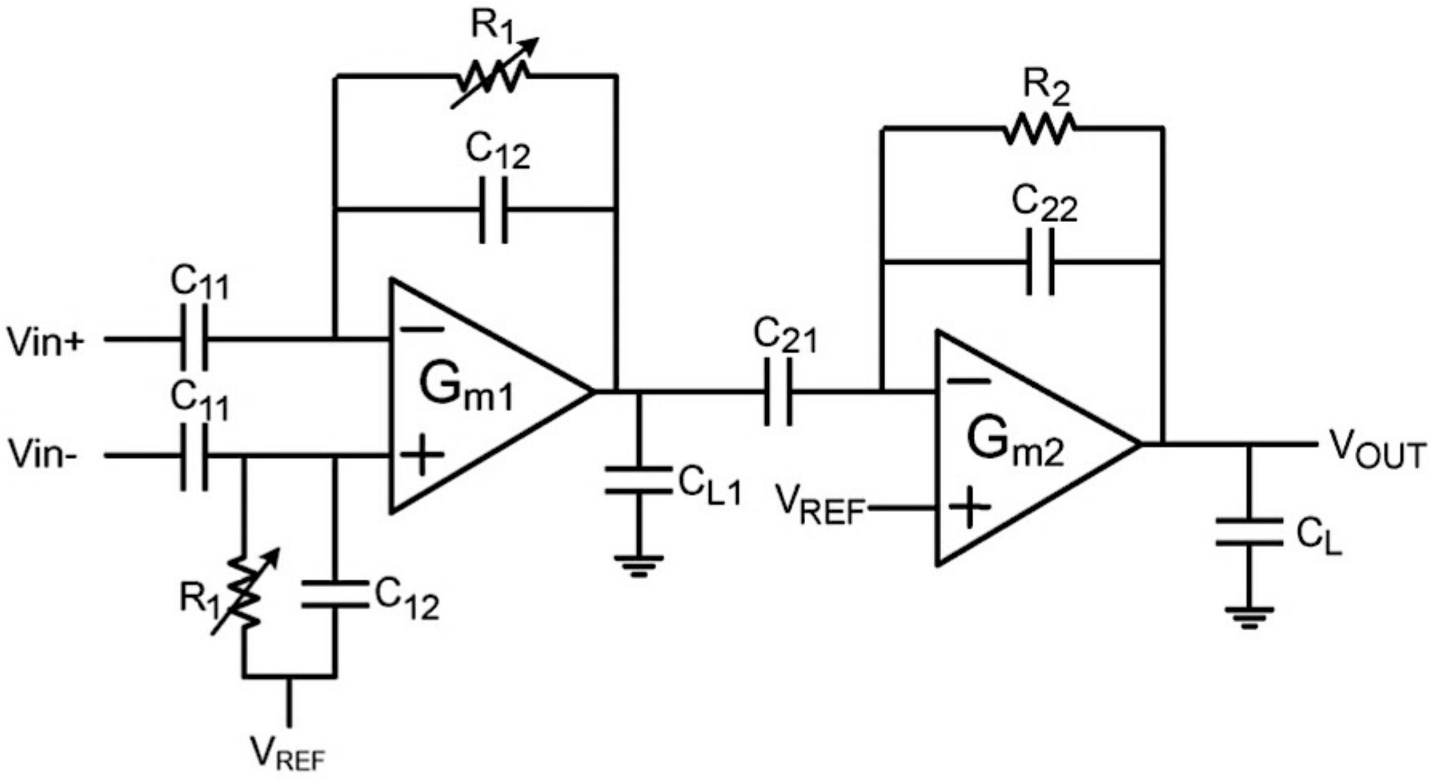
$$= A_M \frac{1 - s/(2\pi f_z)}{\left(\frac{2\pi f_L}{s} + 1\right)\left(\frac{s}{2\pi f_H} + 1\right)}.$$



Neural Amplifier: Capacitive Feedback Architecture

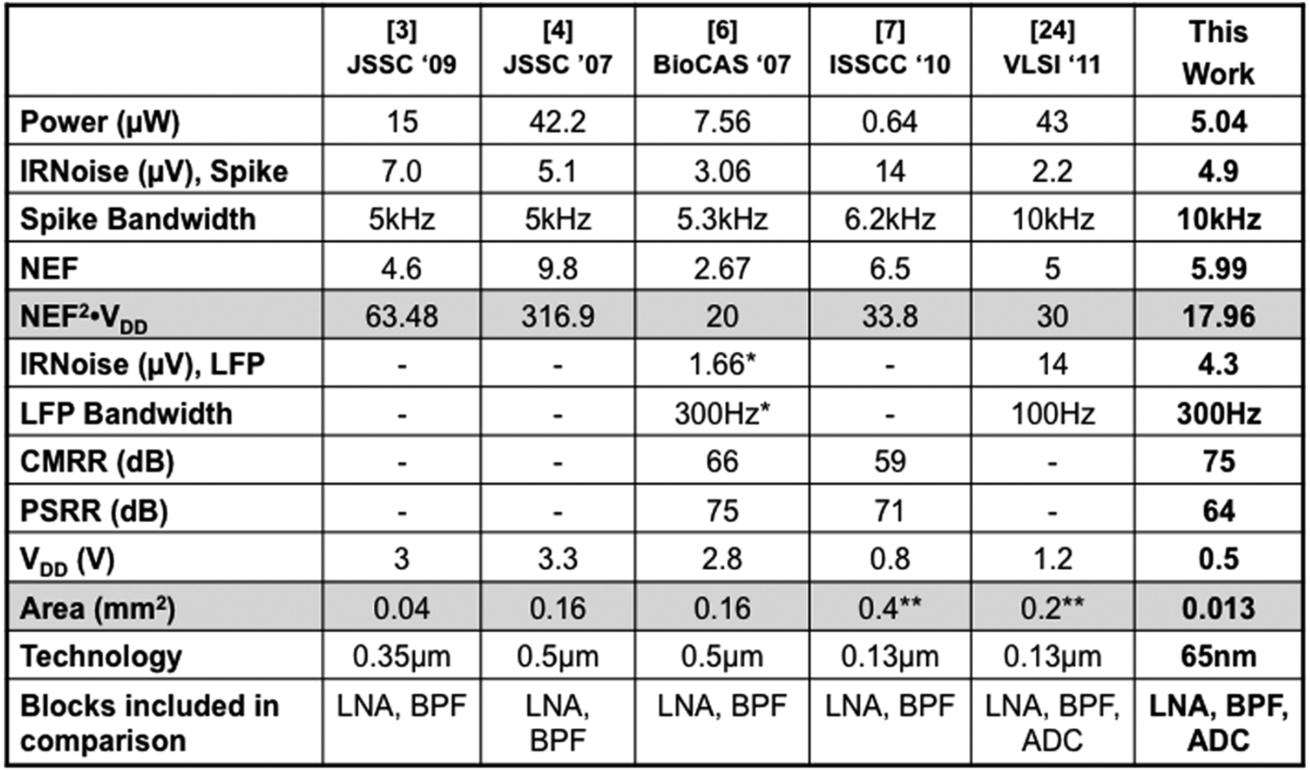


Neural Amplifier: Multi-Stage, Higher Gain



Neural Implants: Power, Area, Noise, …

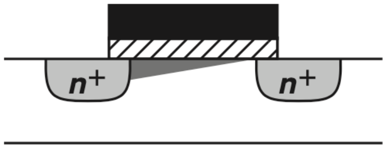
- A typical performance and comparison table



	[3] JSSC '09	[4] JSSC '07	[6] BioCAS '07	[7] ISSCC '10	[24] VLSI '11	**This Work**
Power (μW)	15	42.2	7.56	0.64	43	**5.04**
IRNoise (μV), Spike	7.0	5.1	3.06	14	2.2	**4.9**
Spike Bandwidth	5kHz	5kHz	5.3kHz	6.2kHz	10kHz	**10kHz**
NEF	4.6	9.8	2.67	6.5	5	**5.99**
$NEF^2 \cdot V_{DD}$	63.48	316.9	20	33.8	30	**17.96**
IRNoise (μV), LFP	-	-	1.66*	-	14	**4.3**
LFP Bandwidth	-	-	300Hz*	-	100Hz	**300Hz**
CMRR (dB)	-	-	66	59	-	**75**
PSRR (dB)	-	-	75	71	-	**64**
V_{DD} (V)	3	3.3	2.8	0.8	1.2	**0.5**
Area (mm^2)	0.04	0.16	0.16	0.4**	0.2**	**0.013**
Technology	0.35μm	0.5μm	0.5μm	0.13μm	0.13μm	**65nm**
Blocks included in comparison	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF, ADC	**LNA, BPF, ADC**

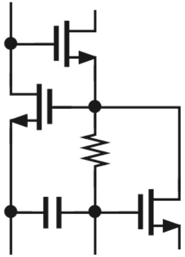
IC Design: Device, Circuit, Architecture, System

Device



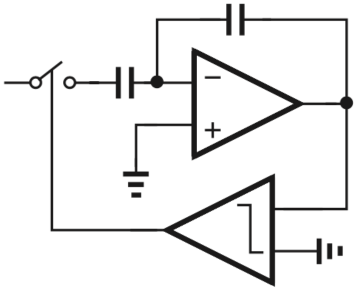
(a)

Circuit



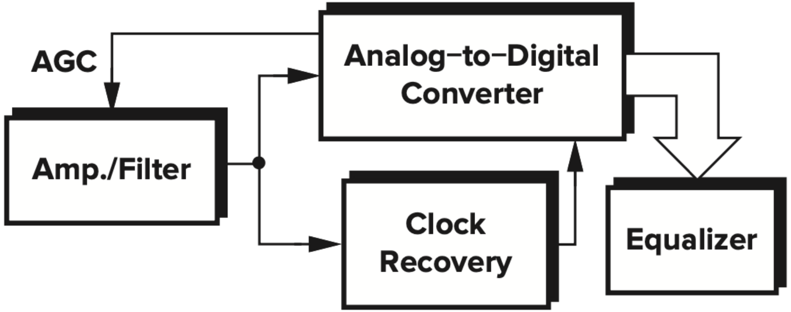
(b)

Architecture



(c)

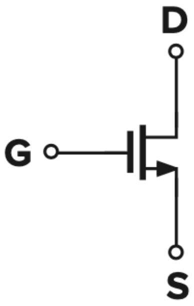
System



(d)

Transistor?

NMOS



$$\boxed{I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2}$$

NMOS Transistor

- An n-type MOS (**NMOS**) device on a **p-type substrate**
  - a heavily-doped polysilicon **(conductor)** operating as the **gate**
  - a thin layer of silicon dioxide (SiO_2) **insulating** the gate from the substrate
  - two heavily-doped **n regions**: **source** and **drain** terminals