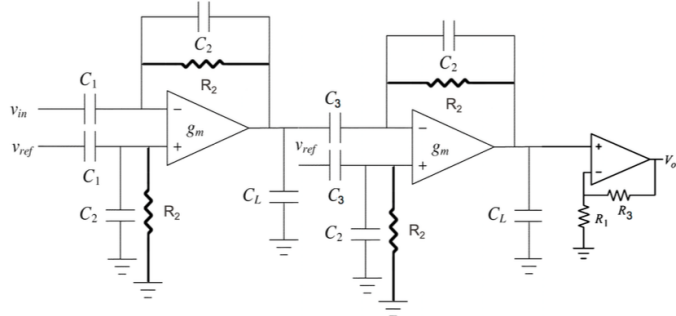


NX-422 EXERCISE 3 – Implantable Electronics Solutions

1. Let's check the details of the three-stage neural amplifier.



(a) The equation for the overall mid-band gain:

$$|A_V|_{3\text{-Stage}} = |A_{V1} \times A_{V2} \times A_{V3}| = \left(\frac{C_1}{C_2}\right) \times \left(\frac{C_3}{C_2}\right) \times \left(\frac{R_1 + R_3}{R_1}\right)$$

(b) Assuming $C_2 = C_u$, we will find the values of C_1 and C_3 in terms of C_u . Ignore C_L , and assume $R_1=40\text{k}\Omega$ and $R_3=60\text{k}\Omega$. For our calculations, we are asked to have a total mid-band gain of 1000 and minimize the chip area by minimizing the total capacitance.

Let's start:

$$C_2 = C_u \text{ assume } C_1 = M \times C_u \text{ and } C_3 = N \times C_u$$

We know that $R_1=40\text{k}\Omega$ and $R_3=60\text{k}\Omega$. Hence, $\frac{R_1+R_3}{R_1} = \frac{100\text{k}\Omega}{40\text{k}\Omega} = 2.5$.

$$|A_V|_{3\text{-Stage}} = 1000 \rightarrow \left(\frac{C_1}{C_2}\right) \times \left(\frac{C_3}{C_2}\right) = \frac{1000}{2.5} = 400 = M \times N$$

Total capacitance excluding C_L is

$$= 2C_1 + 2C_2 + 2C_3 + 2C_2 = 2 \times (M + N + 2) \times C_u$$

$$\text{Area} \propto 2 \times (M + N + 2) \times C_u$$

$$2 \times (M + N + 2) \times C_u = 2 \times \left(M + \frac{400}{M} + 2\right) \times C_u = f(M)$$

To minimize the total capacitance and area $\frac{df}{dM} = 0 \rightarrow 1 - \frac{400}{M^2} = 0$

$$\rightarrow M_{\text{opt}} = 20$$

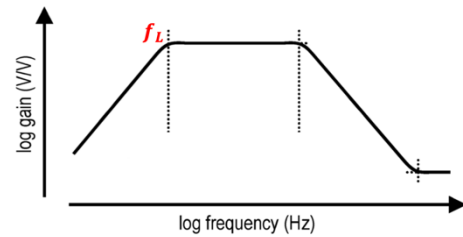
$$\rightarrow C_1 = 20C_u \text{ and } C_3 = \frac{400}{20} C_u = 20C_u$$

(c) The amplifier's bandwidth is set by the first stage and $C_2 = 400\text{fF}$.

$$f_L = \frac{1}{2 \times \pi \times R_2 \times C_2} = 1 \text{ Hz}$$

$$C_2 = C_u = 400 \text{ fF}$$

$$R_2 = \frac{1}{2 \times \pi \times 400 \times 10^{-15}} = 3.98 \times 10^{11} \\ = 0.398 \text{ T}\Omega$$



2. We will draw the drain current of an NMOS (I_D) as a function of V_{GS} where V_{GS} varies from $0 \rightarrow 3\text{V}$.

- $\frac{W}{L} = \frac{50}{0.5}$, $V_{DS} = 3\text{V}$, $V_{TH} = 0.7\text{V}$, $\mu_n C_{ox} = 50 \mu\text{A}/\text{V}^2$ and $\lambda = 0$.

Saturation condition: $V_{DS} > V_{GS} - V_{TH}$

$3\text{V} > (0 \rightarrow 3\text{V}) - 0.7\text{V}$, which means that the assumption is correct. The transistor is in saturation.

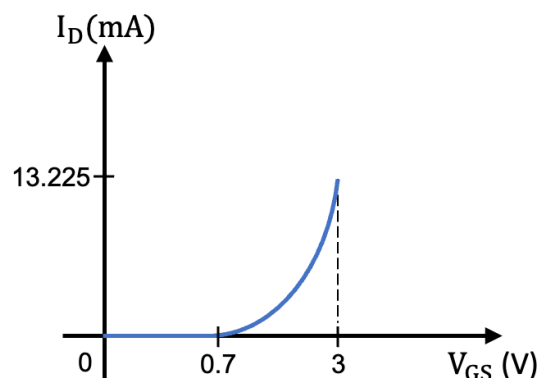
The drain current equation for the saturation ($\lambda = 0$):

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

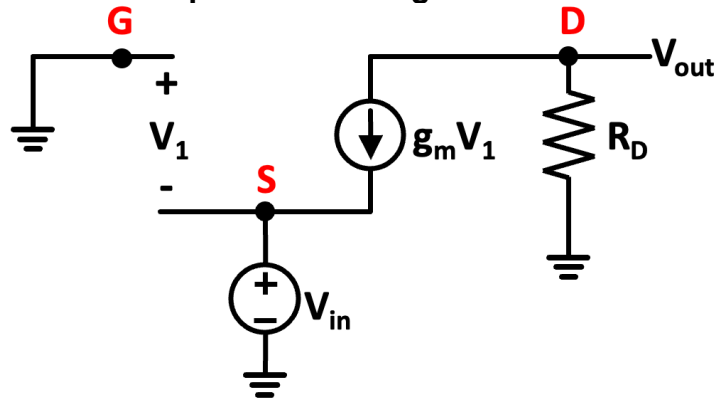
$$I_D = \frac{1}{2} \times (50 \frac{\mu\text{A}}{\text{V}^2}) \times \frac{50}{0.5} \times (V_{GS} - 0.7)^2$$

$$I_D = 2.5 \frac{\text{mA}}{\text{V}^2} (V_{GS} - 0.7)^2$$

At $V_{GS} = 3\text{V} \rightarrow I_D = 13.225\text{mA}$



3. (a) Common-Gate Amplifier Small-Signal Model:



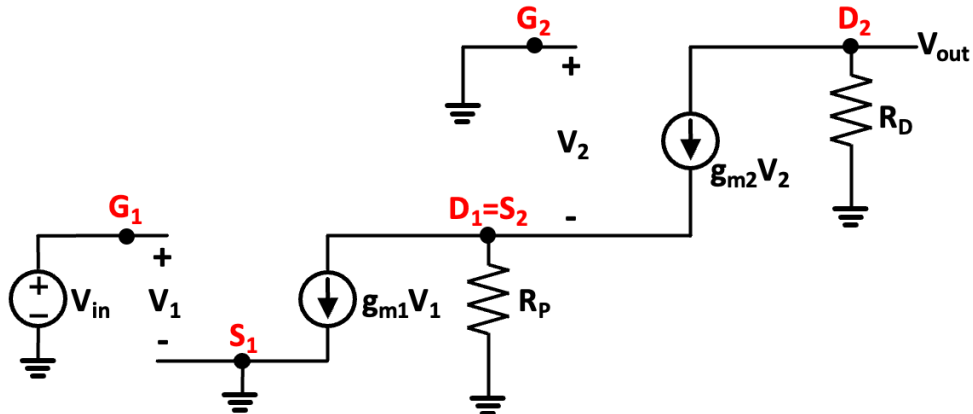
$$V_{GS} = V_1 = -V_{in}$$

$$V_{out} = -g_m V_1 \times R_D$$

$$V_{out} = -g_m \times (-V_{in}) \times R_D$$

$$A_V = \frac{V_{out}}{V_{in}} = g_m \times R_D$$

(b) Cascode Amplifier Small-Signal Model:



$$-V_2 = (g_{m2} V_2 - g_{m1} V_1) \times R_P$$

$$V_2 \times (g_{m2} R_P + 1) = g_{m1} V_1 \times R_P$$

$$V_2 = V_1 \times \left(\frac{g_{m1} R_P}{g_{m2} R_P + 1} \right)$$

$$V_{out} = -g_{m2} V_2 \times R_D$$

$$V_{out} = -g_{m2} R_D \times V_1 \times \left(\frac{g_{m1} R_P}{g_{m2} R_P + 1} \right)$$

$$V_{in} = V_1$$

$$A_V = \frac{V_{out}}{V_{in}} = - \frac{g_{m1} g_{m2} R_P R_D}{g_{m2} R_P + 1}$$