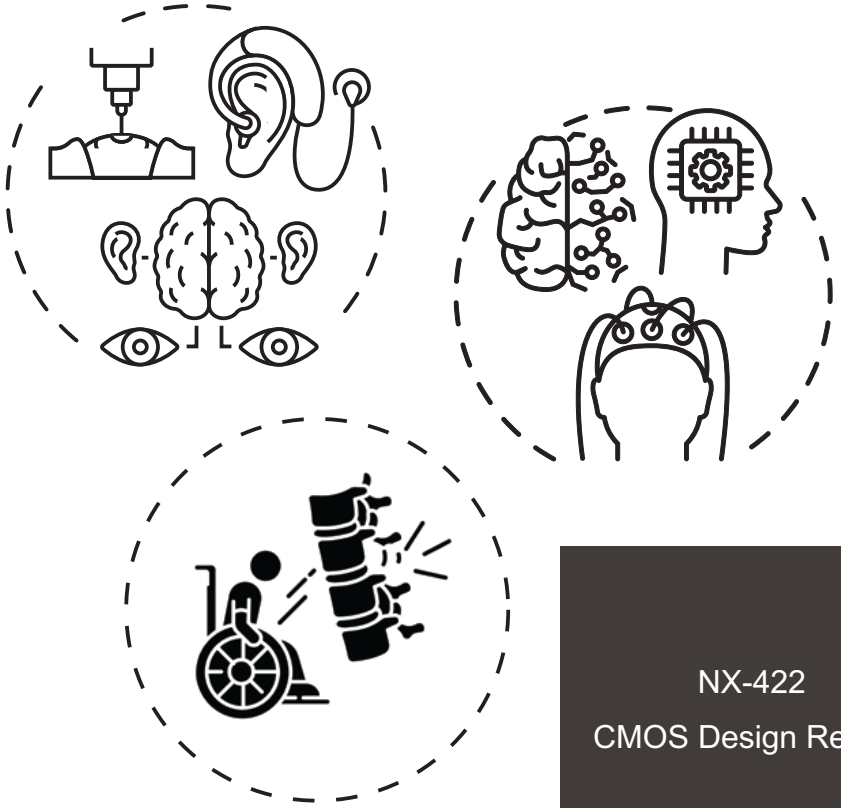


Neural Interfaces

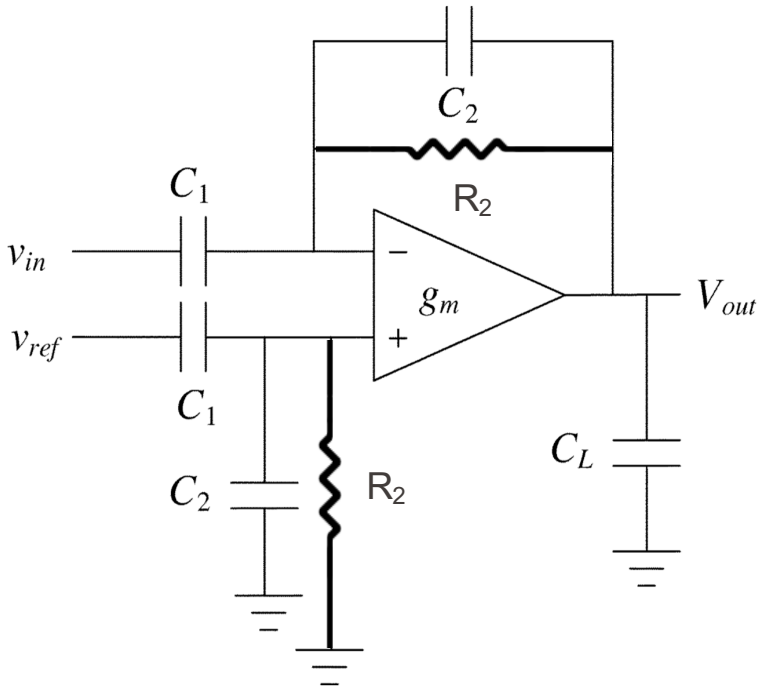
NX-422

CMOS Design Review

Mahsa Shoaran

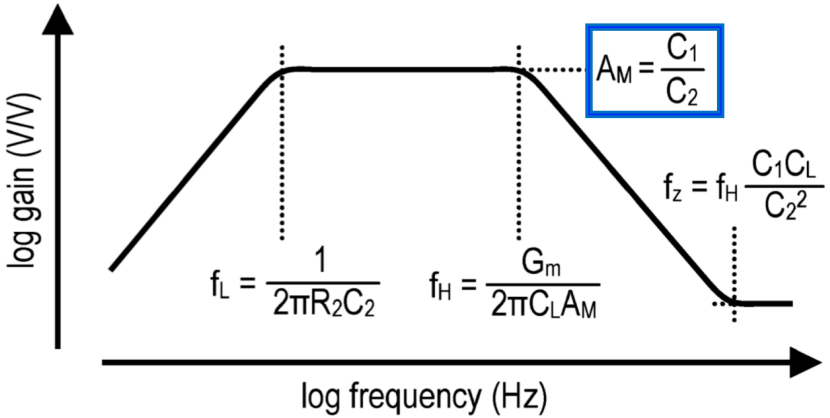
IEM and Neuro-X Institutes

Recap: Neural Amplifier: Capacitive Feedback Architecture

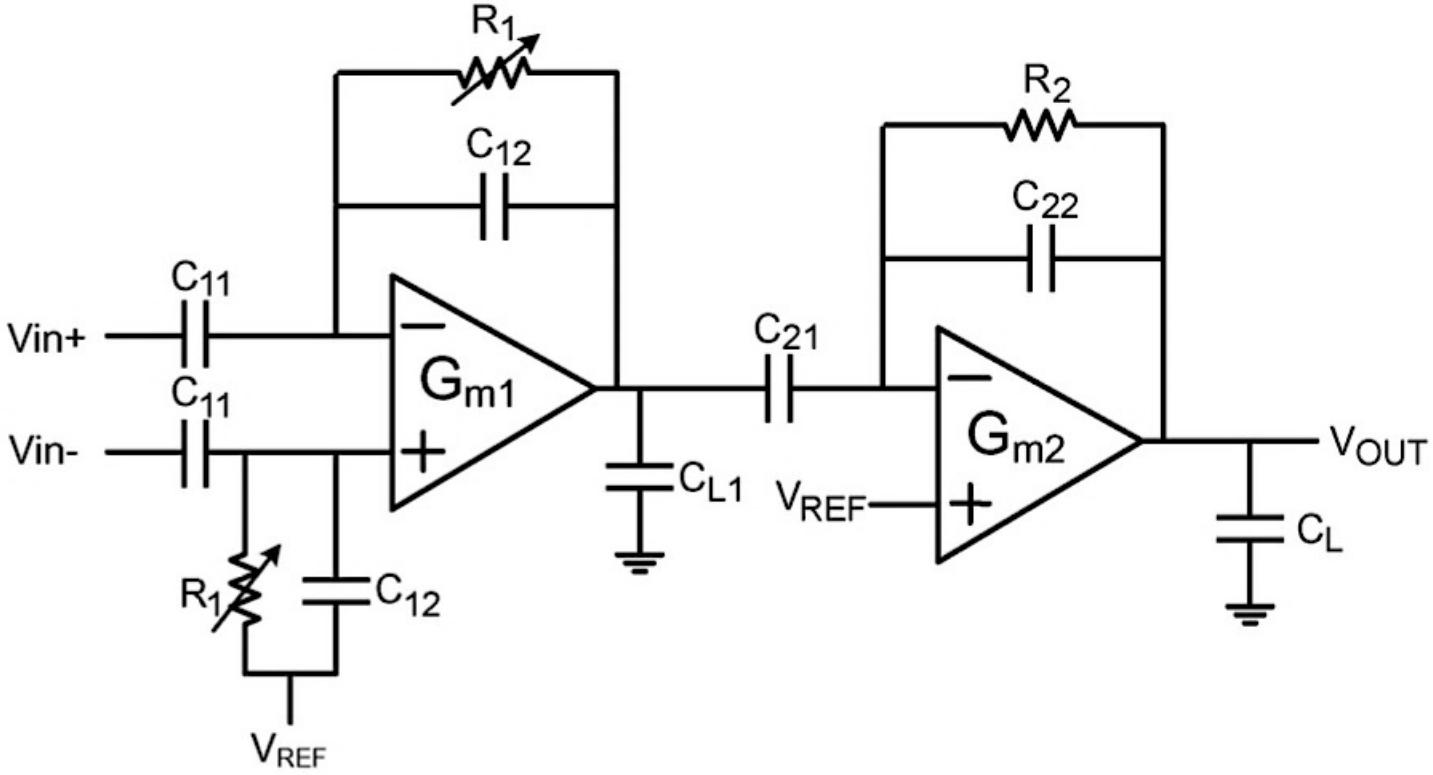


$$\frac{v_{\text{out}}}{v_{\text{in}+} - v_{\text{in}-}} = \frac{C_1}{C_2} \cdot \frac{1 - sC_2/G_m}{\left(\frac{1}{sR_2C_2} + 1\right)\left(s\frac{C_LC_1}{G_mC_2} + 1\right)}$$

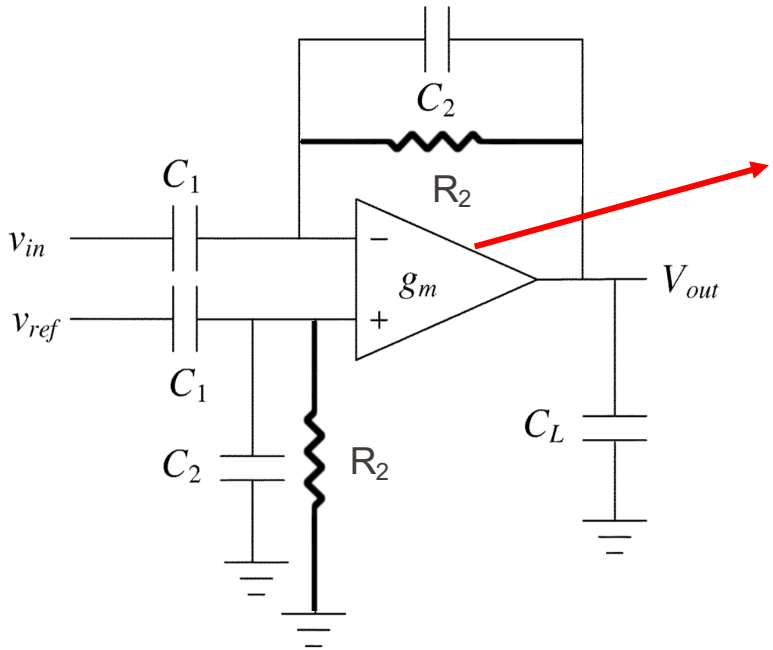
$$= A_M \frac{1 - s/(2\pi f_z)}{\left(\frac{2\pi f_L}{s} + 1\right)\left(\frac{s}{2\pi f_H} + 1\right)}.$$

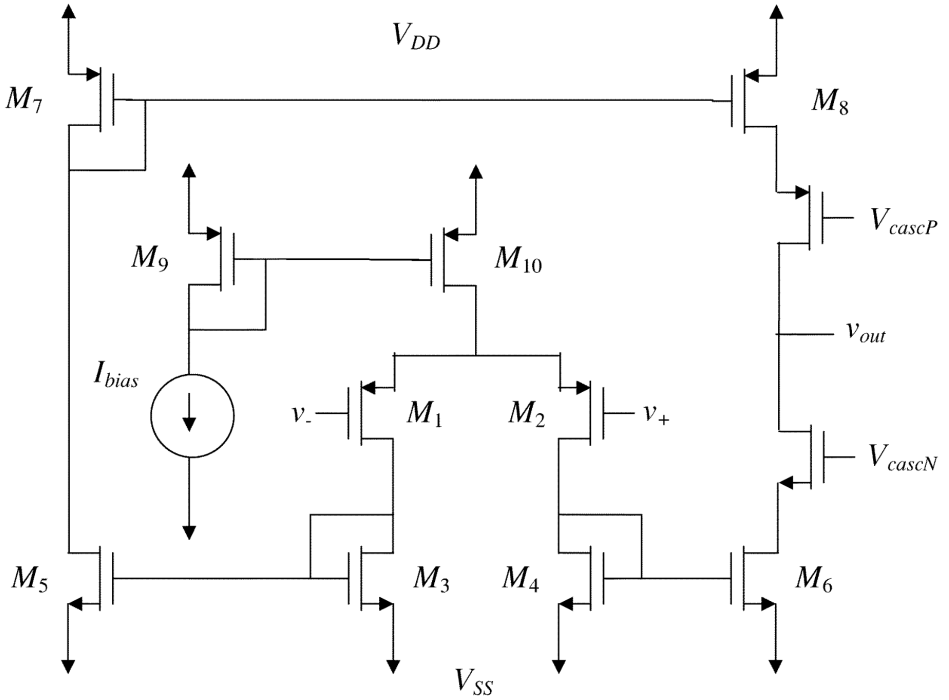


Recap: Neural Amplifier: Multi-Stage, Higher Gain



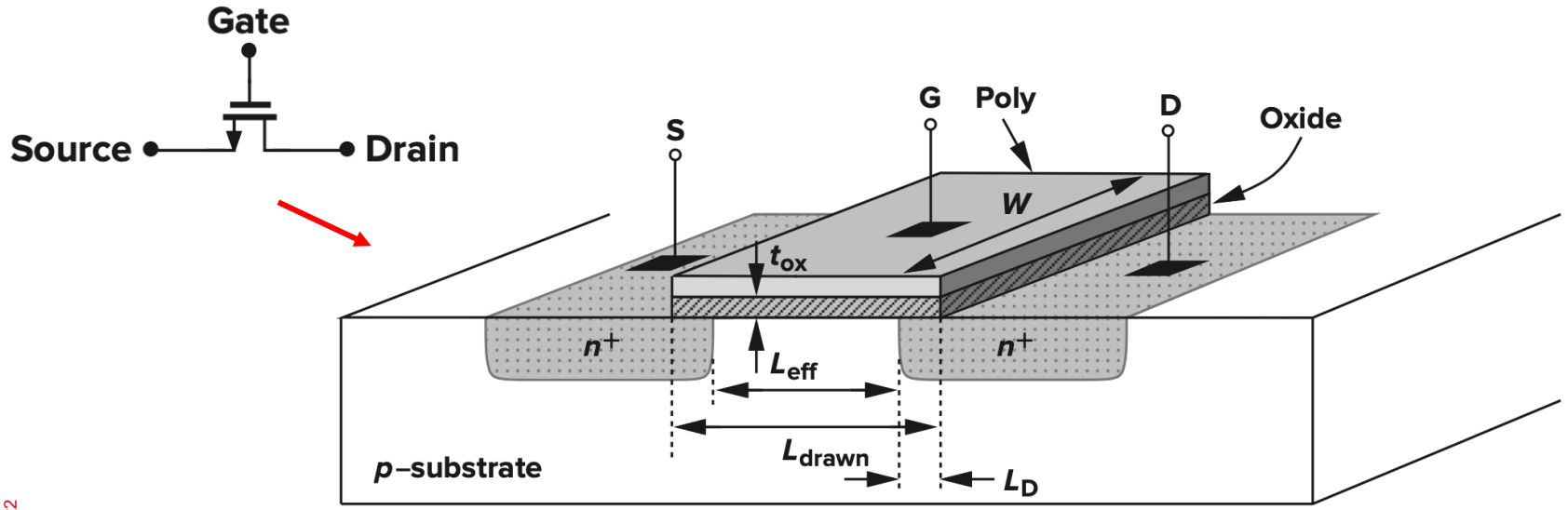
Recap: Neural Amplifier: OTA architecture



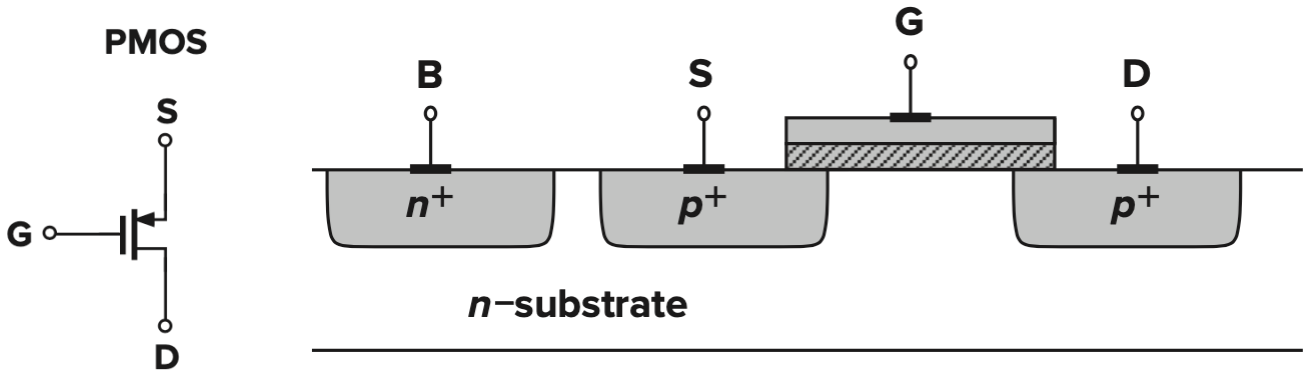


Recap: MOS Transistor

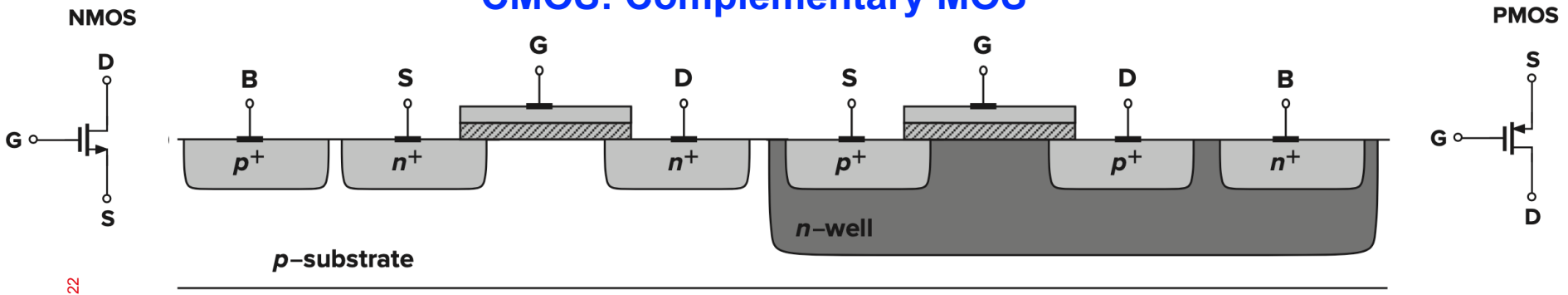
- **MOS: Metal-Oxide-Semiconductor** field-effect transistor (also called MOSFET)
- An n-type MOS (**NMOS**) device on a **p-type substrate**
  - a heavily-doped polysilicon **(conductor)** operating as the **gate**
  - a thin layer of silicon dioxide (SiO_2) **insulating** the gate from the substrate
  - two heavily-doped **n regions**: **source** and **drain** terminals



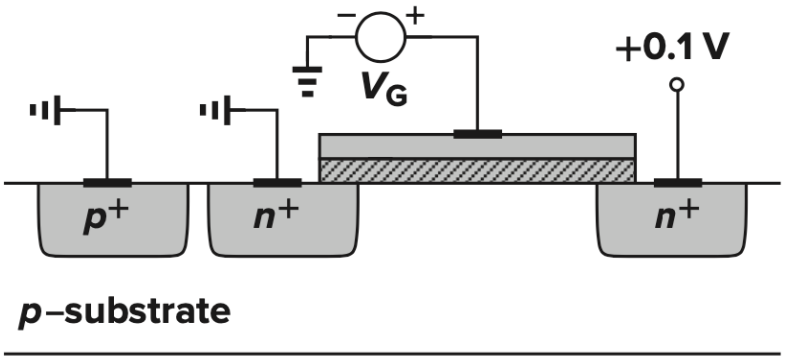
Recap: CMOS: NMOS + PMOS

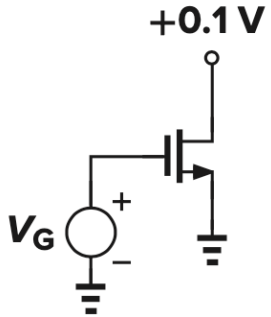


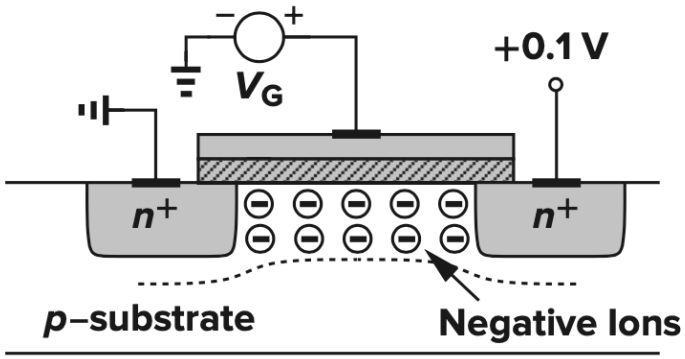
CMOS: Complementary MOS



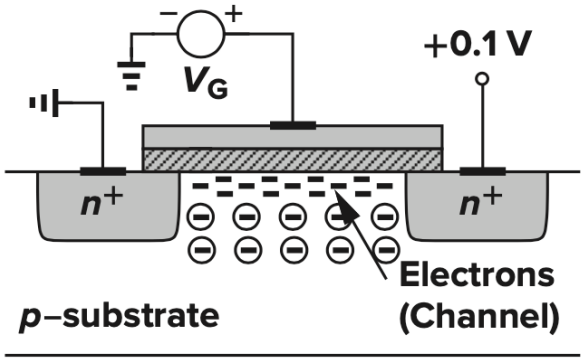
Recap: MOS threshold voltage







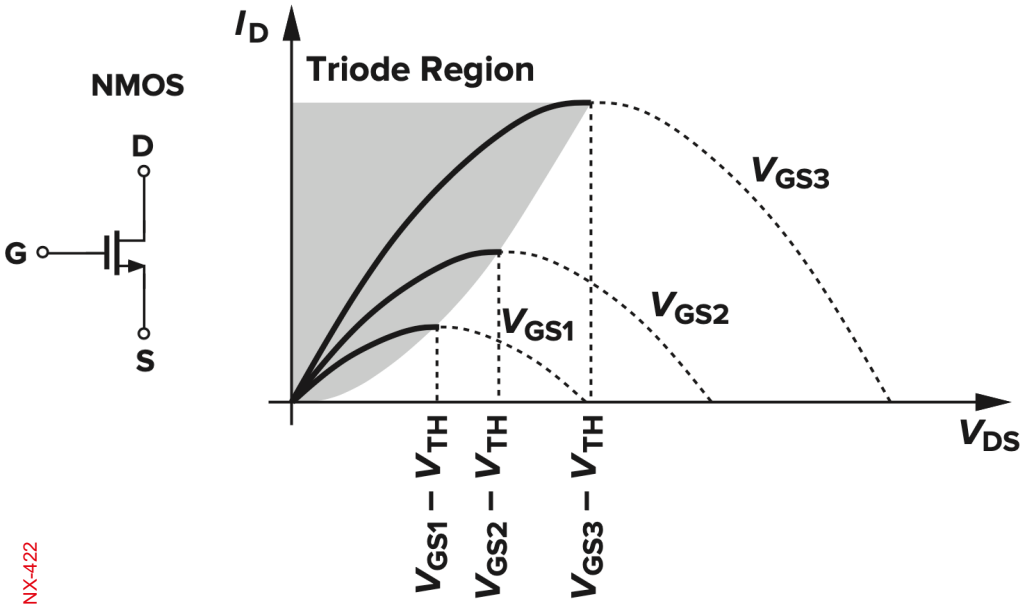
$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$



MOS in Triode

$$V_{DS} \leq V_{GS} - V_{TH}$$

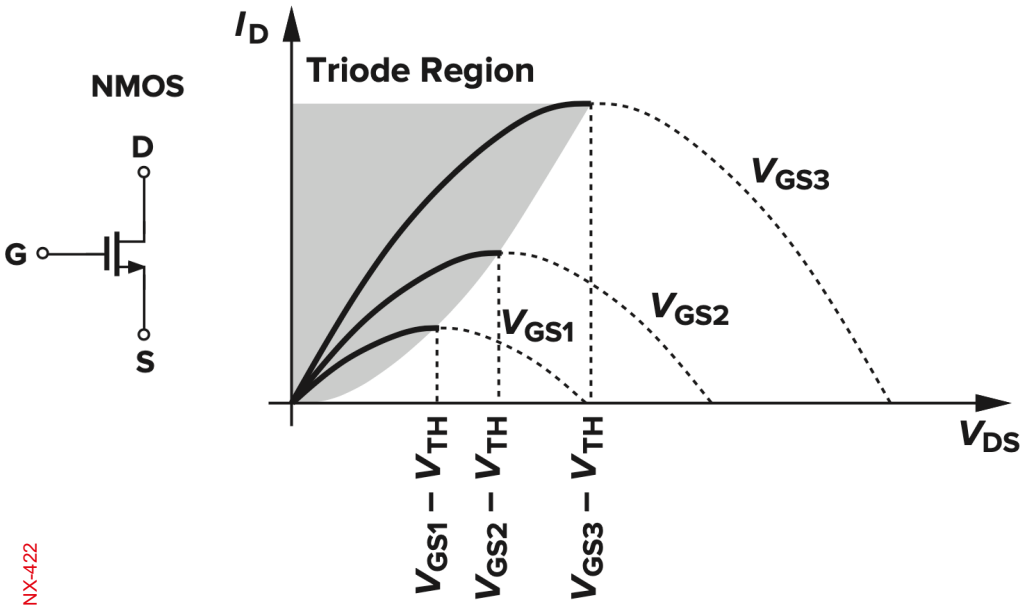
$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

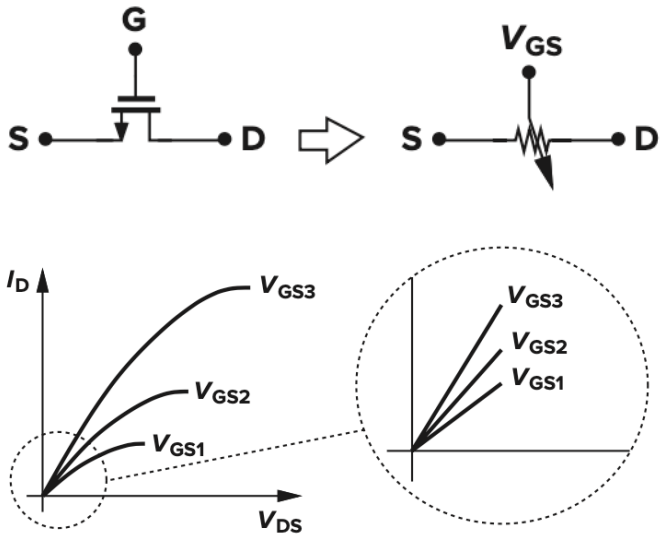


MOS in Triode

$$V_{DS} \leq V_{GS} - V_{TH}$$

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

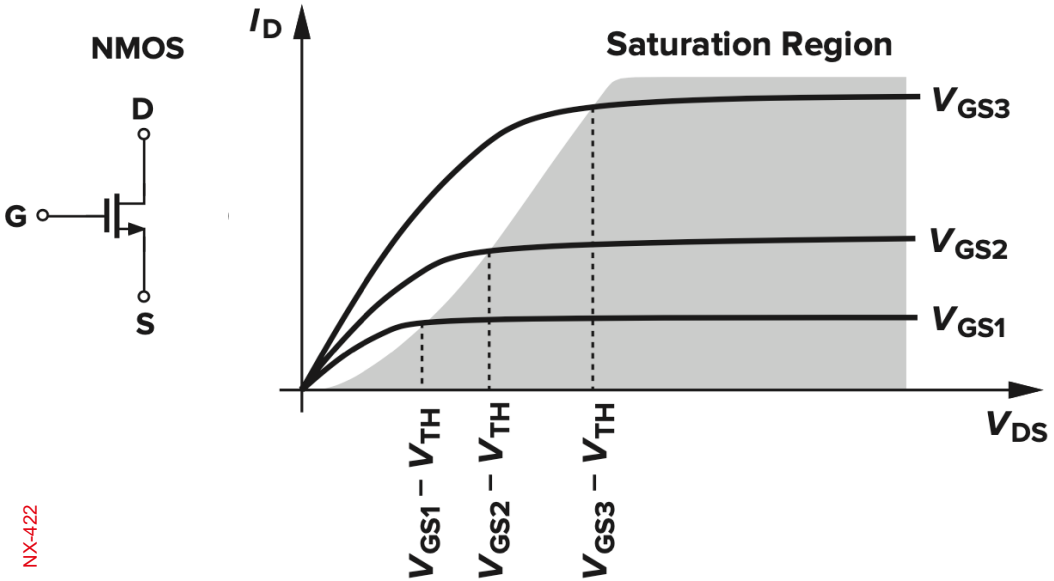




MOS in Saturation

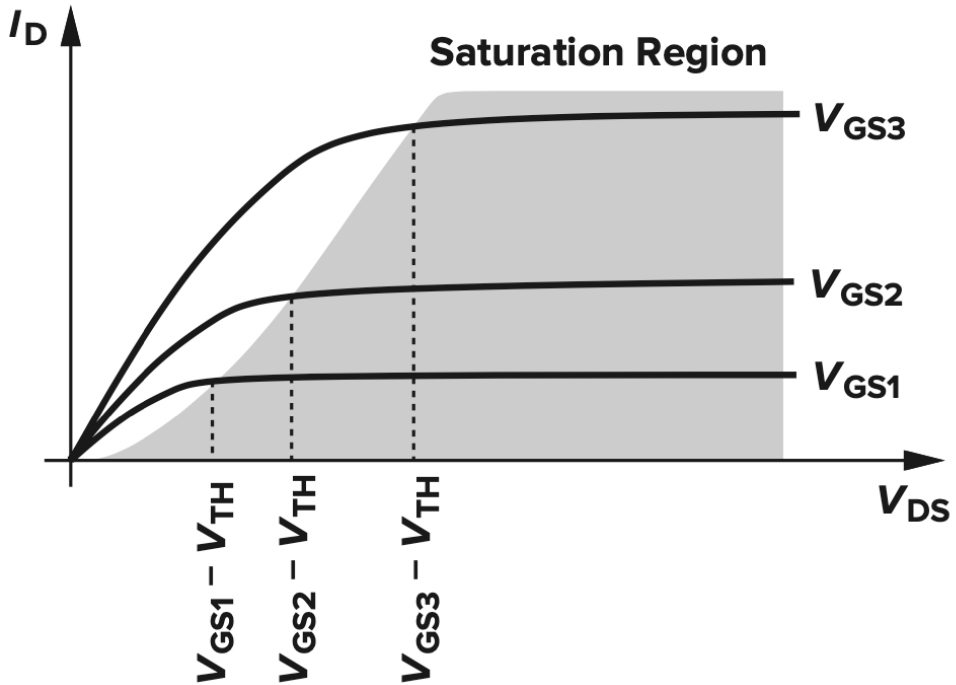
$$V_{DS} > V_{GS} - V_{TH}$$

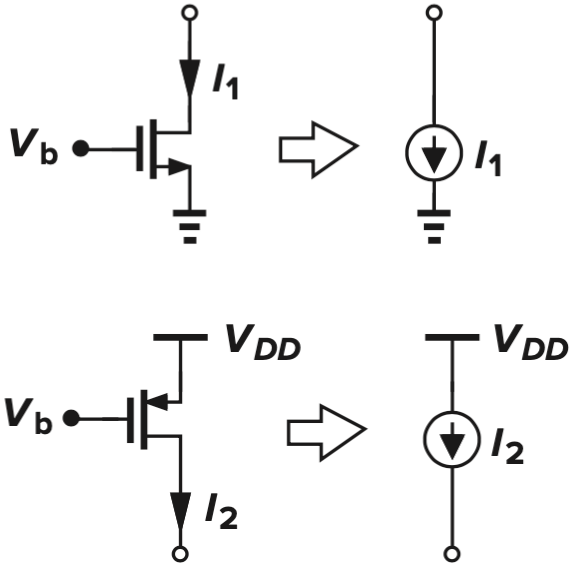
- I_D is relatively **constant with V_{DS}**, and the device operates in the "**saturation**" region.



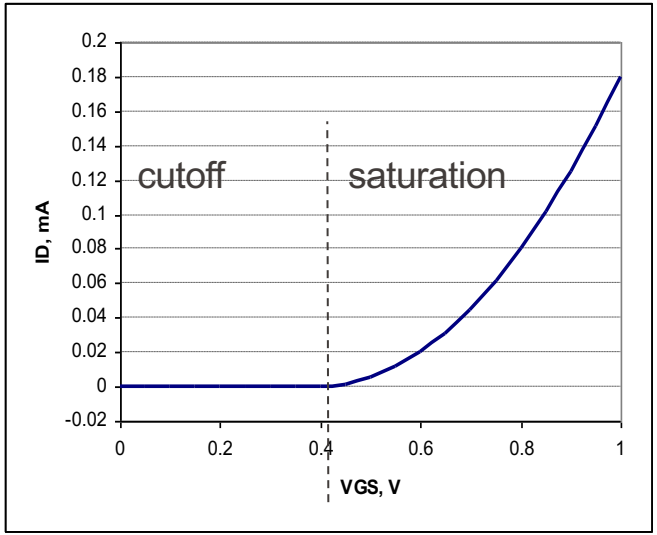
$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

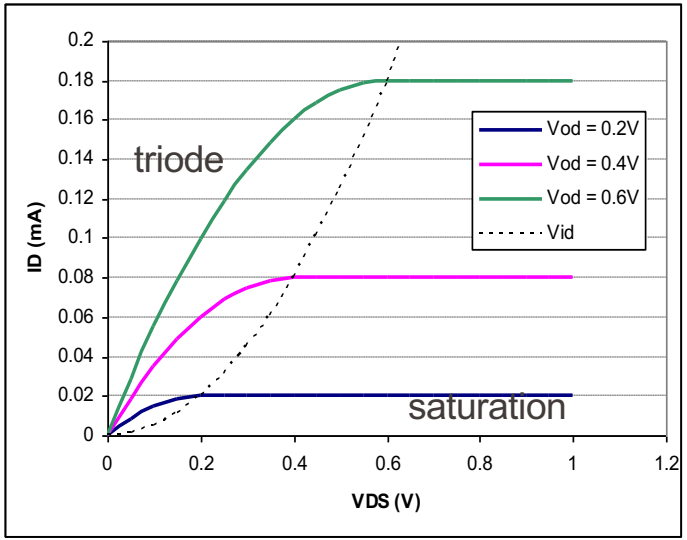
MOS Transistor Regions of Operation





MOS I/V in different regions

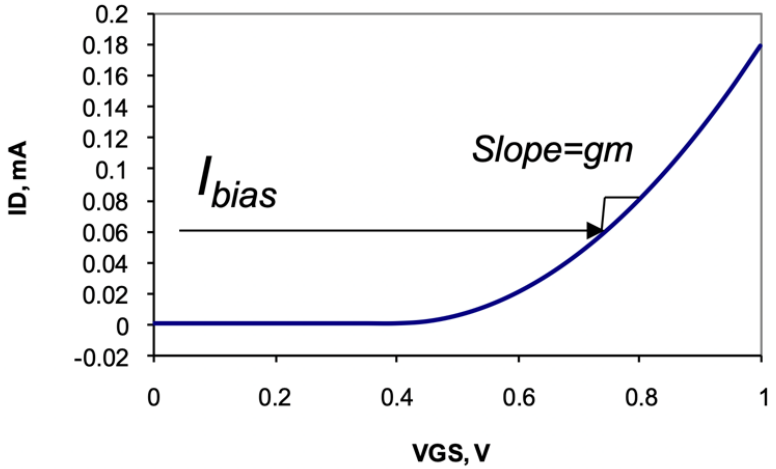




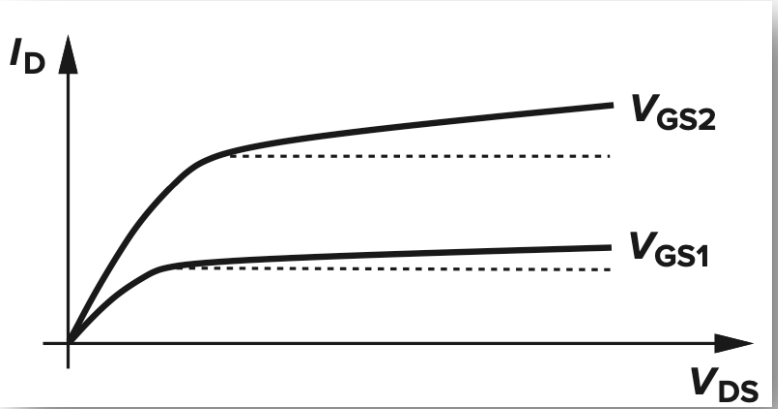
MOS transconductance (gm) in saturation

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS\ \text{const.}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})$$

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

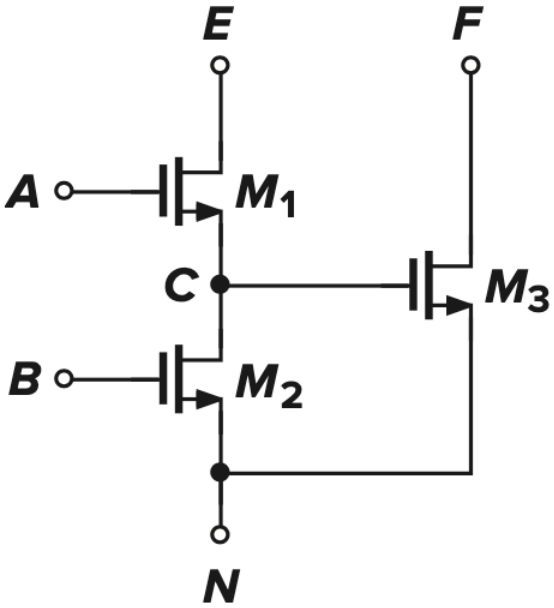


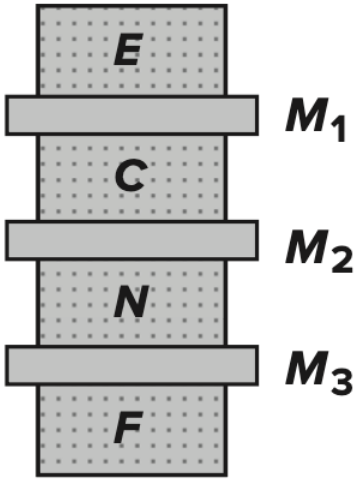
Channel-Length Modulation

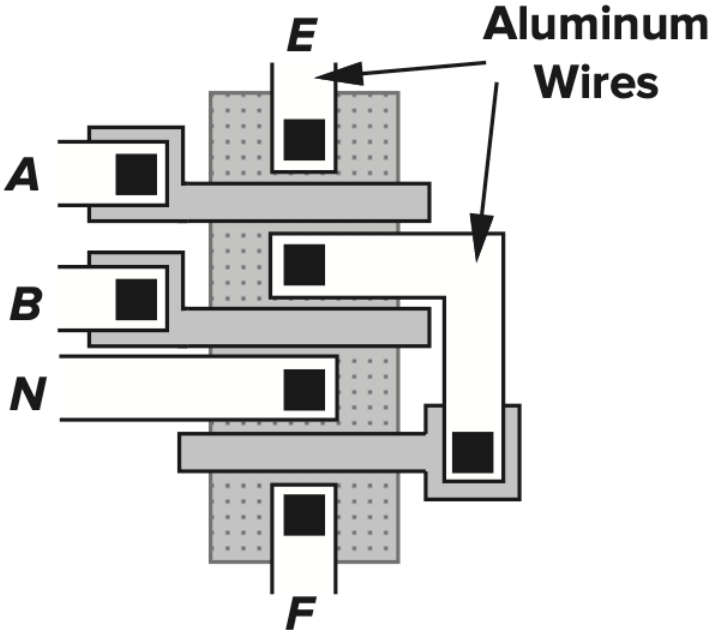


$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

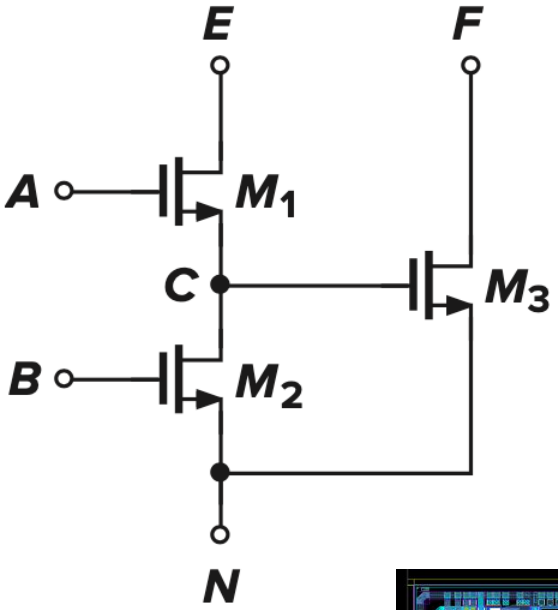
MOS Transistor Layout

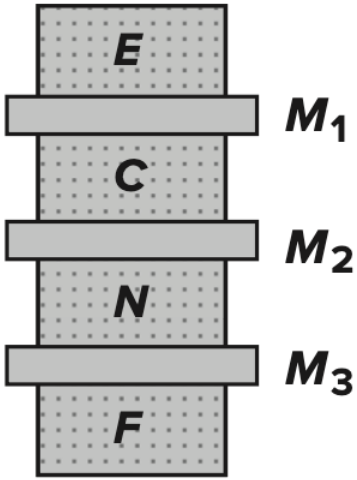


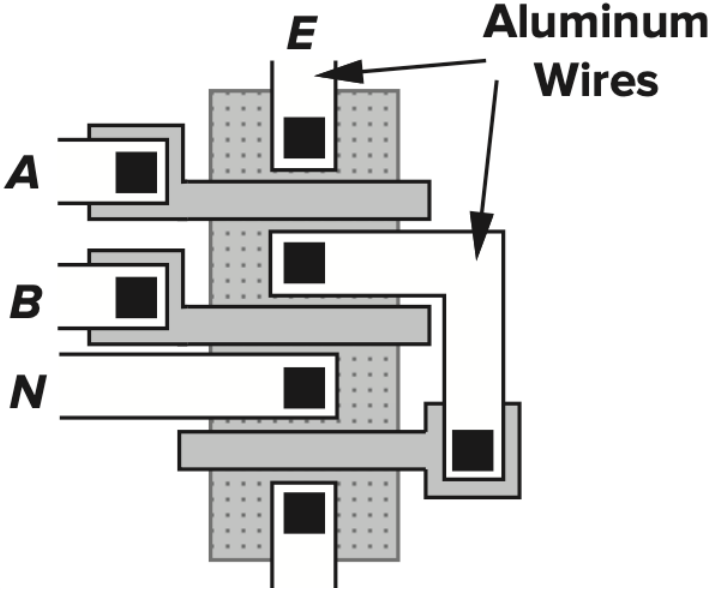


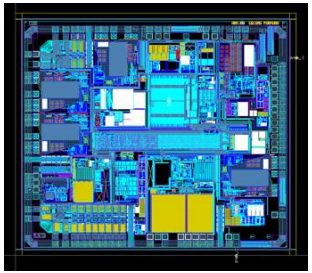


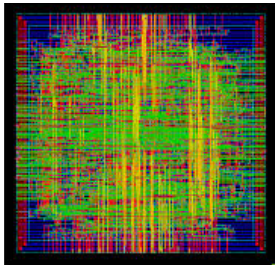
MOS Transistor Layout

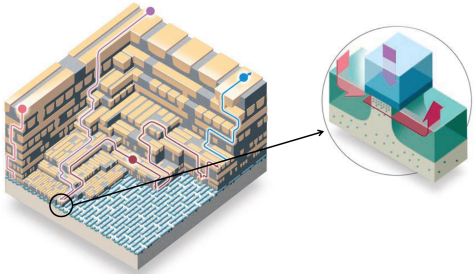




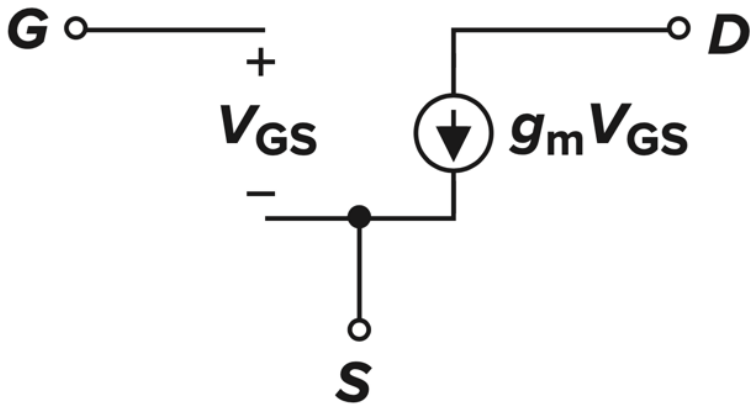




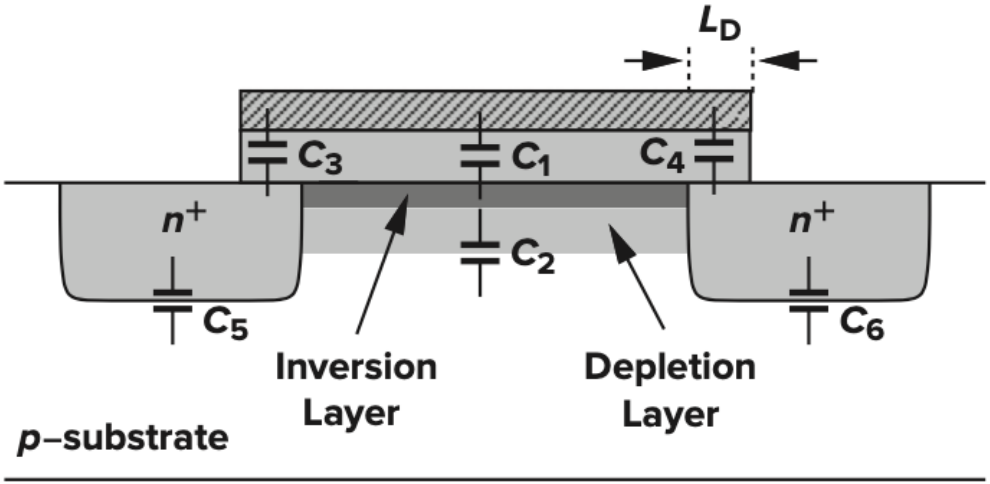


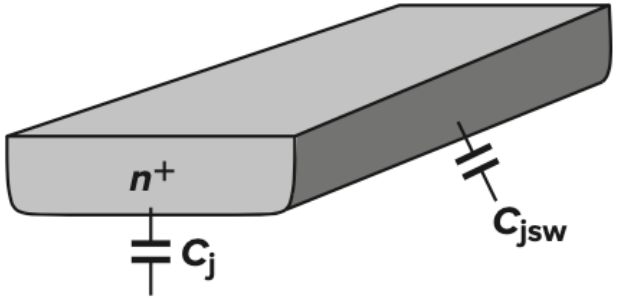


MOS Small Signal Model



MOS Parasitic Capacitances

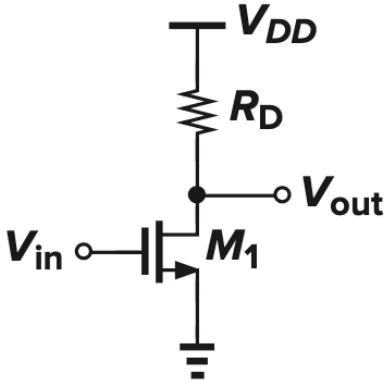


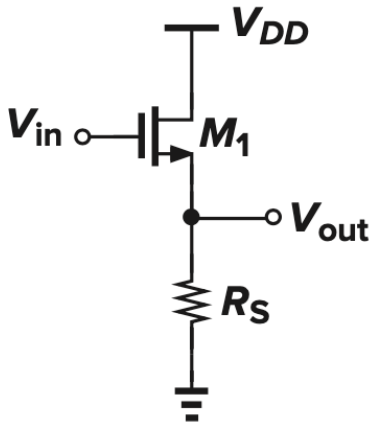


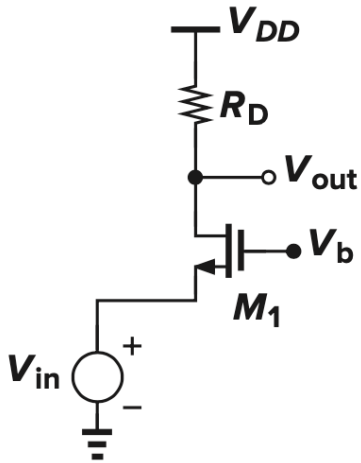
(1) the **oxide** capacitance between the **gate** and the **channel** C_1
(2) the **depletion** capacitance between the channel and the substrate C_2
(3) the capacitance due to **overlap** of the **gate** poly with **source** and **drain**, C_3 and C_4
(4) The **junction capacitance** between the **S/D** areas and the **substrate**, two components: the **bottom-plate capacitance** at the bottom of the junction $\boldsymbol{C_j}$, and the **sidewall capacitance** due to the perimeter of the junction, $\boldsymbol{C_{jsw}}$

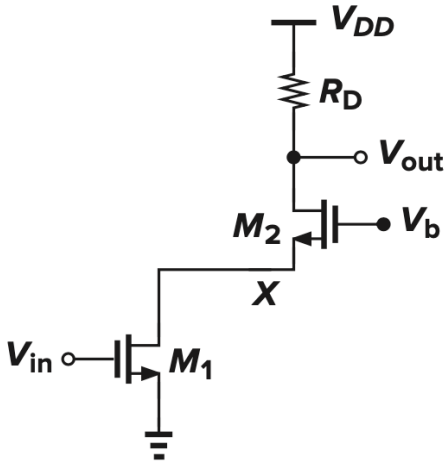
CMOS Amplifiers

Common-Source Stage	Source Follower	Common-Gate Stage	Cascode

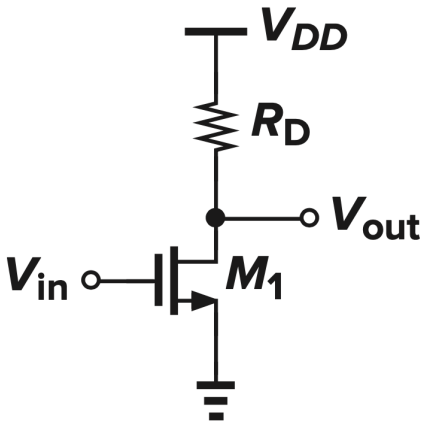




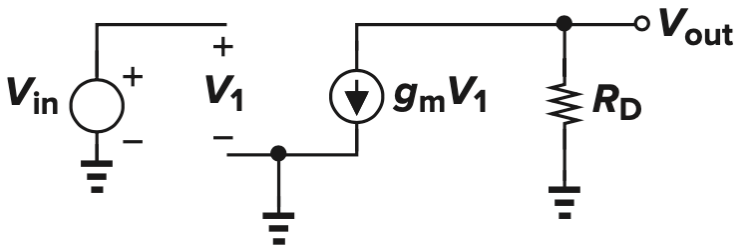




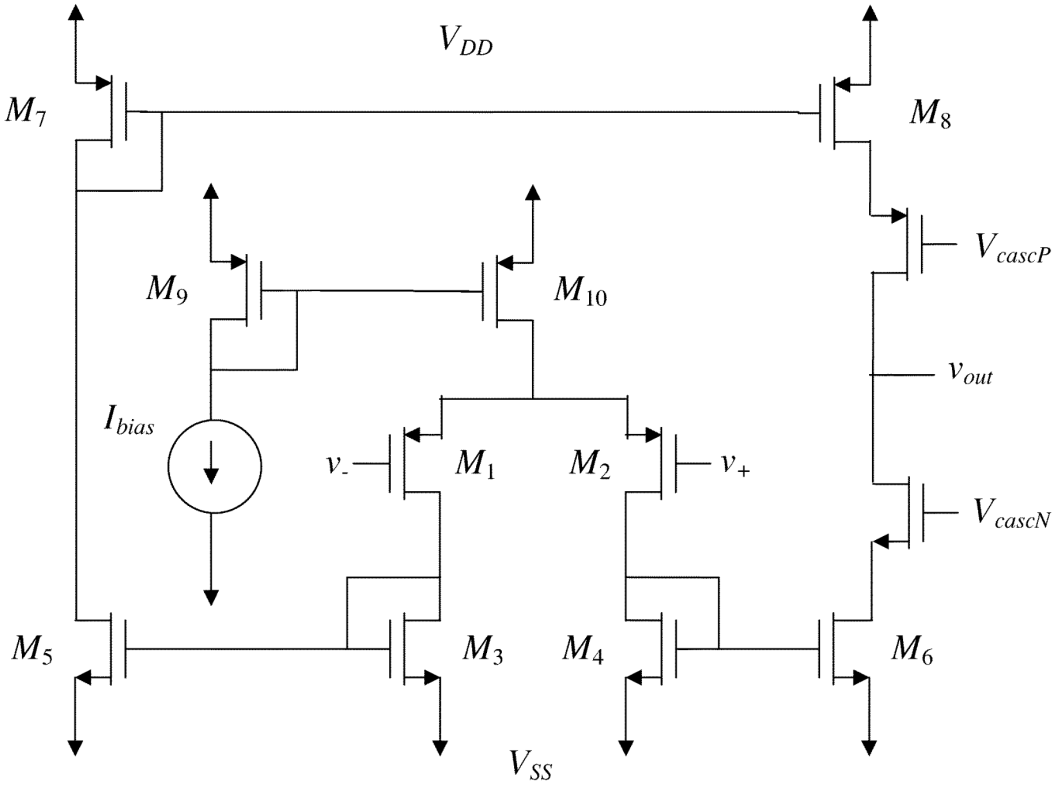
CMOS Amplifiers: Common Source



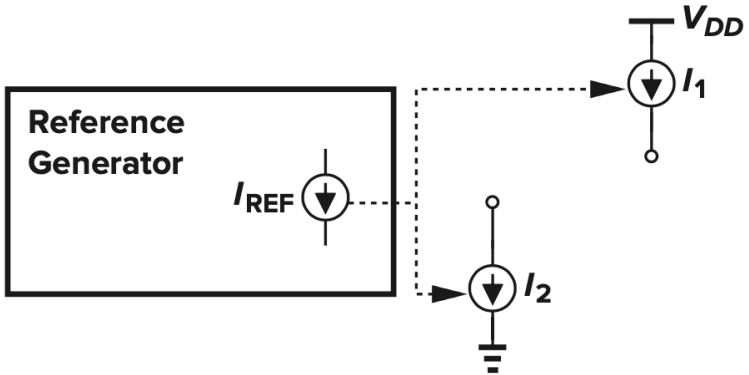
small-signal model:

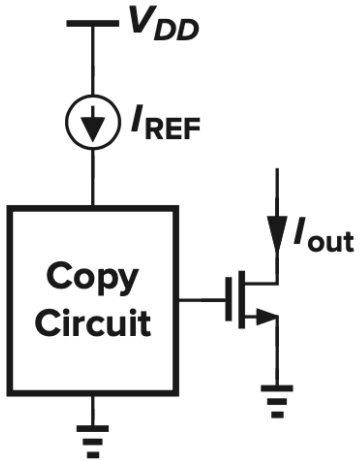


Neural Amplifier: OTA architecture

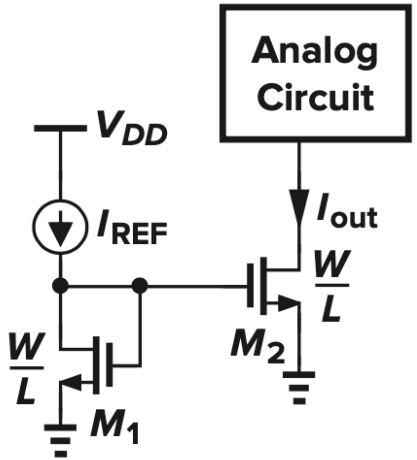


Copying current from a reference



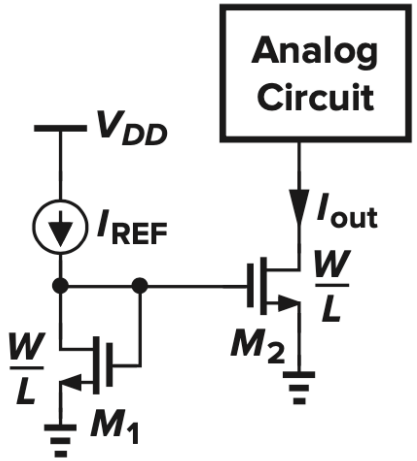


Basic current mirror circuit



(neglecting channel-length modulation)

Basic current mirror circuit



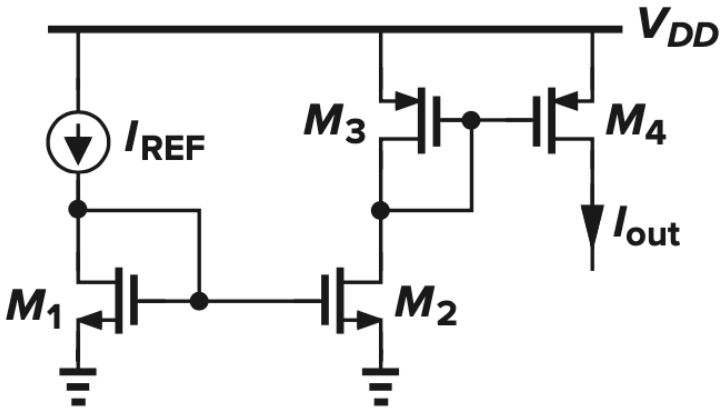
$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$$

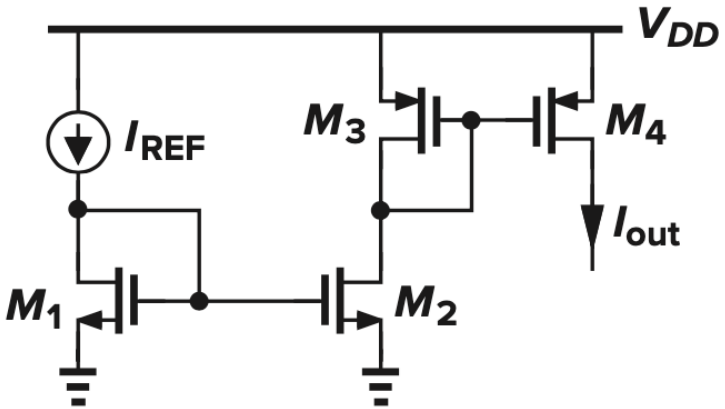
(neglecting channel-length modulation)

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

Basic current mirror circuit: example



Basic current mirror circuit: example



$$I_{D2} = I_{REF}[(W/L)_2/(W/L)_1]$$

$$I_{D4} = I_{D3} \times [(W/L)_4/(W/L)_3]$$

$$\alpha = \beta = 5 \quad \rightarrow \quad I_{REF} \text{ x } 25$$