

#### Bonding of glass

- Introduction
- Field-assisted bonding with Si
- Fusion bonding
- HF-assisted bonding
- Pressure-assisted low-temperature fusion bonding
- Application : capillary electrophoresis microchip

• References

#### Si

#### Field-assisted thermal bonding with Si

- Or: anodic bonding, electrostatic bonding
- To join glass (for example Corning #7740 = Pyrex) to Si
- Low process temperature (180-400 °C)
- Applied voltages: 200-1000 V
- Contacting surfaces need to be flat (roughness<1  $\mu$ m) and dust-free

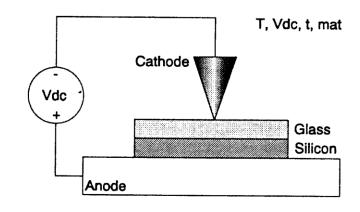


FIGURE 8.12 Principle sketch of anodic glass-to-Si bonding. Control parameters are temperature (300–400°C), bias voltage (700–1200 V), time ( $\sim$ 2′), and materials (glasses, Si, SiO<sub>2</sub>).



Thermal expansion coefficient of bonded materials need to be in the same range.

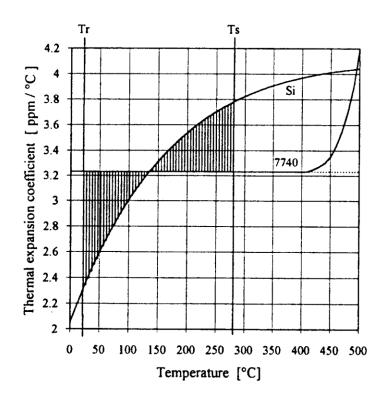


FIGURE 8.13 Thermal expansion coefficients of Si and Corning 7740 Pyrex. Tr = room temperature; Ts = seal temperature. The temperature Ts is a variable. (From Peeters, E., Process Development for 3D Silicon Microstructures with Application to Mechanical Sensor Design, Ph.D. thesis, Catholic University of Louvain, Belgium, 1994. With permission.)

#### Mechanism of anodic bonding



- At high T, glass is conductive solid electrolyte
- Bonding results from the migration of Na<sup>+</sup> (3-5 % concentration in Pyrex) toward the cathode
- This leaves **negative space charge** (bound negative charges) in the region of the glass-Si interface.
- All voltage is dropped over this region, pulling glass and Si in intimate contact
- Covalent bonds are formed between the surface atoms of the glass and the Si.
- Disadvantages:
  - High electrical field
  - One-wafer process
  - Mismatch in thermal expansion

#### 'Improved' anodic bonding



- **Ti-mesh electrode** is deposited over the glass wafer to give uniform high voltage over the interface. Bonding parameters: 400 °C, 600 V, 5 min.
- Deposition of intermediate layers of SiO<sub>2</sub> and Al to screen underlying Si from high electrical fields. Glass is bonded to the Al layer.
- Other possibility: SiO, poly-Si bilayer
- Bonding of two Si wafers with an **intermediate sputtered or evaporated borosilicate glass** (4-7  $\mu$ m). But: glass sputtering rate is very slow.
- Bonding of **2 Si wafers, each with 1 μm SiO<sub>2</sub>** is possible. Parameters: 900 °C, 30 V, 45 min

#### Thermal fusion bonding



- Based on chemical reaction between OH-groups present at the surface of the native or grown oxides covering the wafers
- Bond quality depends on temperature and surface roughness (< 4 nm).</li>
- **High bonding temperature (800 °C)** prevents the incorporation of active electronics before the bonding.
- Same technique can be applied for bonding of :
  - Oxidised Si oxidised Si
  - Bare Si bare Si
  - Oxidised Si bare Si
  - Si glass
  - Quartz quartz

#### Fusion bonding procedure



- Oxidised surface must undergo hydratation: soaking wafers in H<sub>2</sub>O<sub>2</sub>-H<sub>2</sub>SO<sub>4</sub> mixture, diluted H<sub>2</sub>SO<sub>4</sub> or boiling HNO<sub>3</sub>. This forms hydrophilic top layer of O-H bonds.
- Additional treatment in oxygen plasma enhances number of OH groups at surface.
- Wafers are rinsed in DI water and dried
- When brought into contact, direct bonding of the
   2 wafers
- High temperature anneal increases bond strength

#### Mechanism of fusion bonding



- Main reaction:  $Si - OH + OH - Si \rightarrow H_2O + Si - O - Si$
- At anneal T<300 °C, silanol</li> (Si-OH) groups give rise to hydrogen bonding.
- At 300 °C, OH-groups form water molecules, which can form water vapour voids
- Above 300 °C, water vapour disappears and strong siloxane bond (Si-O-Si) develops

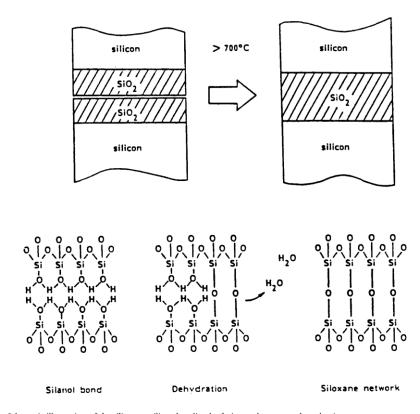


FIGURE 8.14 Schematic illustration of the silicon-to-silicon bonding by fusion and a proposed mechanism.

## Intermediate thin-layer thermal glass bonding

- LPCVD phosphosilicate glass (PSG) (1-2  $\mu$ m) can be used for Si to Si wafer bonding. Anneal at 1100 °C for 30 minutes necessary.
- Low temperature sealing glasses 'frits' exist.
  - Sealing temperatures: 415-650 °C.
  - Glass can be spinned, sprayed, screen-printed.
  - Preglazing to get rid of organic residues
- Spin-on-glass (SOG) (Si(OH) $_x$  with 2<x<4)
  - 50 nm thick film is baked at 250 °C for 1 hr.
  - Annealing for 1 hr at 1150 °C to sinter

#### HF-assisted bonding



- Room temperature bonding process
- HF (C ≥ 0.1 %) is applied in between 2 glass or SiO<sub>2</sub> wafers.
- Pressure is applied (~1 MPa)
- Mechanism: formation of intermediate bonding layer.
- Advantages:
  - no temperature induced stress
  - no degradation of metal leads (Au-Cr, Al,..) and IC 's.
  - bonding strengths of 5-10 MPa

#### HF-assisted bonding



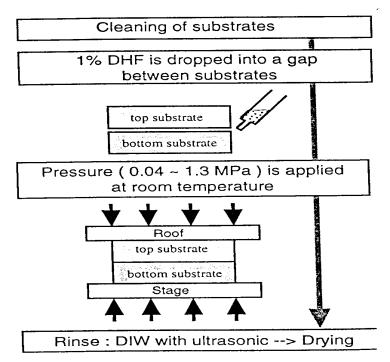
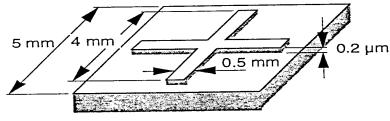


Fig.1 Procedure of HF-bonding

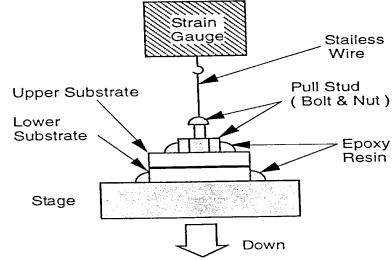
- Substrate cleaning: acetone, methanol,
   H<sub>2</sub>SO<sub>4</sub>+H<sub>2</sub>O<sub>2</sub>
- 1% HF etching to remove surface layer (5 nm)
- 1% diluted HF (DHF) is dropped in gap
- 18 hours of pressurised bonding

#### HF assisted bonding





(a) Schematic of test-chip



(b) Schematic of the tensile test equipment

Fig.2 Set-up for evaluation of bond strength

Bond quality is evaluated by bond strength measurements

#### HF assisted bonding



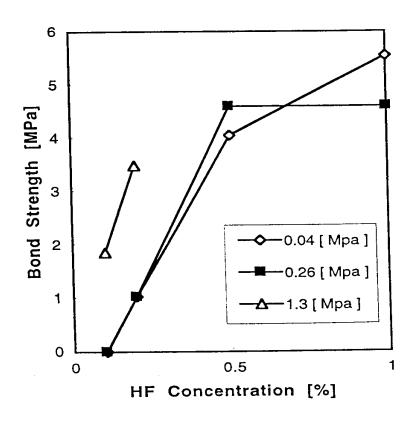


Fig.3 Relationship between HF concentration and bond strength

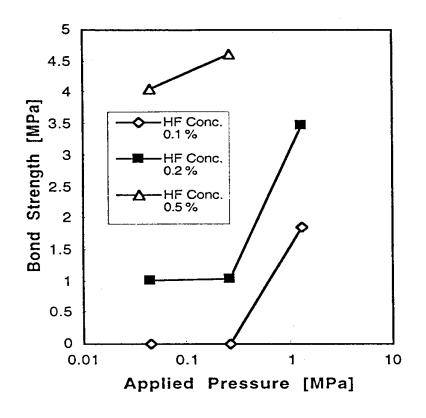
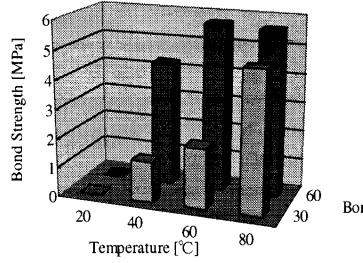


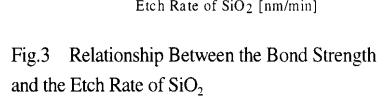
Fig.4 Relationship between applied pressure and bond strength

#### HF assisted bonding

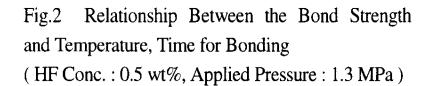


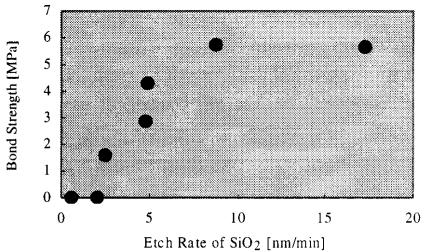


Bonding Time [min]



(Bonding Period: 1 hour, Applied Pressure: 1.3 MPa)





#### **EPFL**

## Pressure-assisted low-temperature fusion bonding

Low temperature bonding process (100-200 °C)

Cleaning of the substrates (no HF)

Pressure is applied (~10 MPa)

Mechanism:

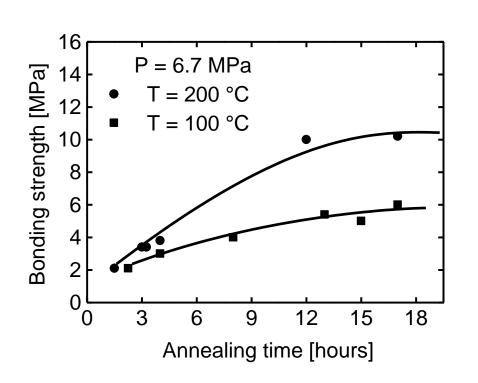
$$AdvaintaQH + OH - Si \rightarrow Si - O - Si + H_2O$$

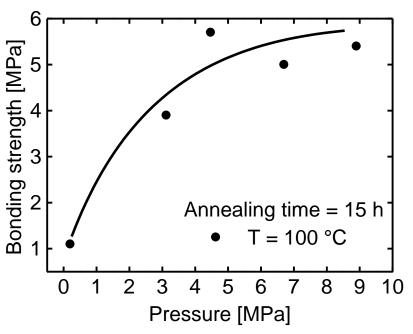
- no temperature induced stress
- no degradation of metal leads (Au-Cr, Al,..) and IC 's.
- bonding strengths of 5-10 MPa
- no HF

#### **EPFL**

## Pressure-assisted low-temperature fusion bonding

Measurement of bonding strength





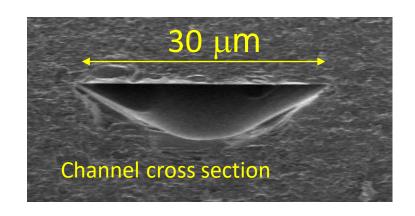
#### 2021

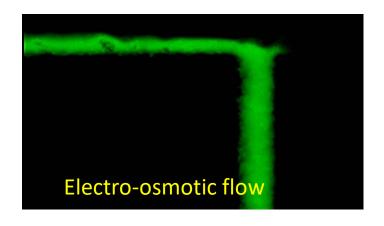
# Prof. M.A.M. Gijs, Dr. V.K. Parashar, Swiss Federal Institute of Technology Lausanne (EPFL)

#### Capillary electrophoresis chip









#### Separation principle

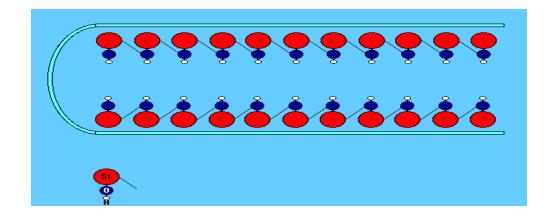


- Electrophoresis : different transport velocity of molecules in a liquid in an electric field, based on the **different charge/mass ratio** of the various biomolecules.
- This principle can be translated to the capillary / microchip format:
  - Capillary : hollow quartz tube (inner  $\emptyset$  25-100  $\mu$ m, length 0.1-1 m)
  - **Microchip**: microchannel realised in glass or quartz wafers by microstructuring and bonding techniques

#### Electro-osmotic flow (EOF) (i)

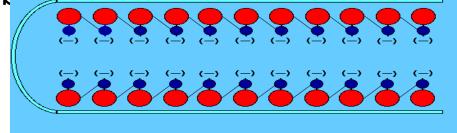


• Capillary is made of fused silica (SiO<sub>2</sub>)



• Filling the channel with buffer solution disociates hydroxyl groups, leaving negative charge on inside

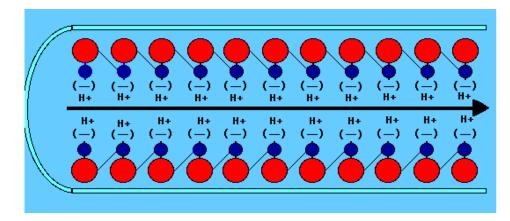




#### Electro-osmotic flow (EOF) (ii)



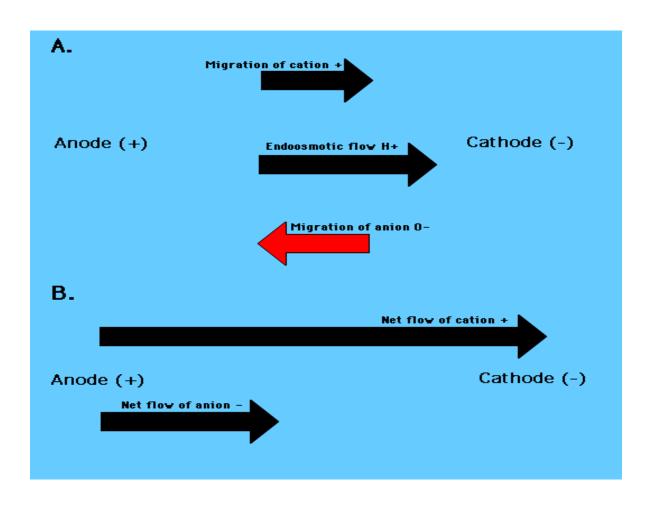
 Applying a voltage across the capillary causes hydrogen ion flow, resulting in EOF or bulk flow



- Turning off the voltage stops the EOF
- EOF mobility adds to electrophoretic mobilities of anions (-) and cations (+)

#### Effective mobilities





• Straight, not parabolic, pumping profile.

#### Electrophoresis and electrochromatography

- Separation using EOF- pumping
  - in a hollow quartz capillary: Capillary electrophoresis (CE)
  - in a microchannel on a glass or quartz chip : Microchip electrophoresis
- Separation can be based on the different diffusion of biomolecules in a stationary phase within a capillary or microchannel ⇒
  - High Performance Liquid Chromatography (HPLC), when liquid transported by mechanical pumping
  - Capillary electro-chromatography (CEC), when liquid transported by EOF
  - microchip CEC (μCEC), when having CEC in channel on microchip

#### Connectors to the chip (i)



- PDMS (Polydimethylsiloxane) reservoirs on top of the chip
  - PDMS: moulded elastomer (silicone)
  - Contains hase and curing agent (containing Pt-hased catalyst) siloxane oligomers siloxane cross-linkers

#### Connectors to the chip (ii)



 PDMS (Polydimethylsiloxane) reservoirs on top of the chip

Three-dimensional cross-linked structure upon mixing

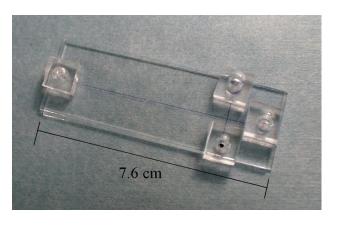
(10:1)

Metal mould



**Casted PDMS** structure

Adhesion promotor

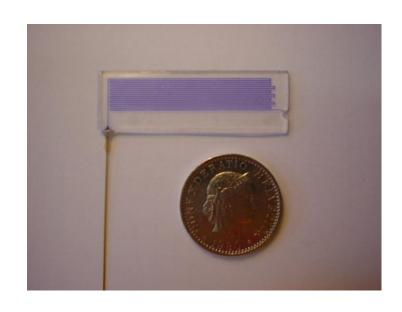


#### Connectors to the chip (iii)



#### Chip side connectors using powder blasting/gluing

- Low dead-volume connector
- Allows chip integration in commercial capillary detection system

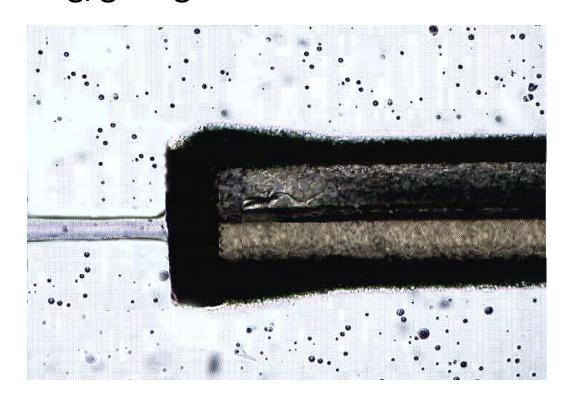




#### Connectors to the chip (iv)



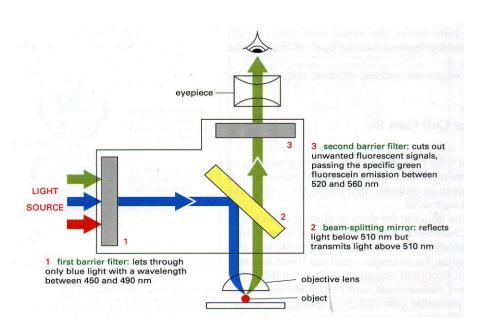
Chip/capillary side connectors using powder blasting/gluing

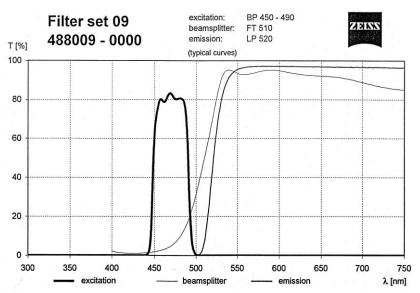


# PFL

#### Chip detection platform (i)

#### Fluorescent detection using an inverted microscope

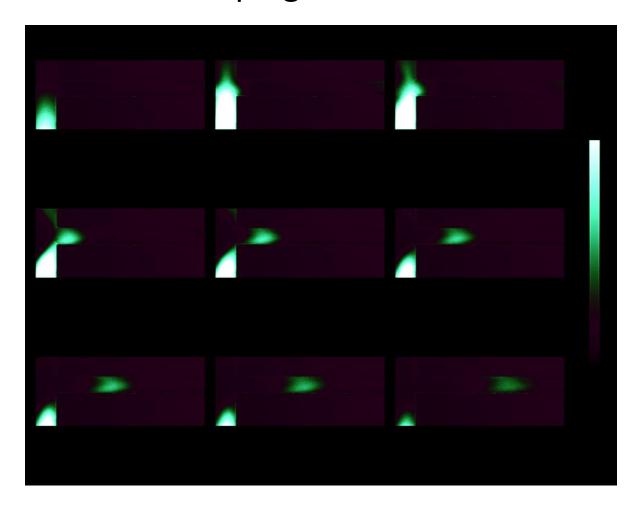




#### Chip detection platform (ii)

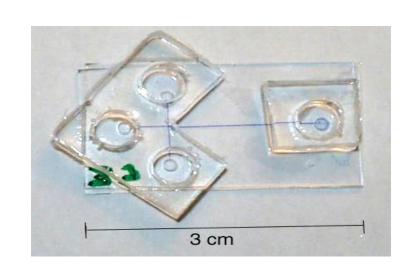


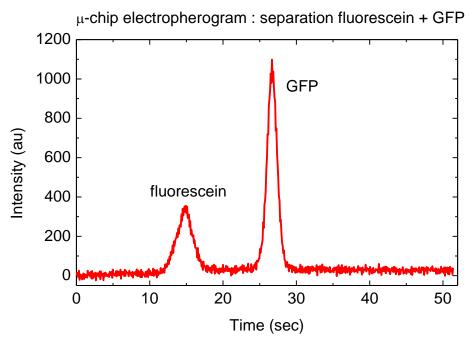
#### Injection of fluorescent plug



#### EPFL

## Fluorescein – GFP separation electropherogram



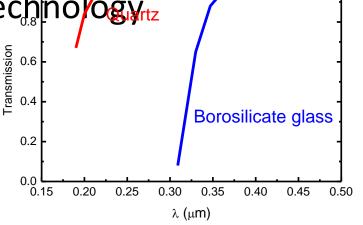


#### Towards a universal detection scheme



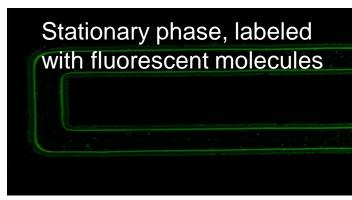
- Only fluorescently labeled molecules can be visualised by fluorescence
- All proteins absorb in UV → universal means for detection
- Also glass absorbs in UV

• Solution : use quartz for microchip fabrication → develop quartz technology.



### μ-chip chromatography using sol-gel stationary phases • Inject a liquid solution in the channel

- Let it polymerise to a stationary phase, which covers the channel walls
- Inject a liquid mobile phase containing the molecules to be separated
- Bio-molecules will selectively adsorb/desorb on the formed stationary phase → chromatography application
- Driving force for the flow is electrosmosis  $\rightarrow \mu$ -chip Capillary Electro Chromatography



#### References



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