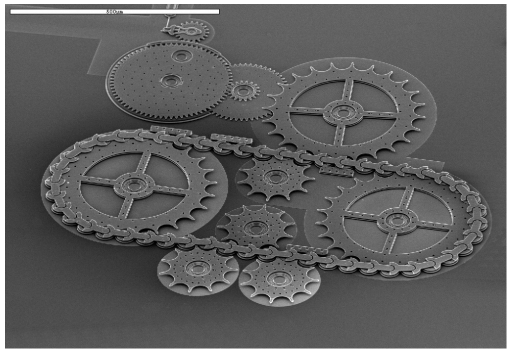
Microfabrication Process Flow

Preparing a process flow

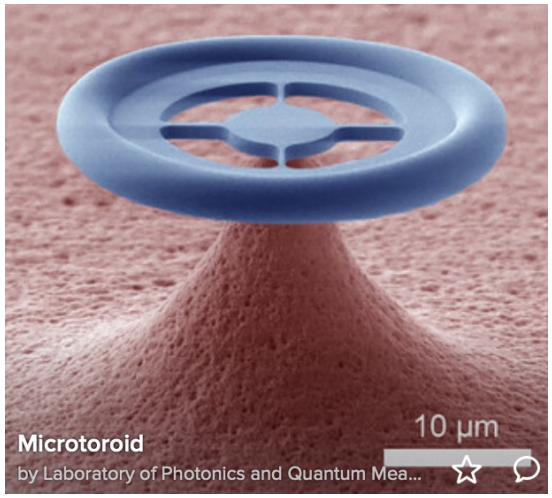
SP Lacour – 25.9.24

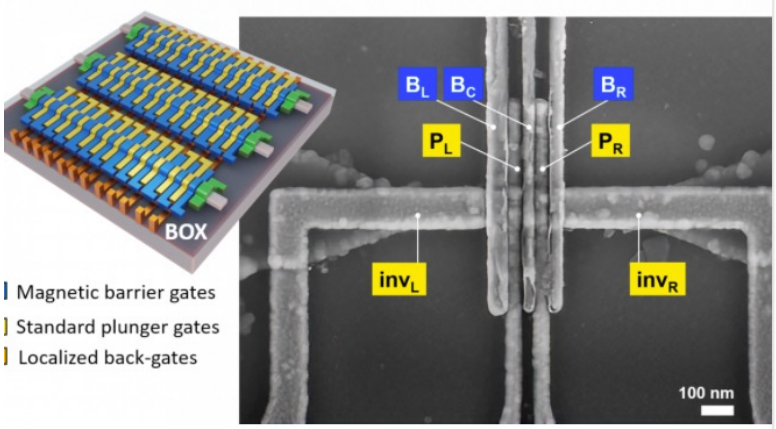
Ecole Polytechnique Fédérale de Lausanne

Examples of Micromachined devices

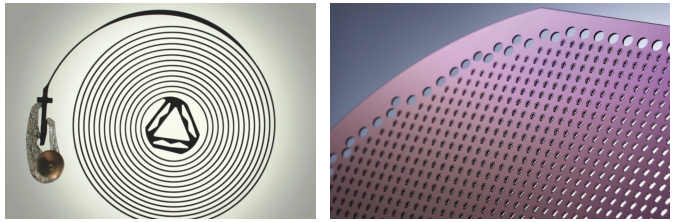


Sandia silicon microchain, 2002





Nanolab, EPFL , Quantum dots Nanowires, 2023

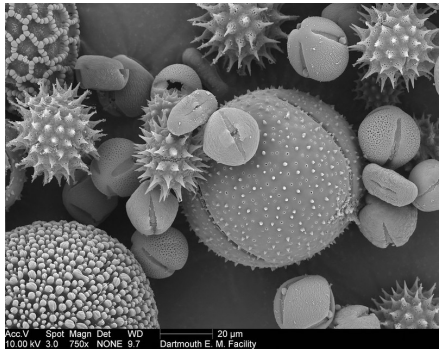


Patek Philippe – 2016
silicon regulating organ & reset mechanism

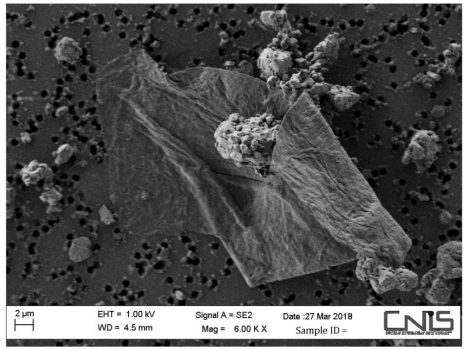
Neurosoft
Bioelectronics
soft ECoG, 2023

Cleanroom
a highly controlled environment

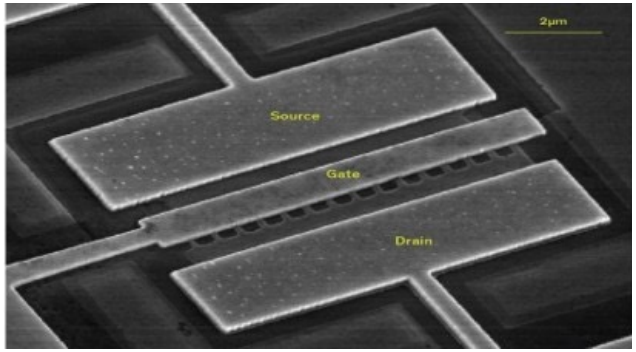
- **a controlled particle count**
  - designed to minimise airborne particles (dust, skin flakes, fibers) that can interfere with the manufacturing process



pollen



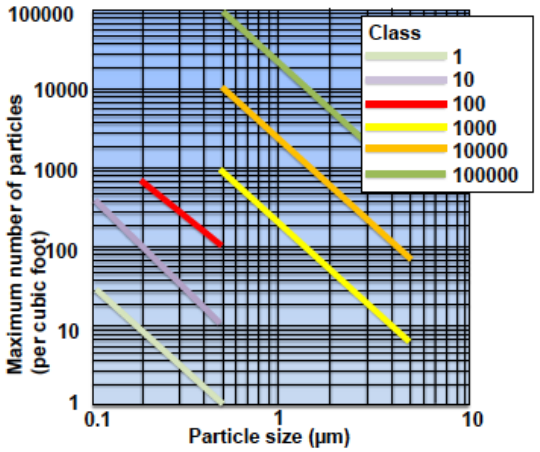
skin dust



transistor

Cleanroom
a highly controlled environment

- **Classification ISO**
  - ISO class 1: 10 particles per m^3 (particles > 0.1µm)
  - ISO class 5: 100'000 particles per m^3 (particles > 0.1µm)



Class	>0.1 um	>0.2 um	>0.3 um	>0.5 um	>1 um	>5 um	FED STD 209E equivalent
ISO 1	10	2					
ISO 2	100	24	10	4			
ISO 3	1,000	237	102	35	8		Class 1
ISO 4	10,000	2,370	1,020	352	83		Class 10
ISO 5	100,000	23,700	10,200	3,520	832	29	Class 100
ISO 6	1,000,000	237,000	102,000	35,200	8,320	293	Class 1,000
ISO 7				352,000	83,200	2,930	Class 10,000
ISO 8				3,520,000	832,000	29,300	Class 100,000
ISO 9				35,200,000	8,320,000	293,000	Room Air

Cleanroom
a highly controlled environment

- **air filtration**
  - HEPA (High Efficiency Particulate Air) or ULPA (Ultra-low Penetration Air) filters
  - constant air flow: 20 to 600 air changes per hours
  - positive air pressure

- **temperature and humidity control**
  - temperature: 20 – 24°C (stability of photolithography)
  - humidity: 40 – 60% RH

- **surface cleanliness**
  - surfaces, equipment, tools designed to minimise particle shedding
  - stainless steel, coated plastics, lint-free cloths

Cleanroom
a highly controlled environment

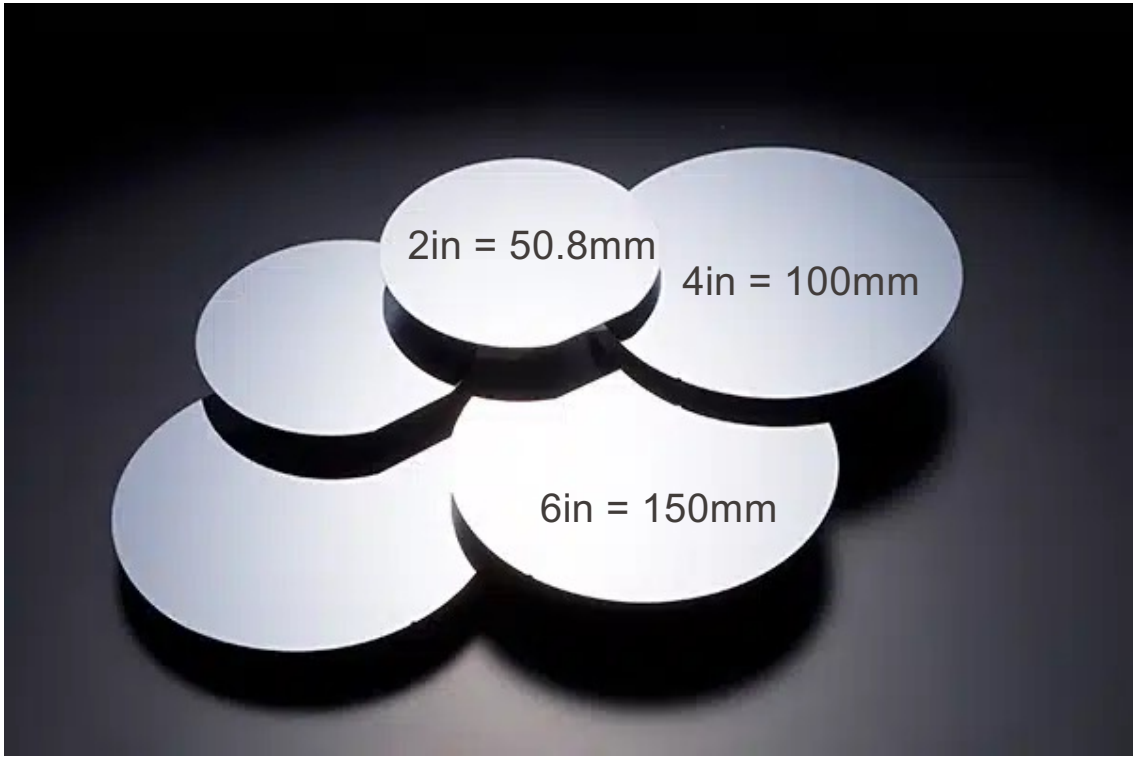
- **personnel and protective clothing**
  - human presense is a large source of contamination!

1. full-body overall
2. gloves
3. goggles
4. mask
5. shoe covers

  - gowning room

Materials

- **substrates**
  - Silicon, GaAS, glass
  - *polymers*
- Si wafers
  - diameter: 2in – 18in
  - *12in: modern semicond. fab.*
  - thickness: 275 - 1’000 µm
  - flatness
  - orientation flat and notch
  - *(100) or (111) orientation*



Materials

- **thin-films**
  - metals
  - insulators
- deposition
  - evaporation
  - sputtering
  - ALD
  - CDV…
- etching

sputterer

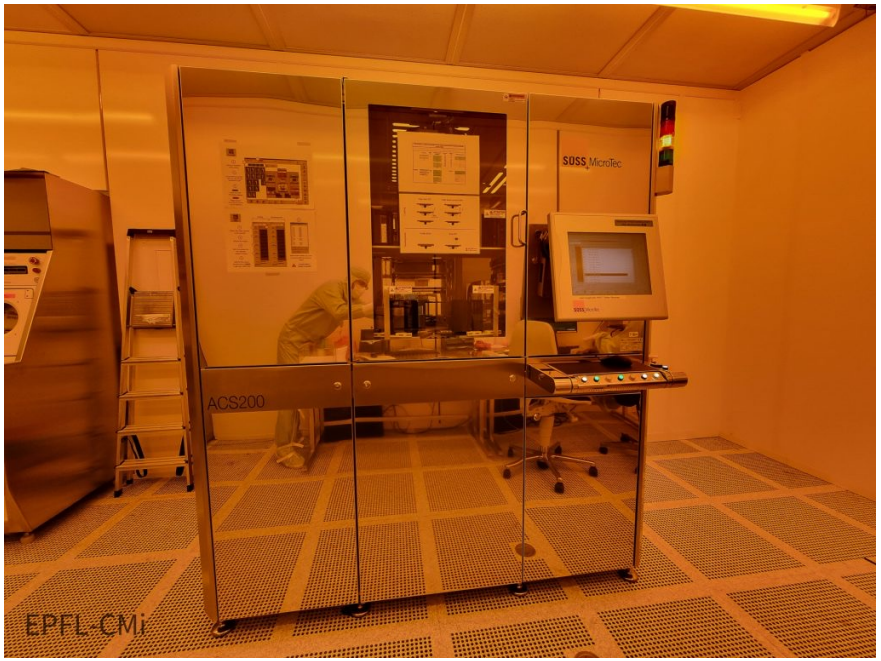
evaporator

Materials

- **photoresists**
  - positive
  - negative

- parameters
  - Thickness range: 0.5 - 2 µm (thin)
  - Thickness range: 2 - 100 µm (thick)
  - spin-coating speed

  - DUV to UV sensitive
  - E-beam and X-ray



coater - developper

The process flow

- **detailed sequence of steps and techniques** to fabricate a device

→ a roadmap outlining how various fabrication processing are combined to create the desired features on a silicon wafer

materials

instruments and tools

result

Ingrédients

Nombre de personnes - 8 +

500 g	**de farine pour tresse** ou de farine blanche
1.5 c.c.	**de sel**
1 c.c.	**de sucre**
0.5 cube	**de levure** (env. 20 g)
60 g	**de beurre**
3 dl	**de lait** (300 g)
1	**jaune d'œuf**
1 c.s.	**de lait** ou de crème

Comment c'est fait:

Mélanger dans un grand bol farine, sel et sucre. Émietter la levure, incorporer. Ajouter le beurre en dés et le lait, mélanger, pétrir en pâte molle et lisse. Laisser doubler de volume env. 2 h à couvert à température ambiante.

Diviser la pâte en deux portions, façonner chacune en un rouleau d'env. 70 cm de long aux extrémités plus fines. Tresser, déposer sur une plaque chemisée de papier cuisson. Mélanger le jaune d'œuf et le lait, en dorer la tresse, laisser lever encore env. 30 minutes. Préchauffer le four à 200°C. Dorer encore à l'œuf au lait.

Cuisson: env. 35 min dans la moitié inférieure du four.

Profil nutritionnel par 100 g:

kcal	lip	glu	pro
311	9g	46g	10g

quantities, time, temperature…

The process flow

- **Recipe:** To define the roadmap.
- **Repeatability**: To ensure that devices are fabricated consistently with high yield.
- **Optimization**: To minimize defects and improve performance.
- **Documentation**: Provides a clear record of every step and parameter, essential for troubleshooting and improving processes.

How to define a process flow?

1. **Define the objectives**
   - what is the final **device**?
     - a transistor, MEMS device, sensor or I.C., etc
   - understand the **key features** and **functional** requirements of the device
     - materials, structure and performance
   - identify the required **layers and materials**
     - silicon, metal, insulation
     - layer thicknesses

How to define a process flow?

2. Break down the device structure

- Analyze the device structure. What are the important regions (e.g., active areas, gates, interconnects)?
- Identify which features need patterning, doping, deposition, or etching.
- Divide the process into layers
  - Start with the substrate (e.g., silicon wafer) and think about each layer that needs to be added or patterned, such as insulating layers, conductive layers, or doped regions.

How to define a process flow?

3. List the major steps

- Wafer preparation: Cleaning or polishing the wafer.
- Oxidation: Growing oxide layers if needed.
- Deposition: Adding thin films of materials (e.g., silicon dioxide, polysilicon, metals).
- Patterning: Using photolithography to define regions for etching or doping.
- Etching: Removing material to create the desired features.
- Doping: Introducing impurities to alter electrical properties.
- Metallization: Adding metal layers for interconnections.
- Packaging: Preparing the device for final use (cutting, bonding, sealing).

Preparation of a process flow

- template from the Cmi

- 2 examples
  - Si mold
  - Flexible electrodes