

COMPOSANTS SEMI-CONDUCTEURS

XIII) Solutions S13

P.A. Besse

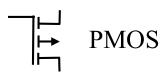
EPFL



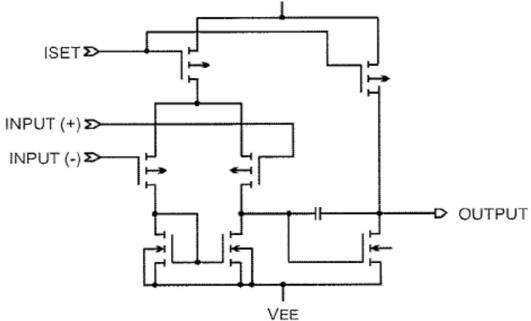
Exercice 13.1 A











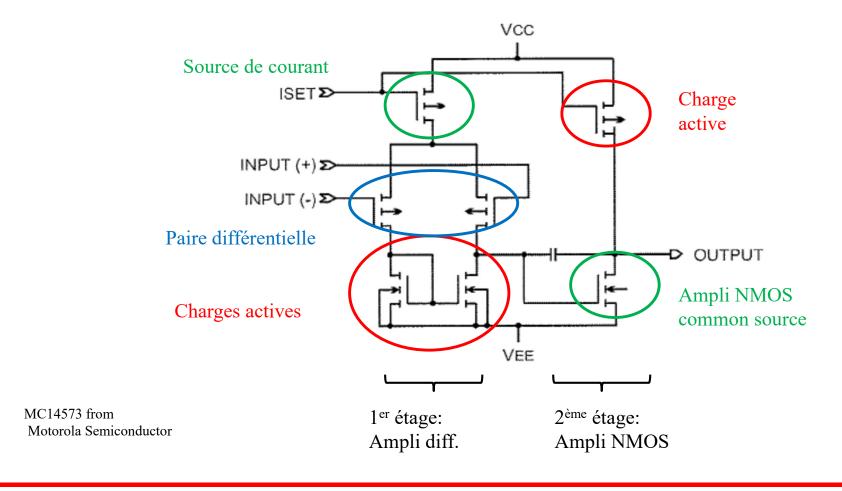
MC14573 from Motorola Semiconductor



Exercice 13.1 A: Solution Op-Amp



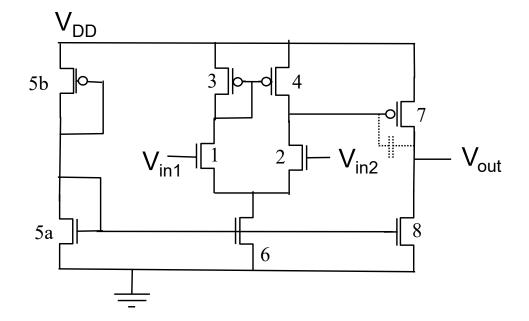
OpAmp deux étages mais basé sur une entrée PMOS



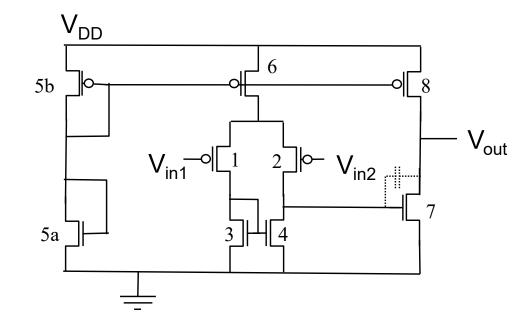


Differential amplifier

NMOS inputs



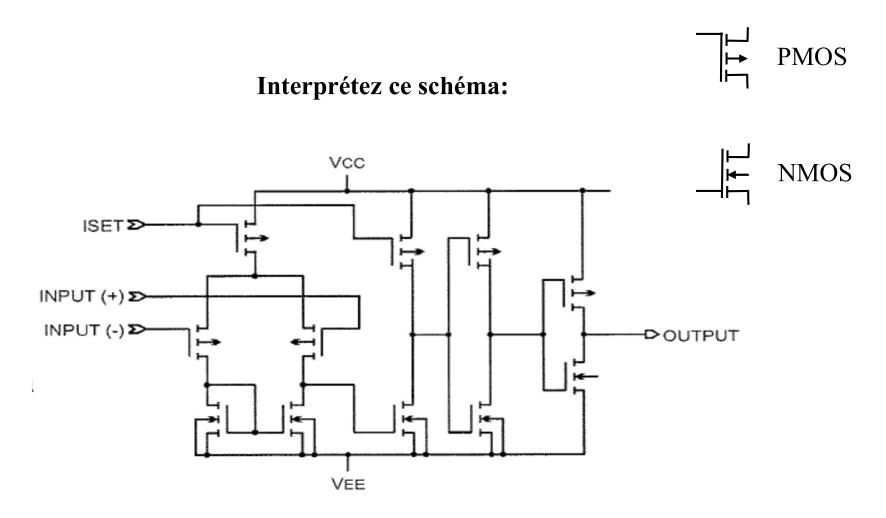
PMOS inputs





Exercice 13.1 B





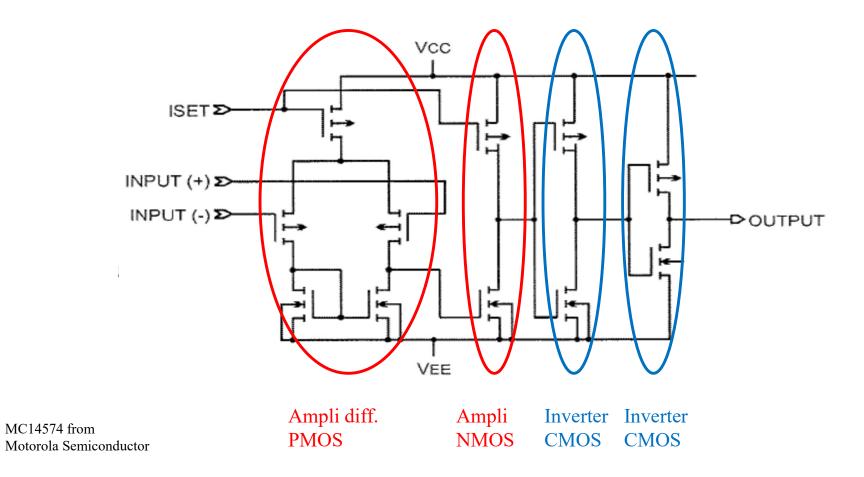
MC14574 from Motorola Semiconductor



Exercice 13.1 B



Comparateur = OpAmp 2 étages et 2 inverseurs en amplificateurs





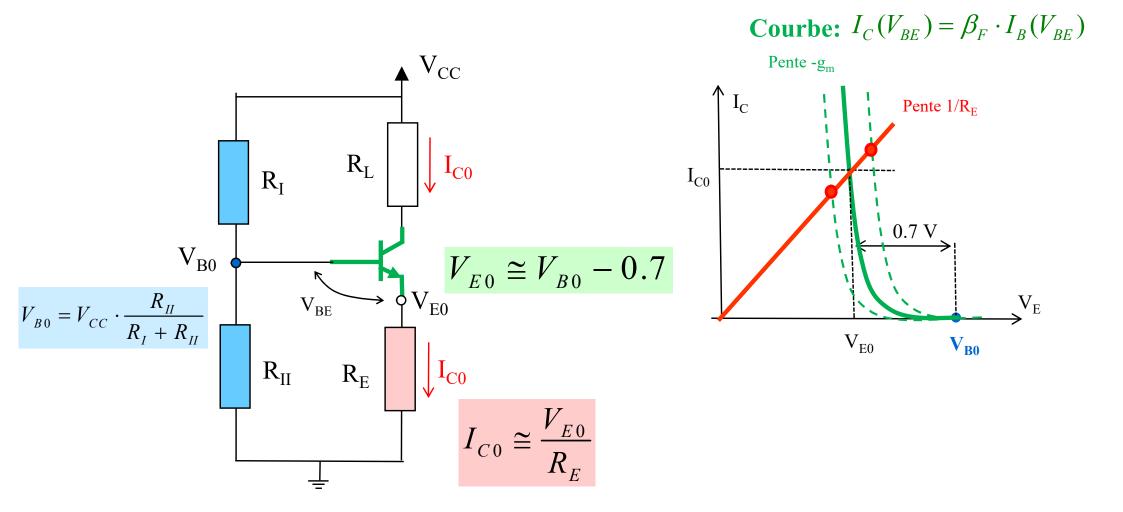
Exercice E13.2: Ampli de tension avec NMOS



Utilisez un NMOS comme ampli de tension. Inspirez-vous du chapitre 7 sur les BJT. Remplacez le transistor bipolaire par un NMOS!



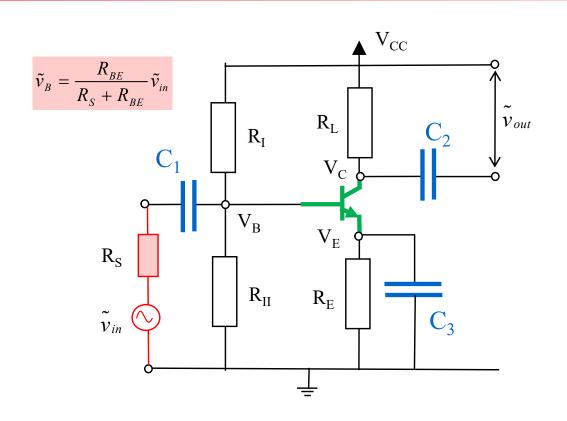
BIPOLAIRE npn: point de travail

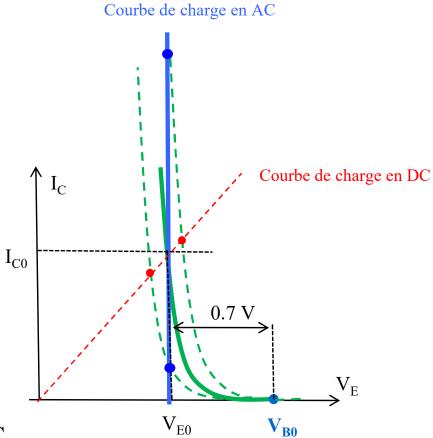


R_E assure la stabilité du courant de bias I_{C0}.



BIPOLAIRE npn Couplage capacitif



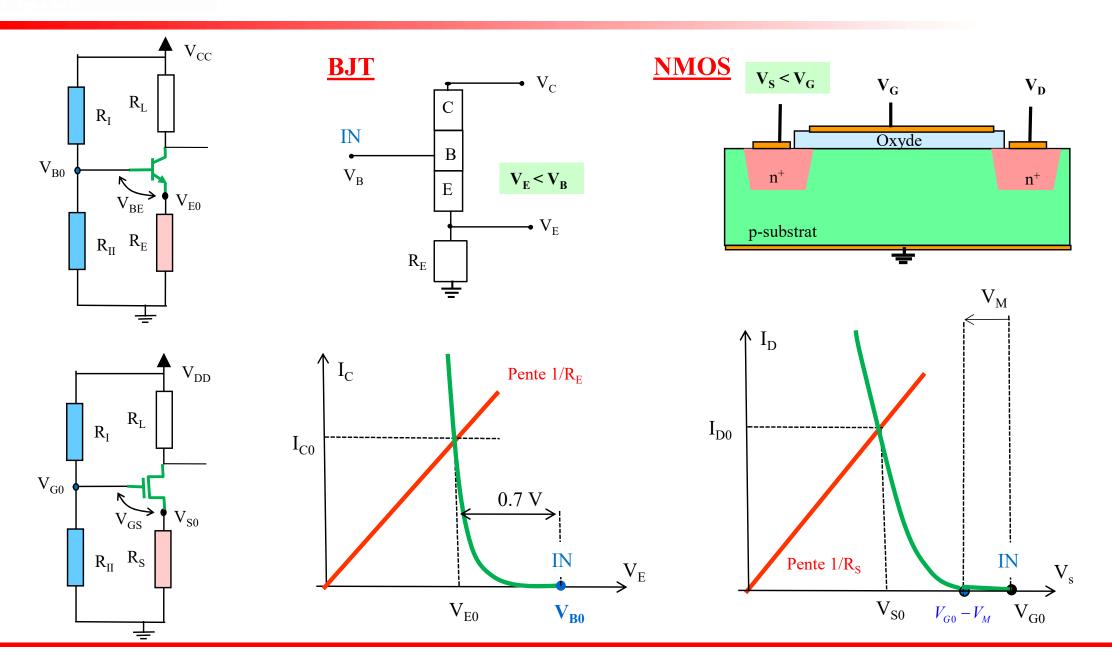


- Les capacités C₁ et C₂ assurent le couplage du signal AC à l'entrée et à la sortie
- La capacité C_3 maintient la tension de bias V_{E0} fixe et assure un transfert complet du signal v_{in} sur le courant I_C .
- R_S doit être beaucoup plus petit que R_{BE} =1/ g_{BE}

$$\frac{\tilde{v}_{out}}{\tilde{v}_B} \cong -g_m \cdot R_L$$

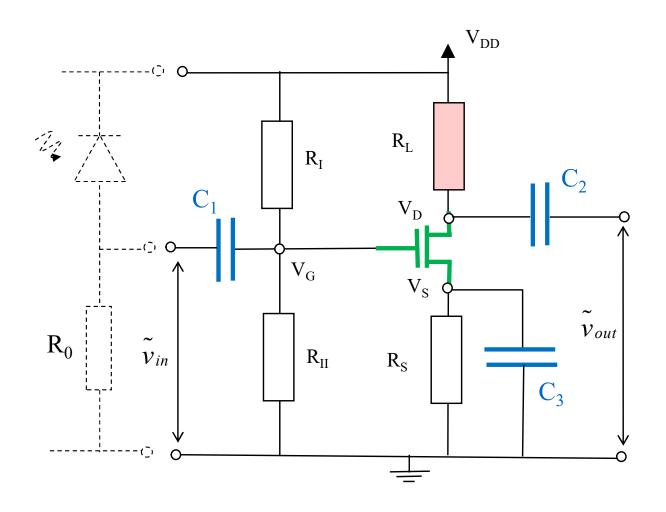


Comparaison BJT-NMOS





NMOS: Couplage capacitif

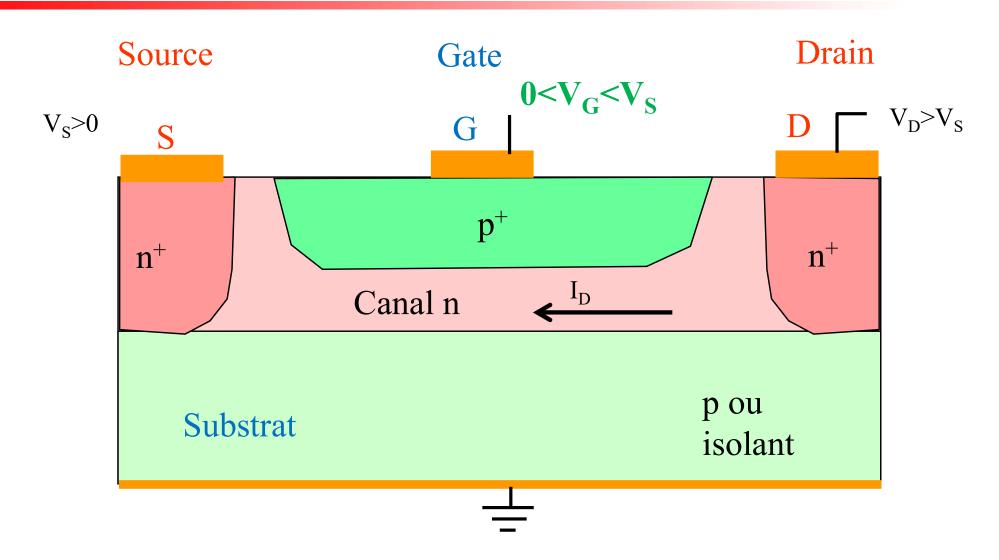


Gain en tension

$$\frac{\tilde{v}_{out}}{\tilde{v}_{in}} \cong -g_m \cdot R_L$$



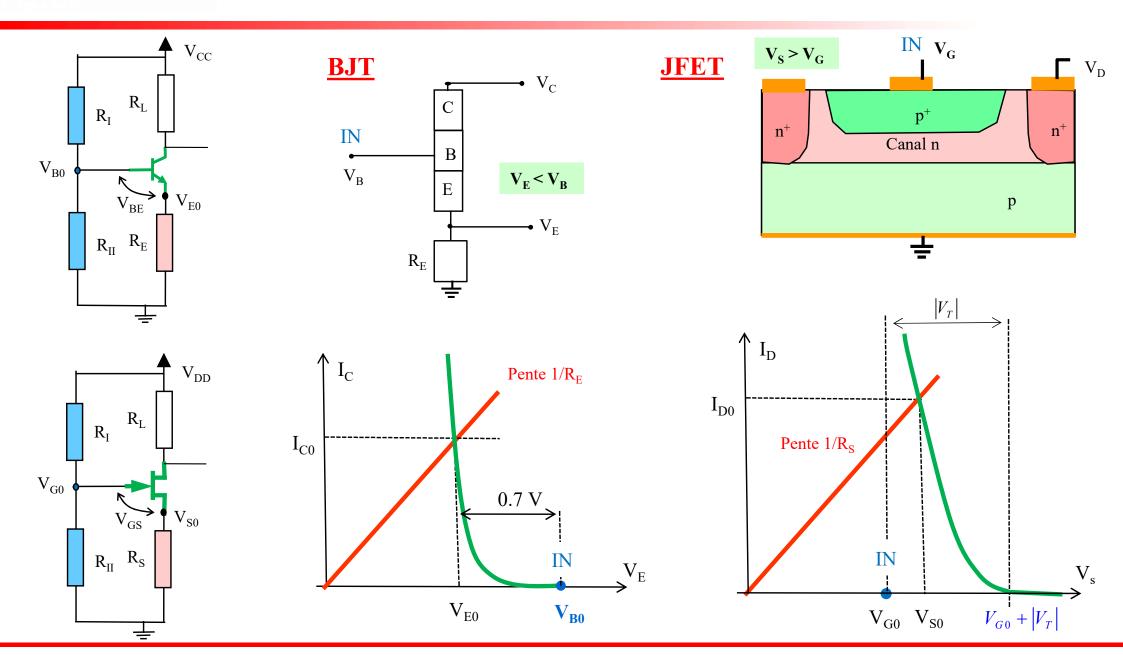
JFET à canal n



Plus V_S est supérieur à V_G plus le canal se ferme !

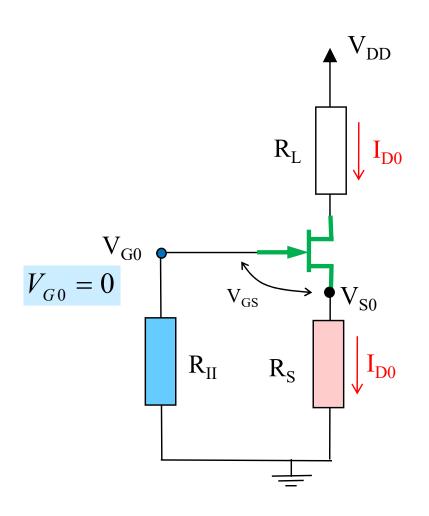


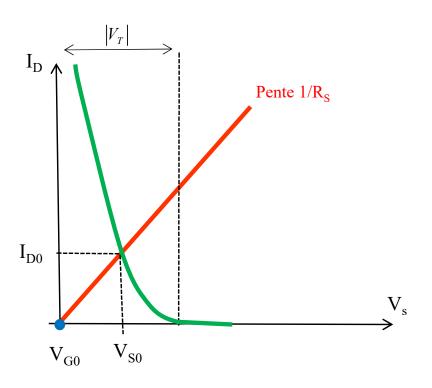
Comparaison BJT-JFET





Polarisation du JFET: cas spécial



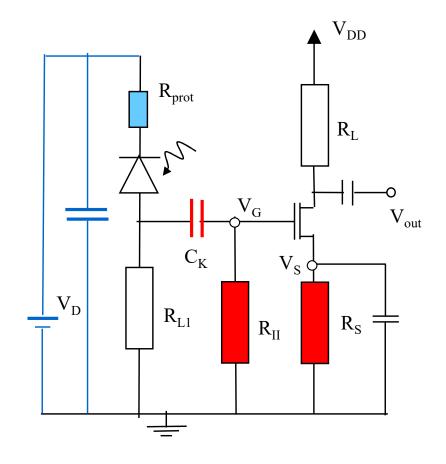


Il est possible de travailler avec V_{G0} =0

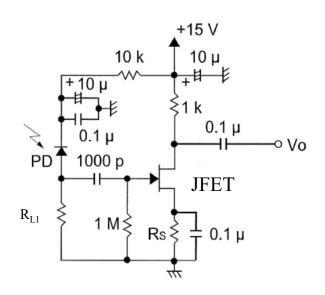


Exemple: photo-diode

Couplage capacitif



Note d'application Hamamatsu



PD: High-speed PIN photodiodes (S5052, S2506-02, S8314, S5971, S5972, S5973, etc.)

R_{L1} Determined by sensitivity and time constant of Ct of photodiode

Rs : Determined by operation point of FET

FET: 2SK152, 2SK192A, 2SK362, etc.

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