PHYSIQUE DES COMPOSANTS SEMI-CONDUCTEURS

XIII) Circuits analogiques en CMOS

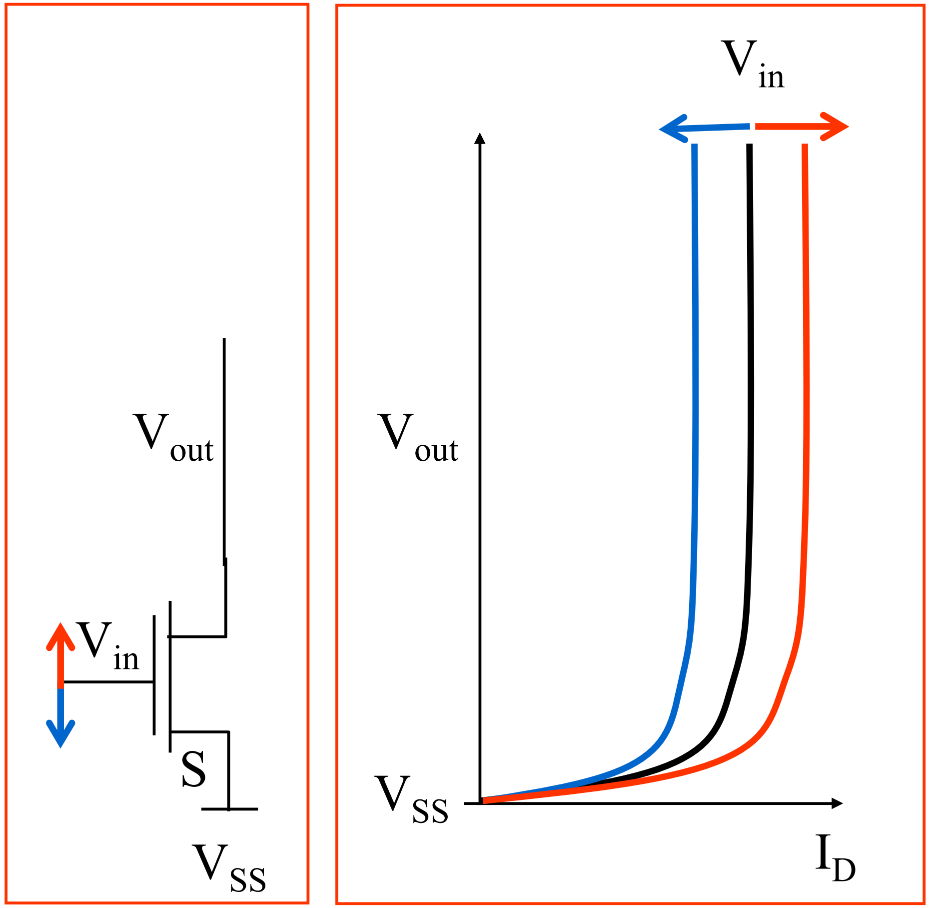
P.A. Besse

EPFL

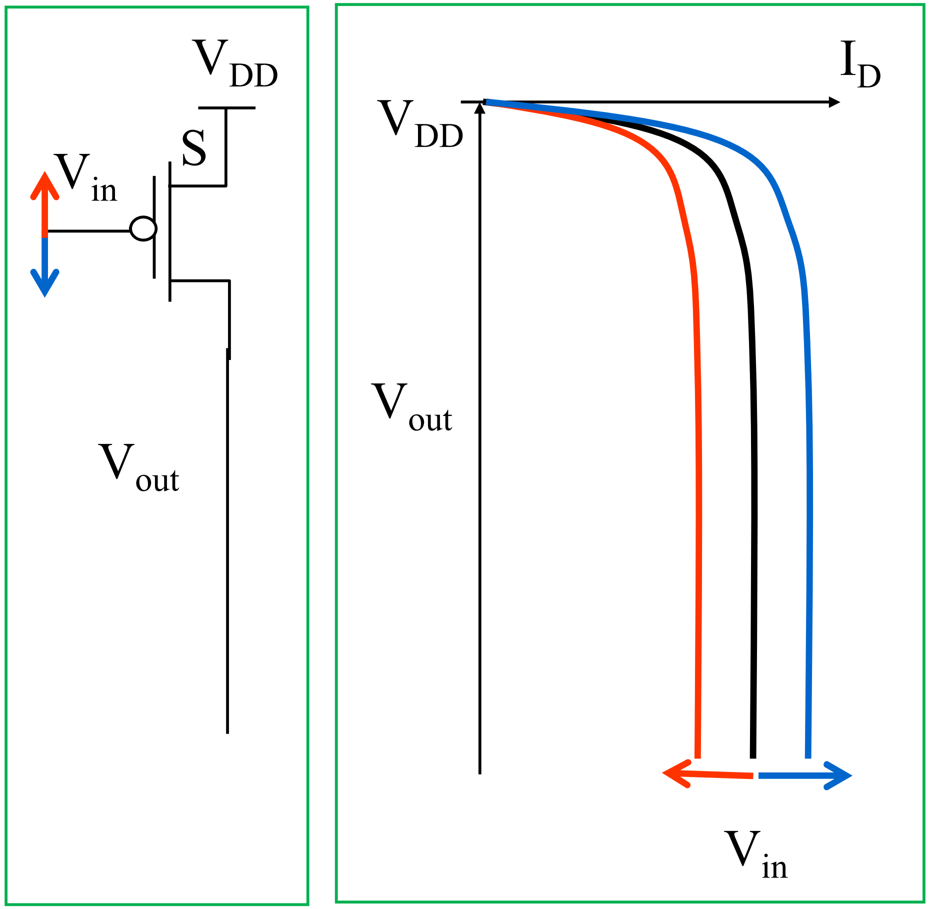
Résumé des courbes caractéristiques des MOS

Caractéristiques (1)

N-MOS

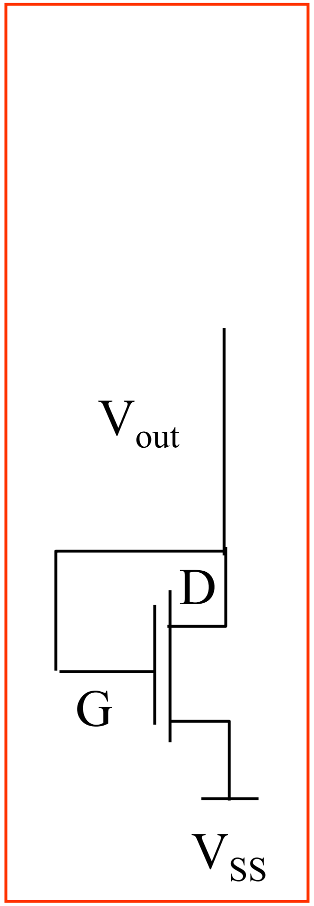


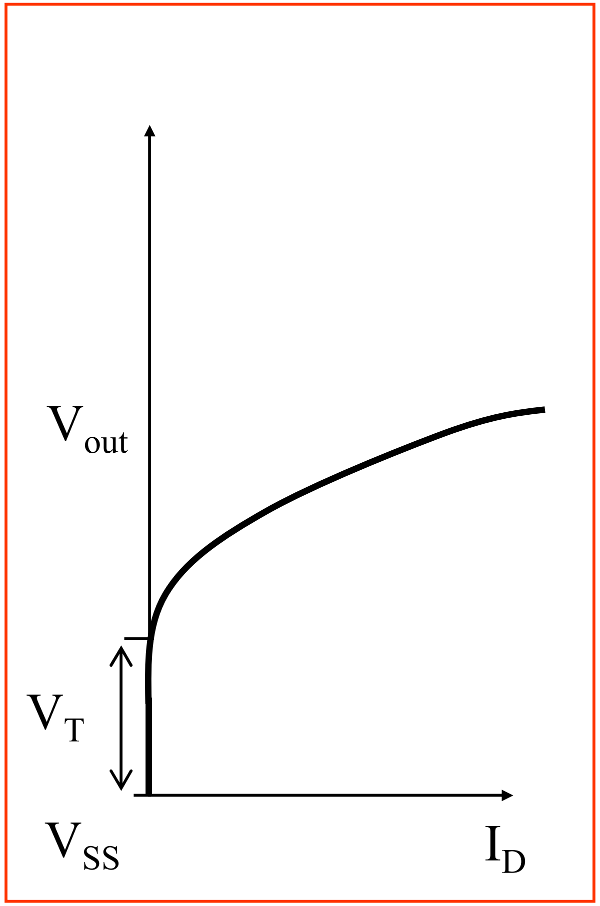
P-MOS

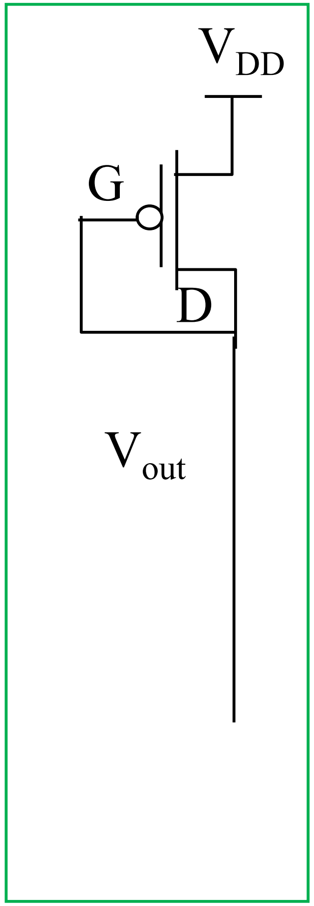


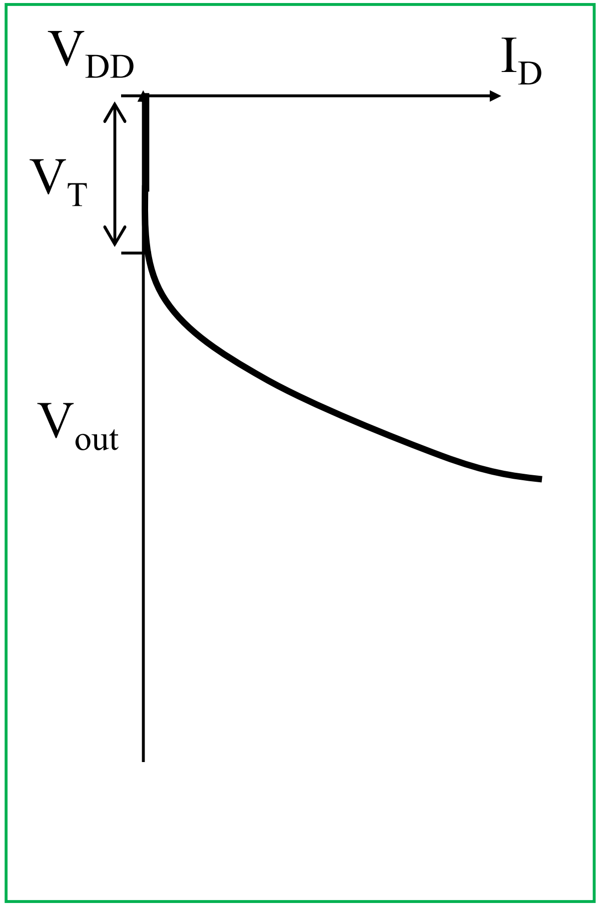
Caractéristiques (2)

N-MOS « gate – drain reliés » **P-MOS**



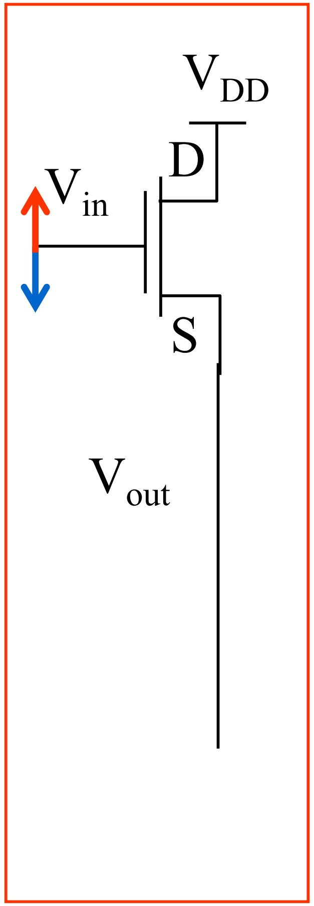


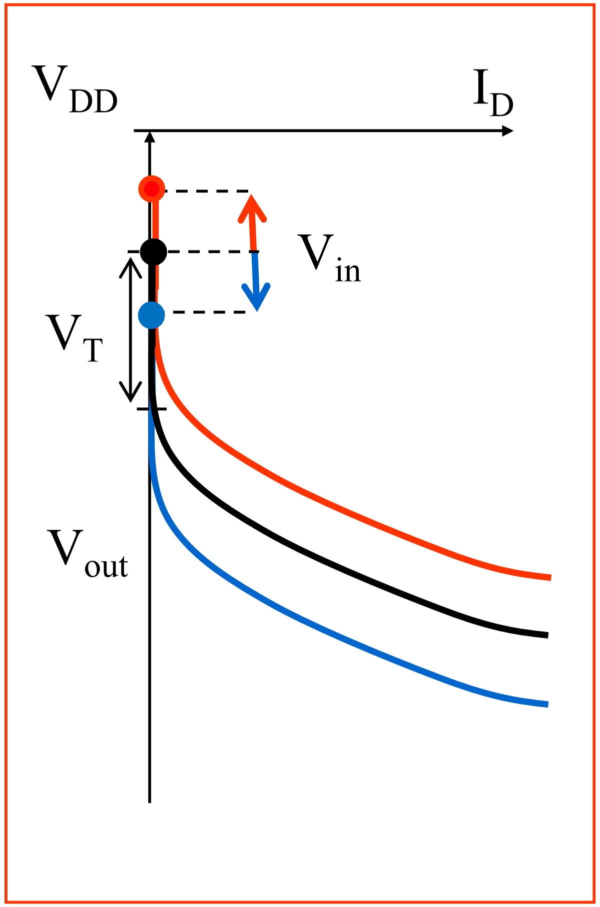




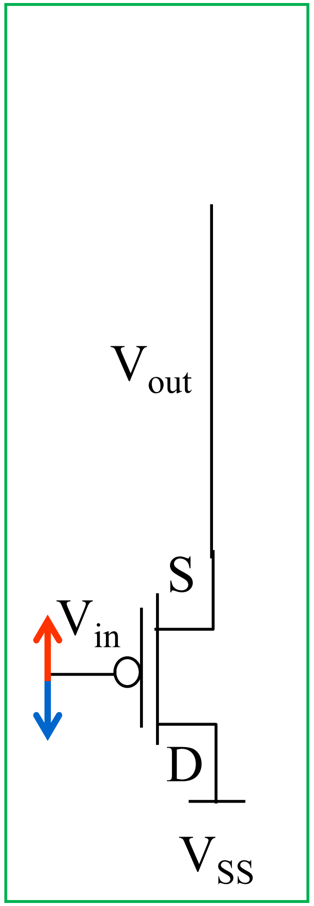
Caractéristiques (3)

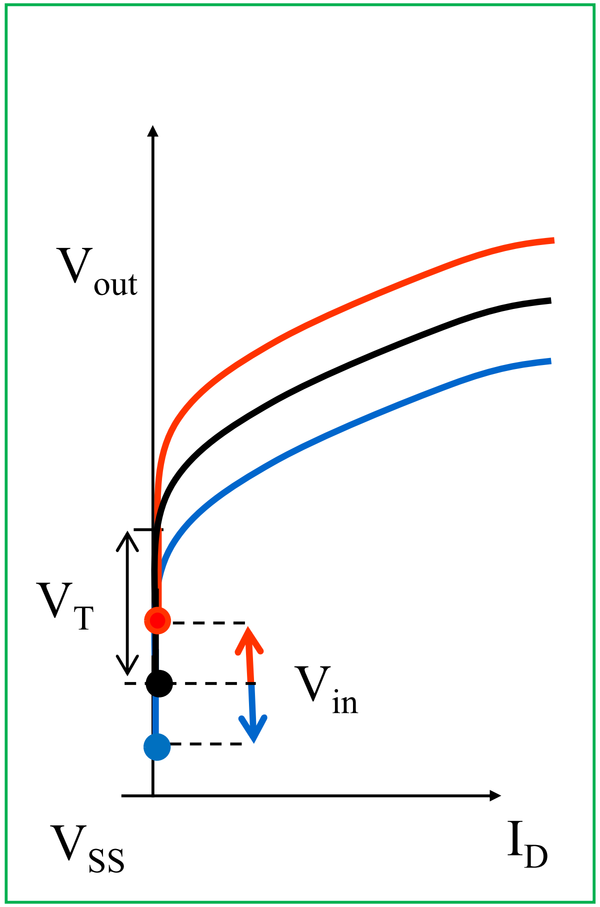
N-MOS





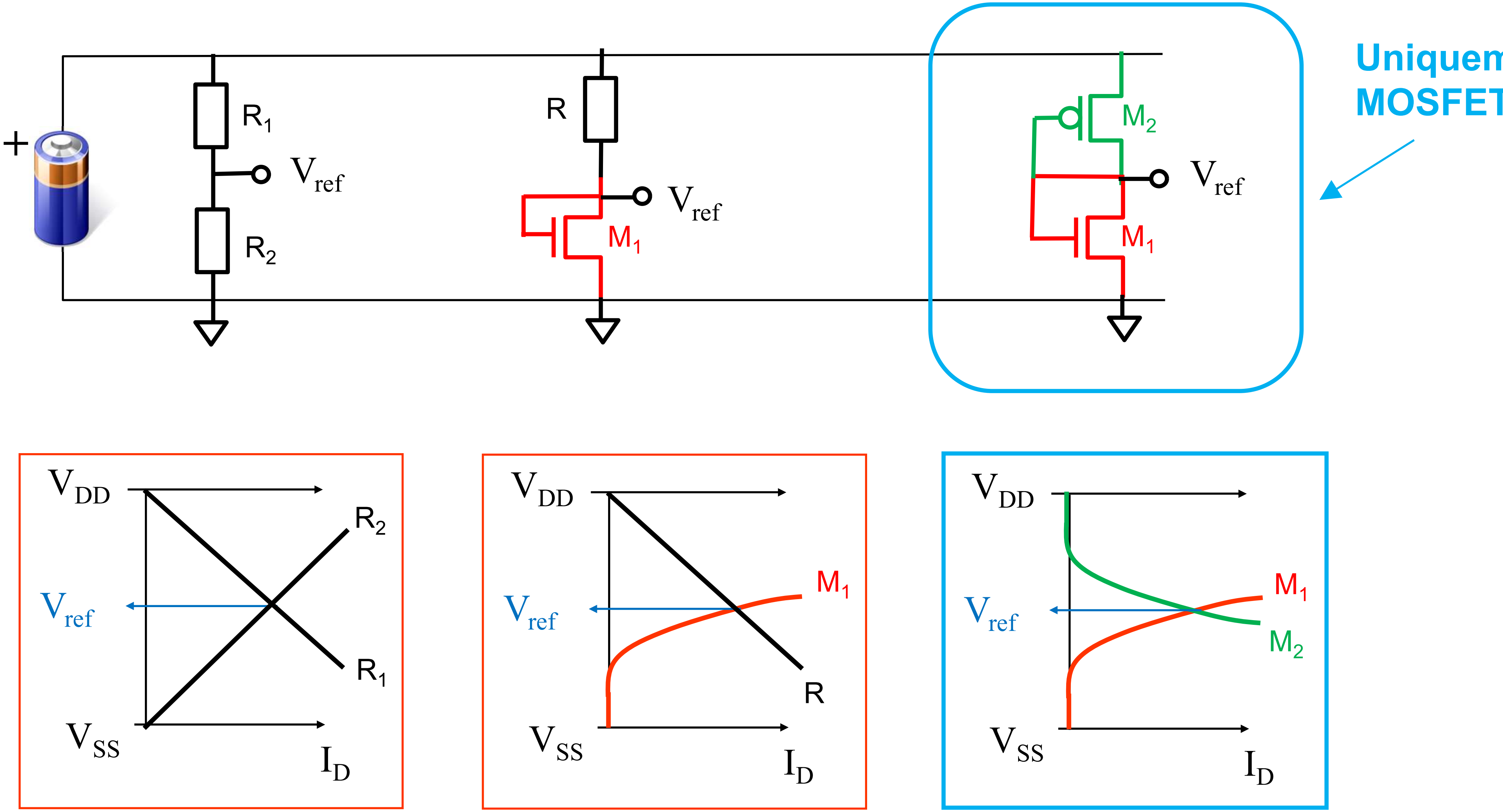
P-MOS





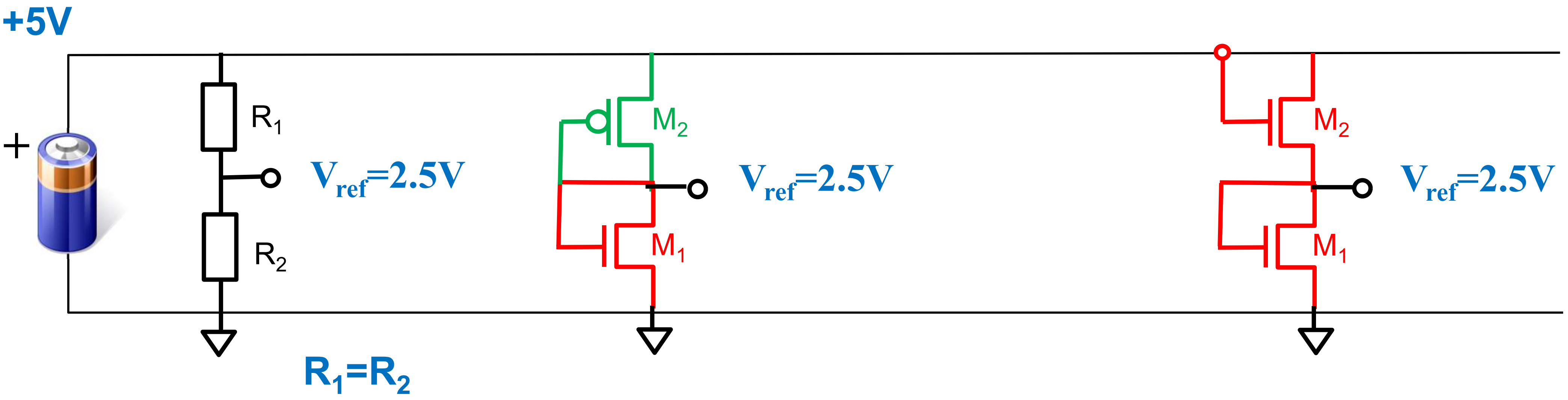
Diviseurs de tension

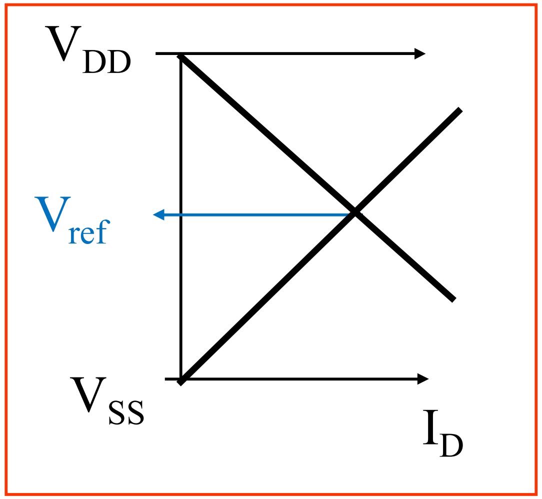
Diviseurs de tension

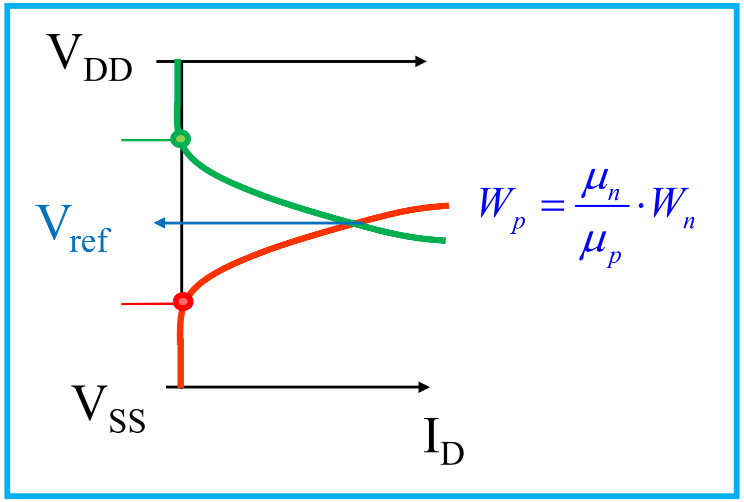


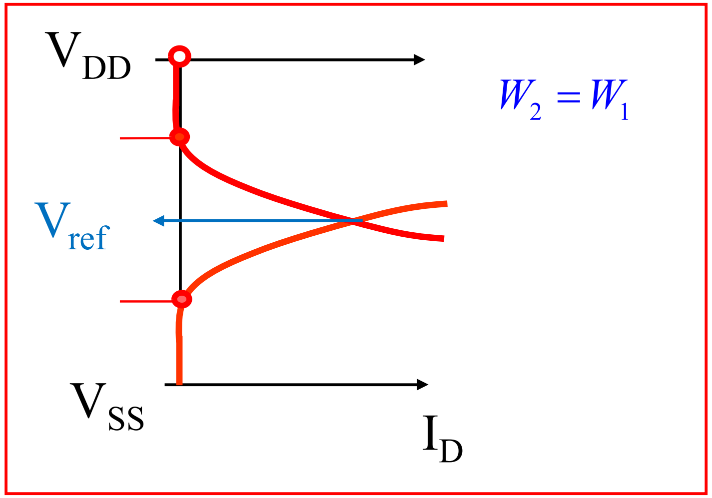
Question:
Diviseurs de tension

Pile de 5V: comment obtenir 2.5V pour V_{ref} ?

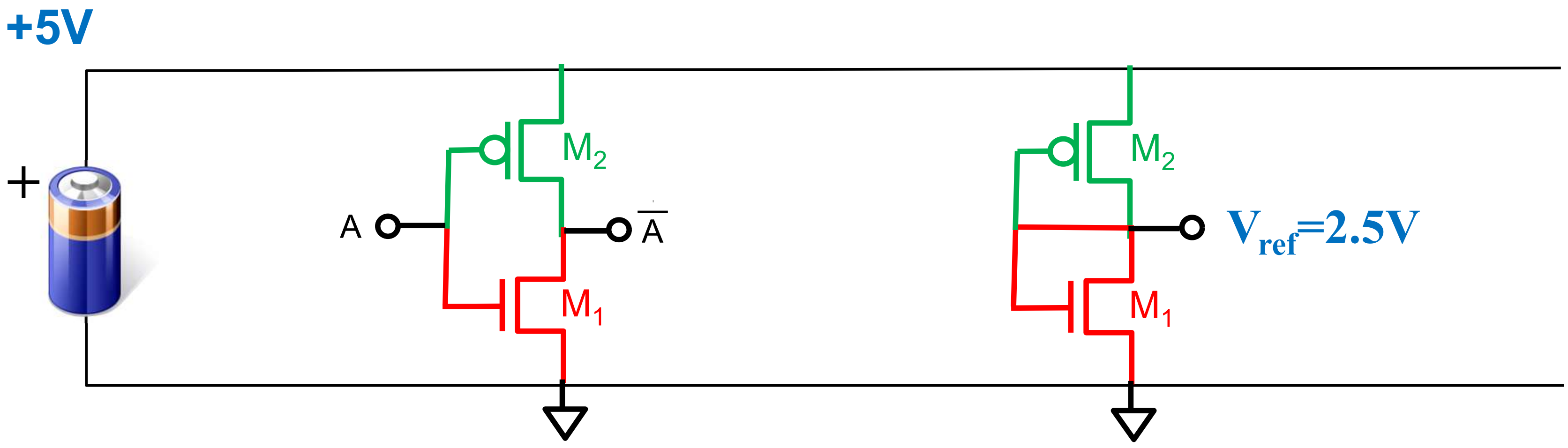






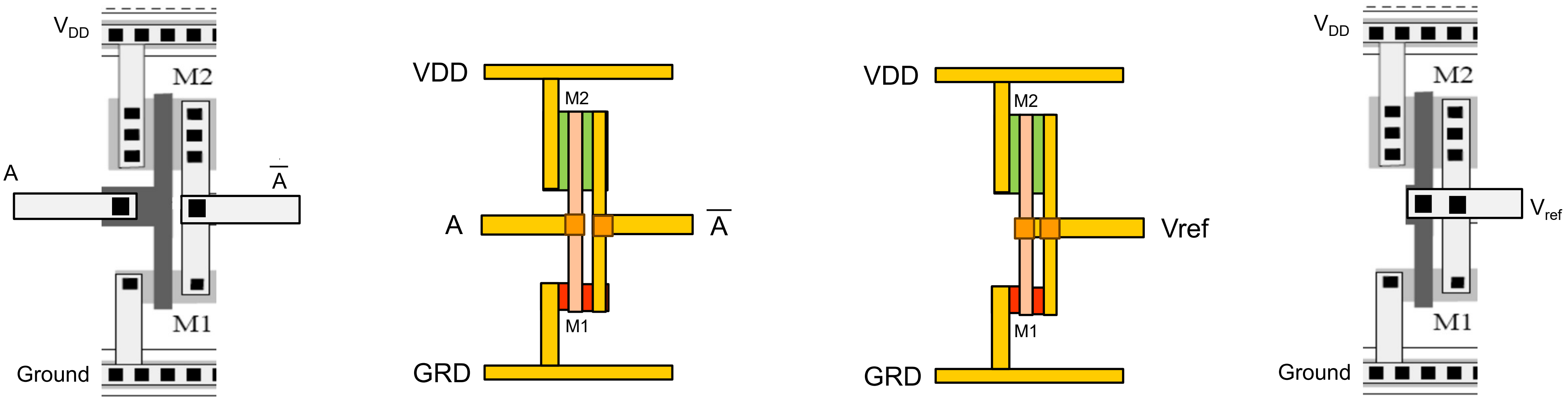


Comparaison: Inverseur / Diviseurs de tension



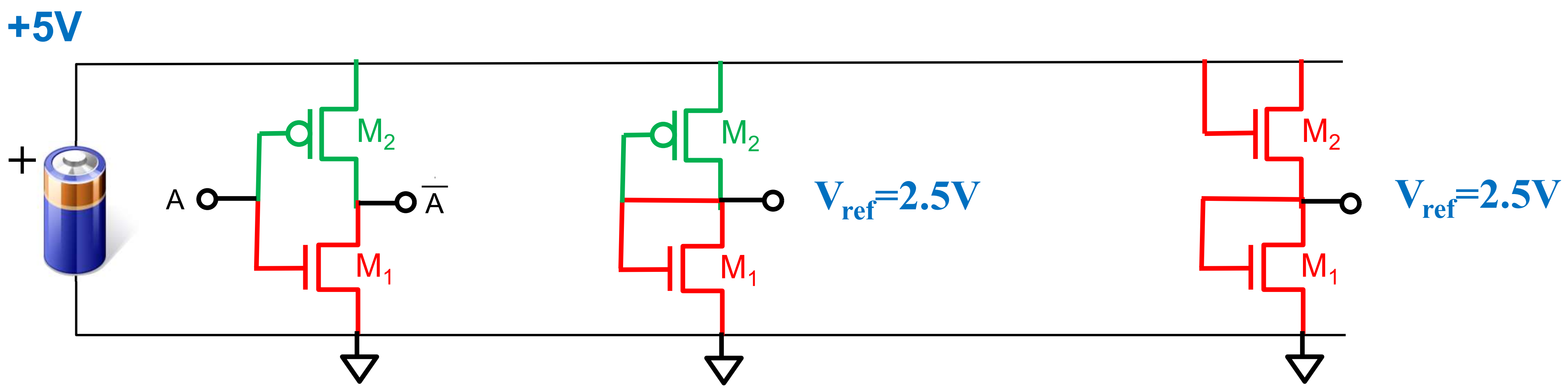
Inverseur

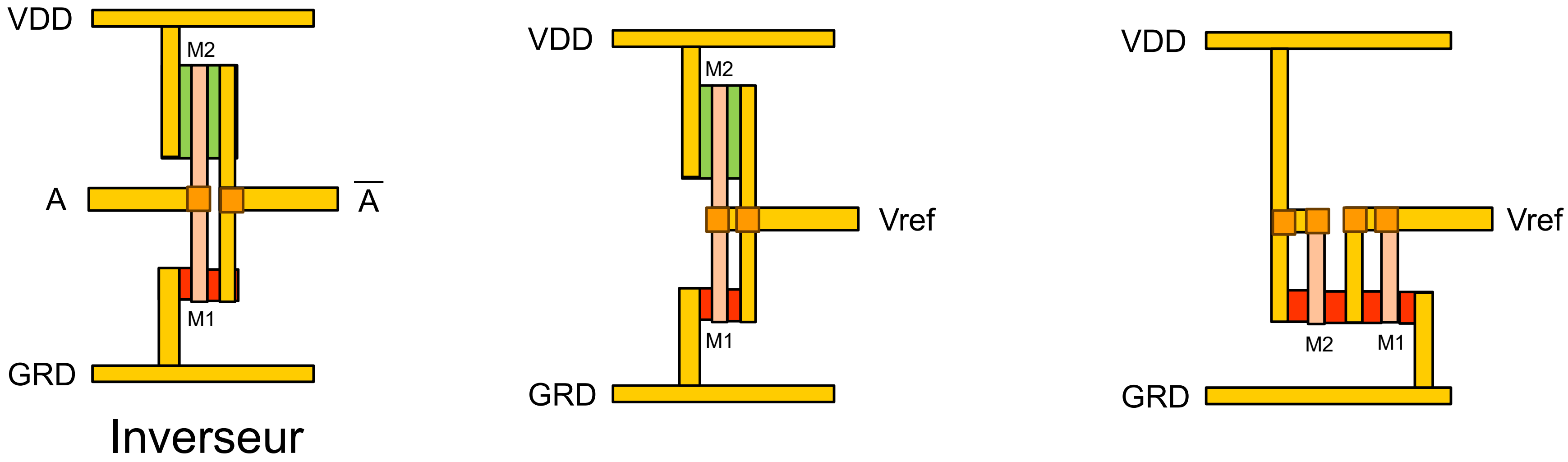
Diviseur de tension



Question:
Diviseurs de tension

Pile de 5V: comment obtenir 2.5V pour V_{ref} ?

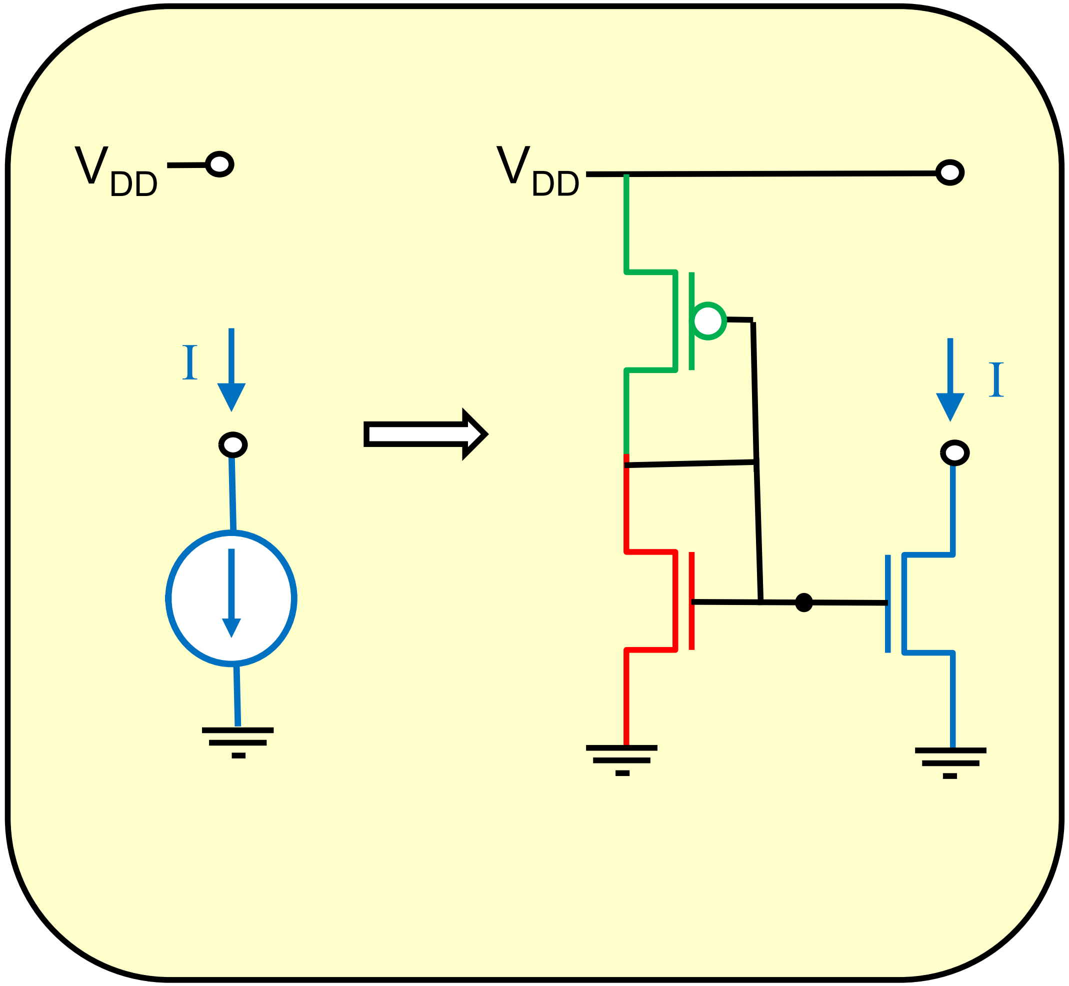




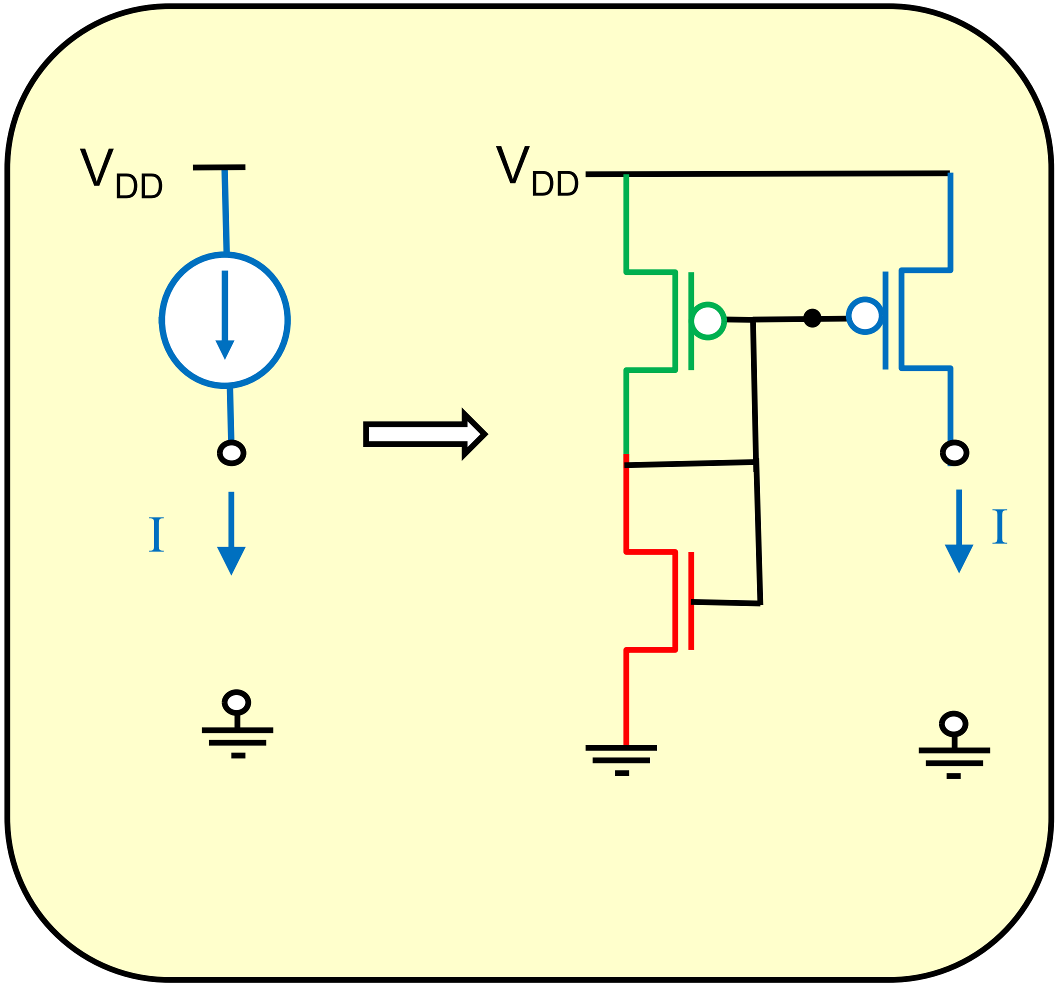
Sources et miroirs de courant

Source de courant simple (1)

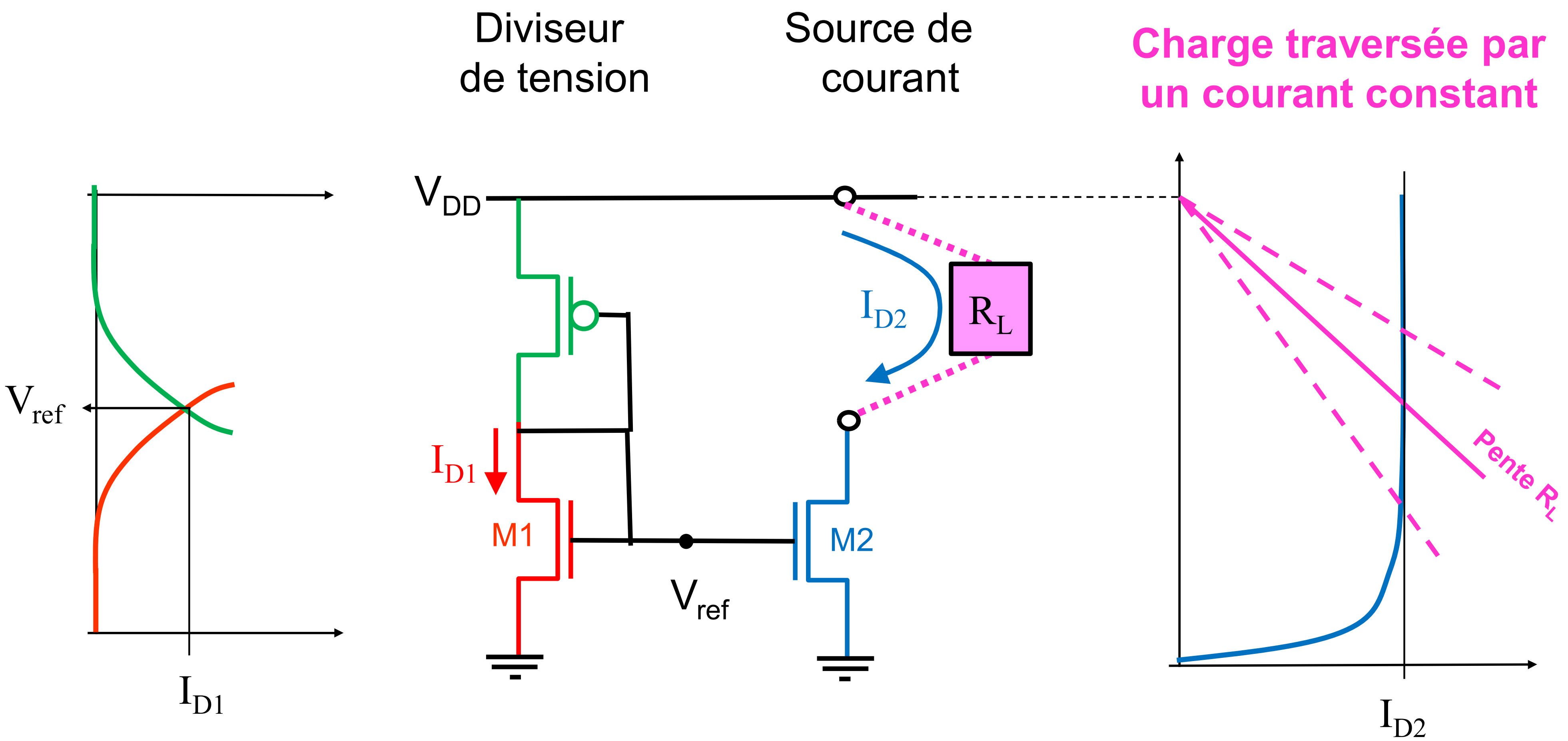
NMOS comme source de courant



PMOS comme source de courant



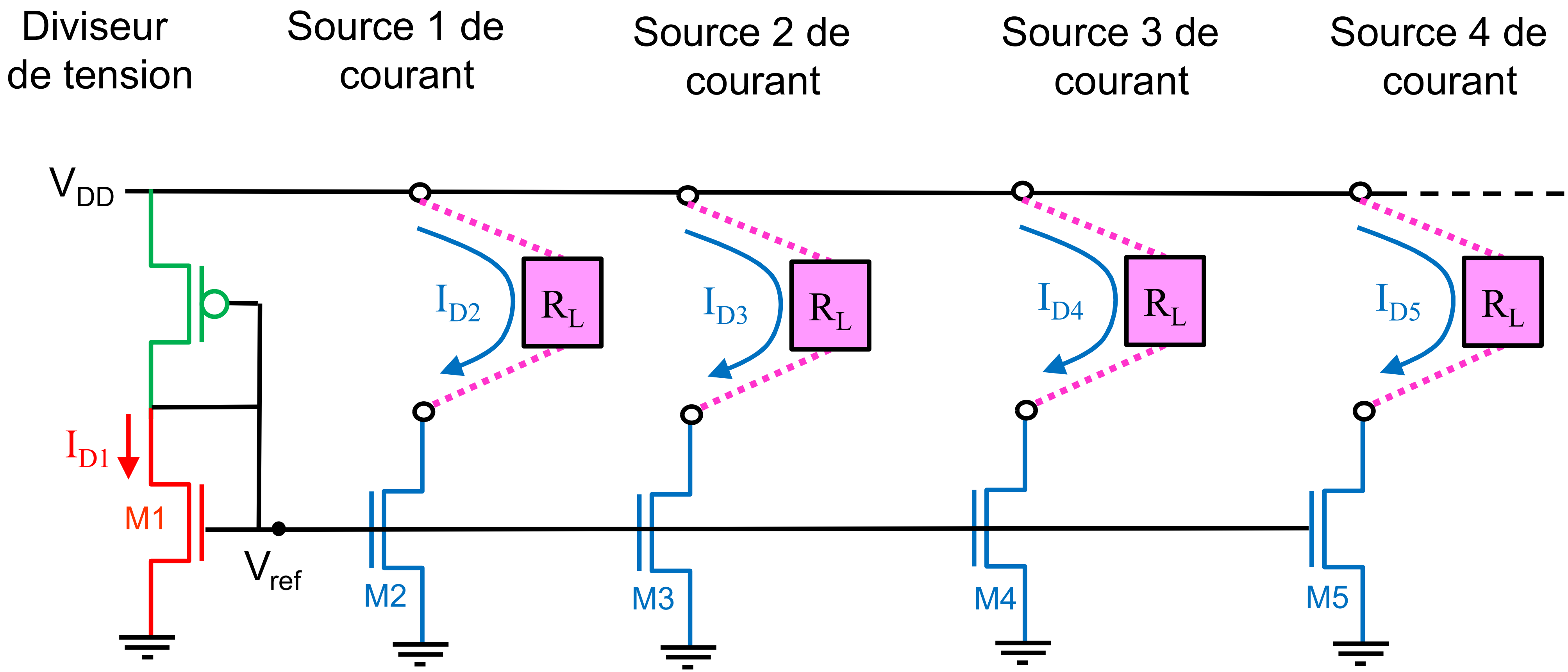
Source de courant simple (2)



Un diviseur de tension sert à contrôler un NMOS

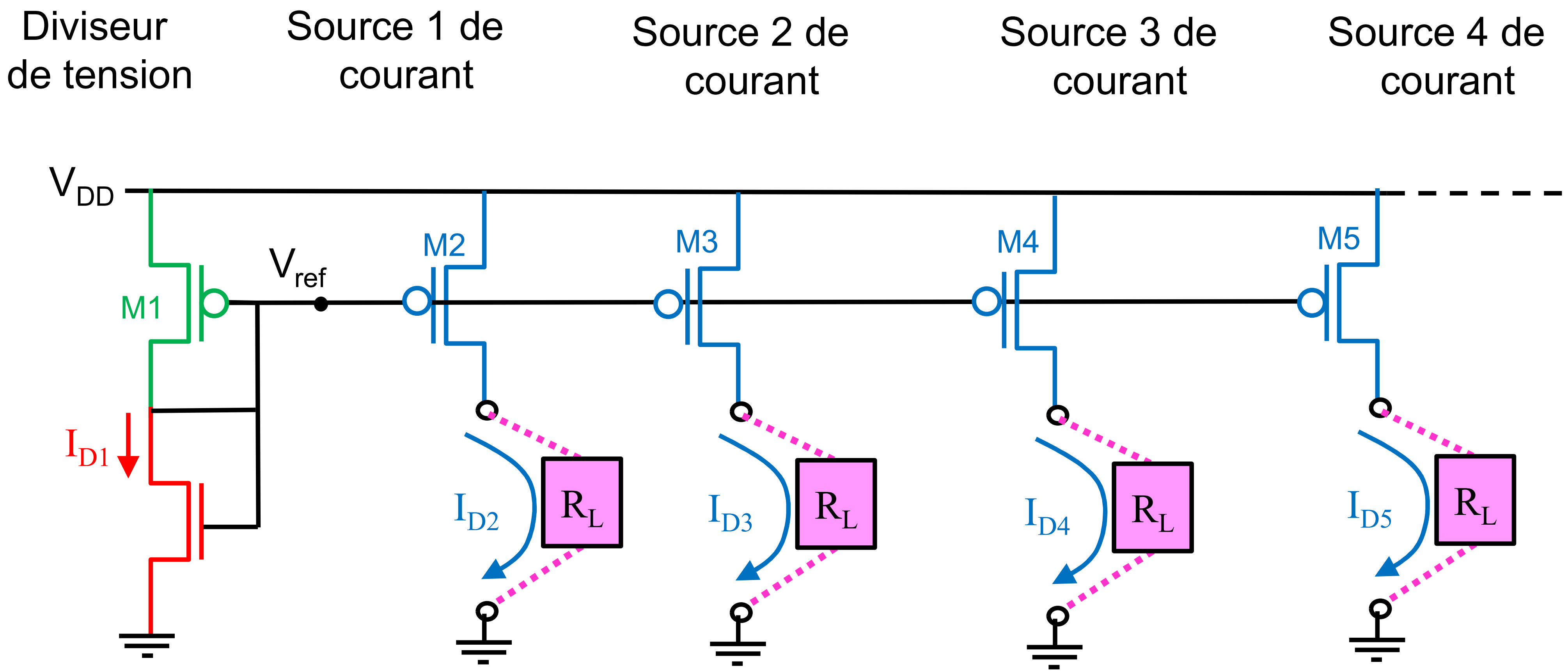
$$I_{D2} = \frac{W_2}{W_1}\frac{L_1}{L_2} \cdot I_{D1}$$

NMOS comme multiple sources de courant



$$\boxed{I_{Dn} = \frac{W_n}{W_1} \frac{L_1}{L_n} \cdot I_{D1}}$$

PMOS comme multiple sources de courant

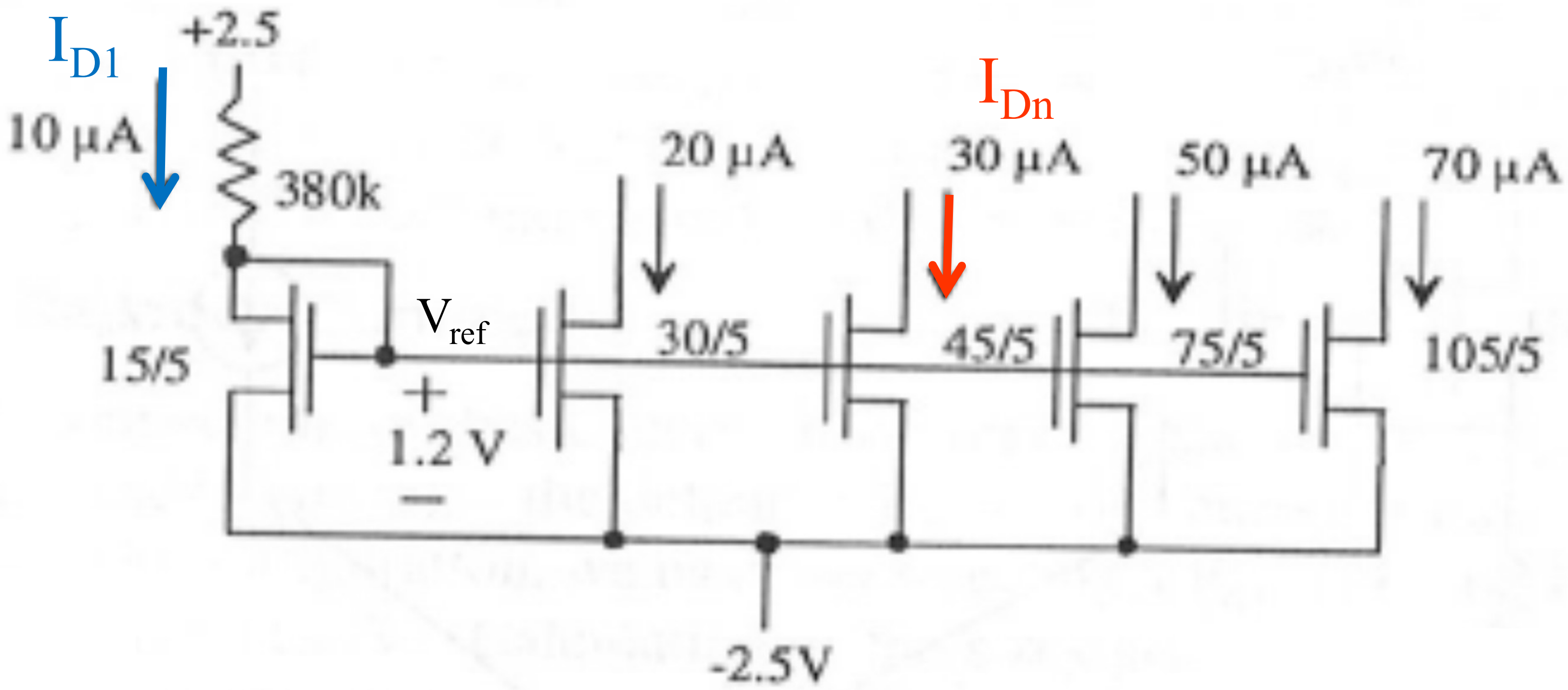


$$I_{Dn} = \frac{W_n}{W_1}\frac{L_1}{L_n}\cdot I_{D1}$$

Exemple de multiple sources de courant

Diviseur de tension

4 sources de courant en parallèle

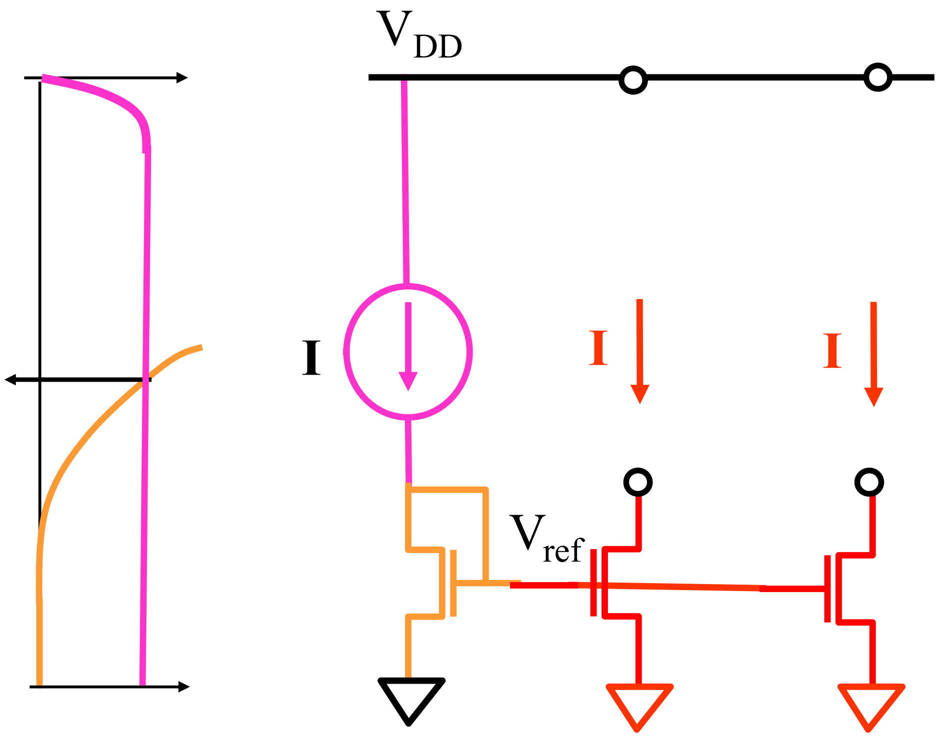


$$I_{Dn} = \frac{W_n}{W_1}\frac{L_1}{L_n}\cdot I_{D1}$$

R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

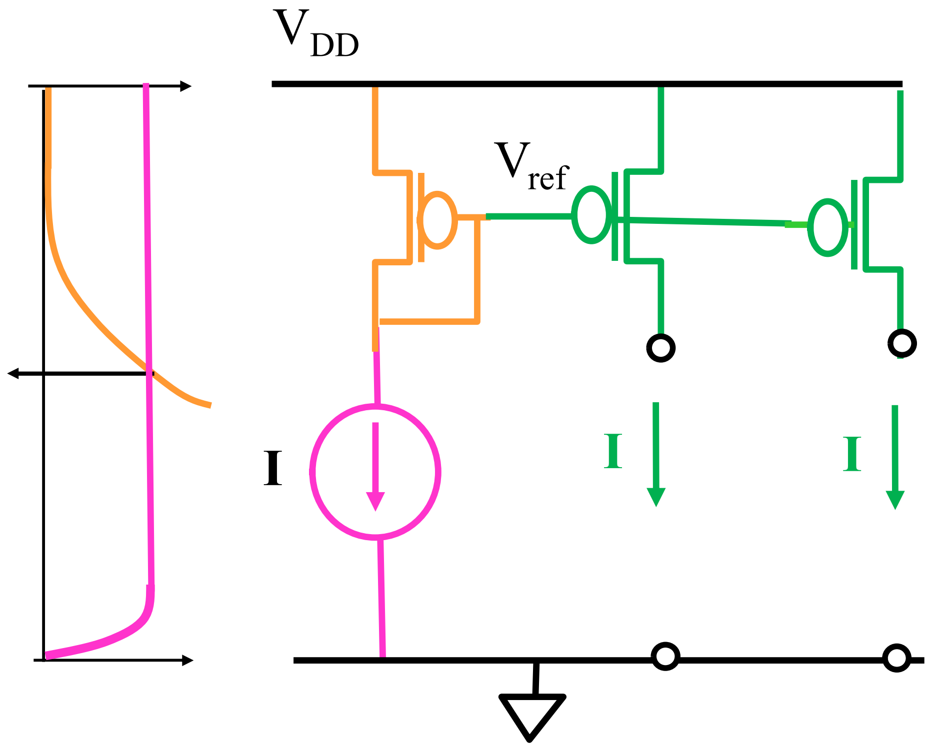
Miroir de courant

Basé sur NMOS



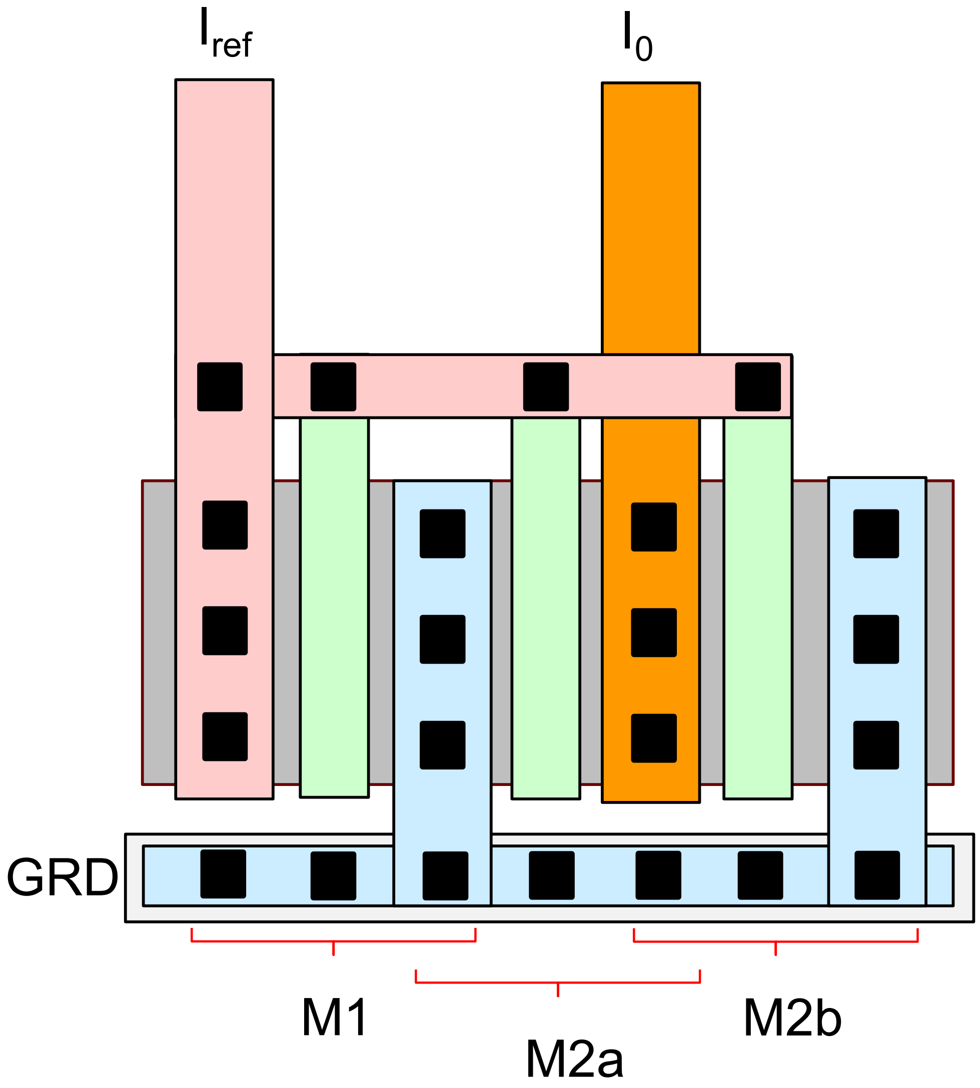
La source de courant
peut être un PMOS

Basé sur PMOS

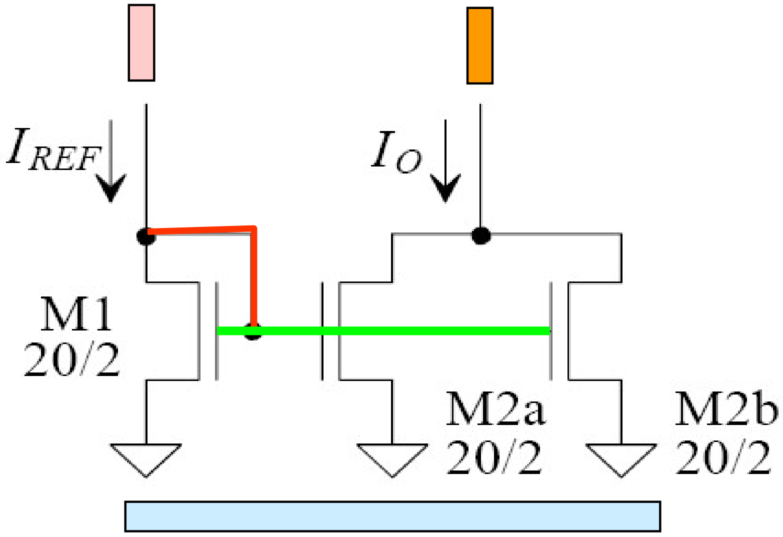


La source de courant
peut être un NMOS

Miroir de courant: exemple de layout



R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press



$$I_0 = 2I_{ref}$$

Ampli de tension

en boucle ouverte

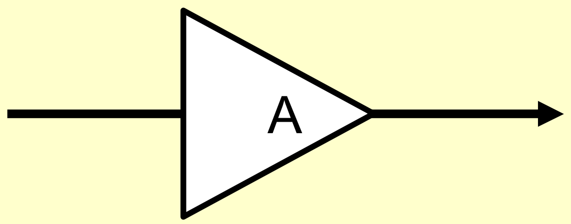
Ampli de tension: catégories

<u>En boucle ouverte</u>

- Résistance de charge
  ou
  Résistance active

- Gain modeste

- Point de travail par couplage capacitif

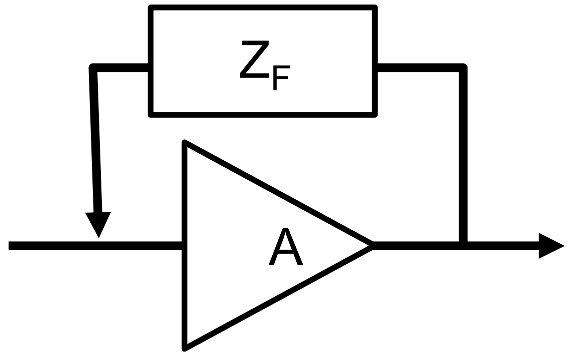


En boucle fermée

- Source de courant comme charge

- Gain en boucle ouverte
  très important
  Gain final déterminé par le feedback

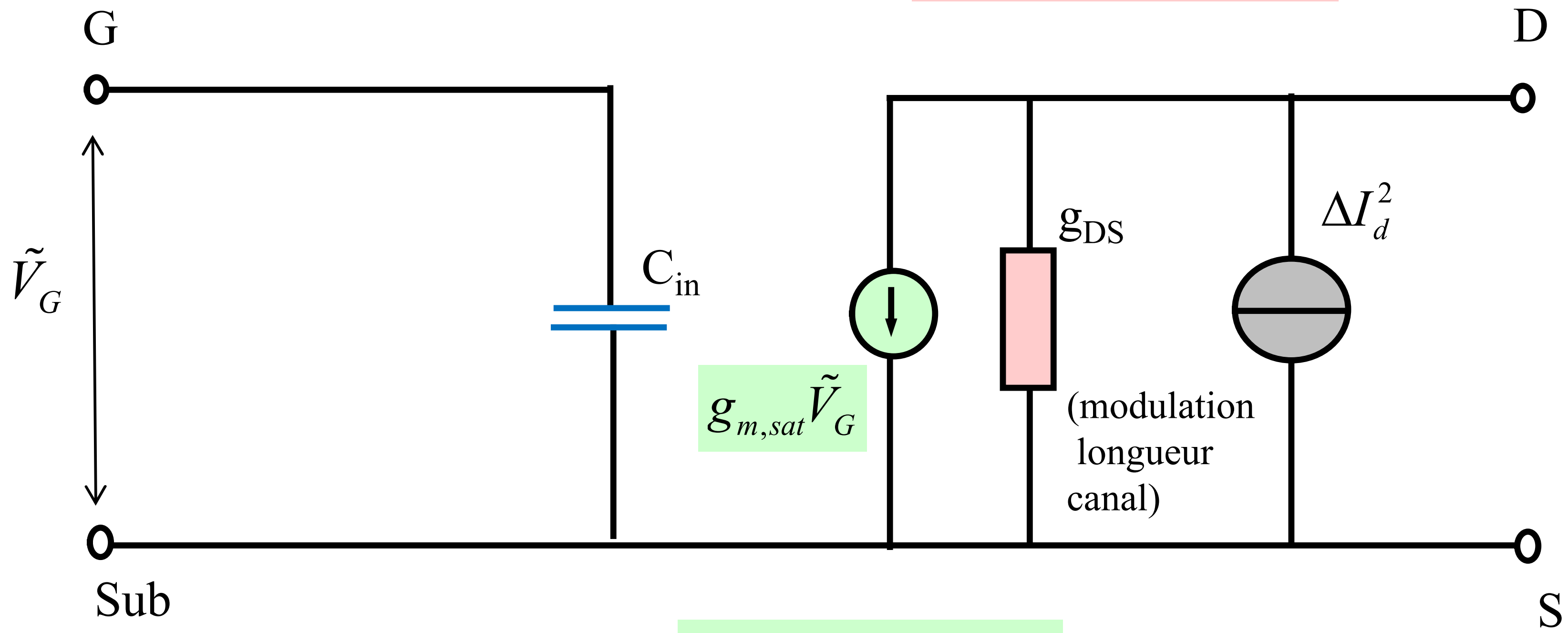
- Point de travail fixé par une boucle de feedback



Rappel: MOSFET circuit petits signaux simplifié

$$C_{in} \cong (Z \cdot L) \cdot \overline{C}_{ox}$$

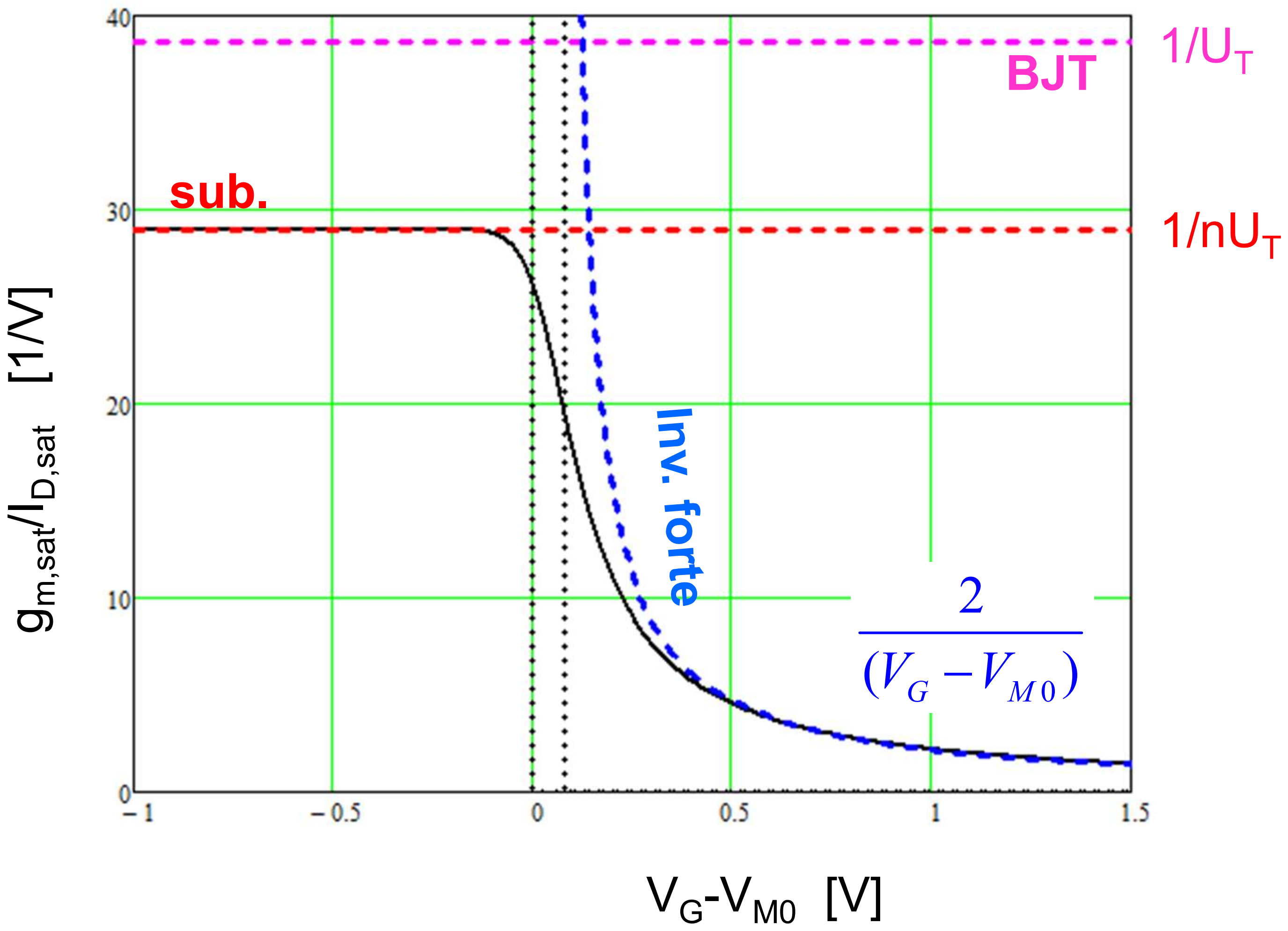
$$g_{DS} \equiv \frac{\delta I_D}{\delta V_D} \cong \frac{|I_{D,sat}|}{|V_A|}$$



$$\frac{g_{m,sat}}{|I_{D,sat}|} \cong \frac{2}{V_G - V_T}$$

Inversion forte

Comparaison: g_m/I_D



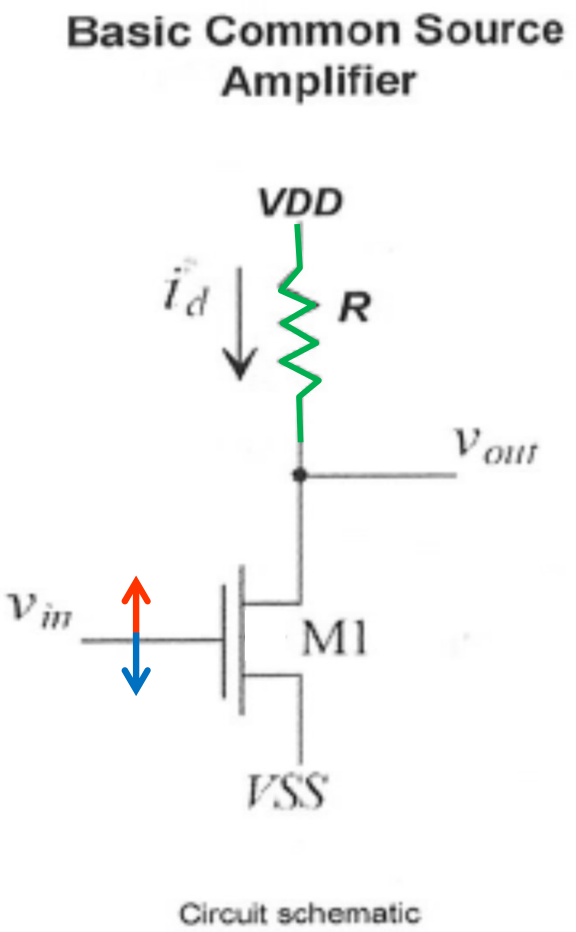
Transconductance
définition

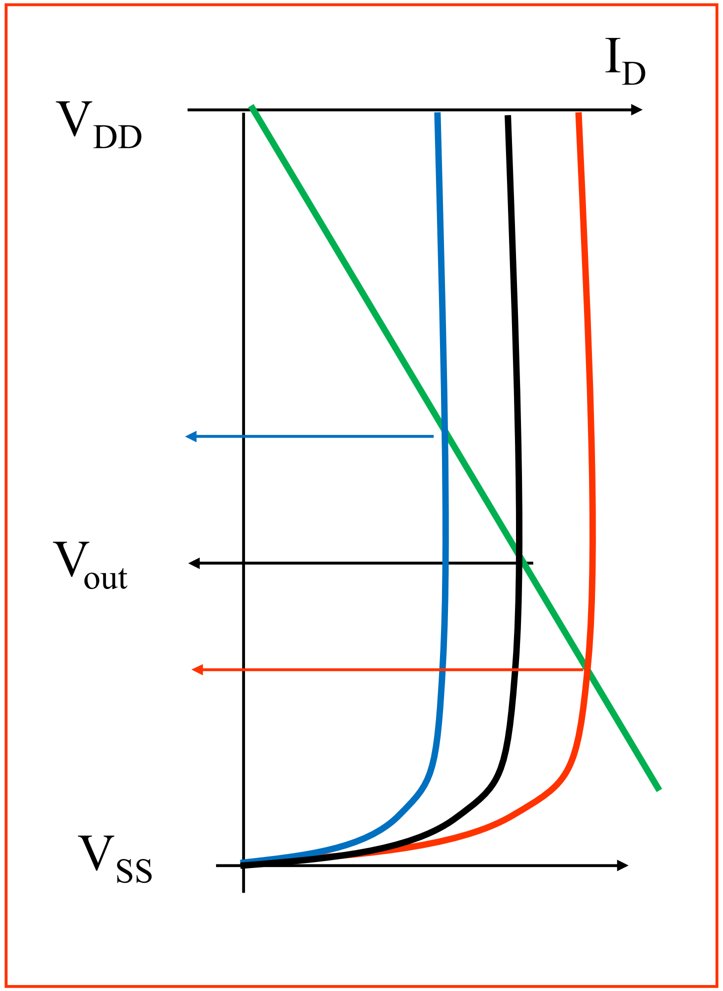
$$g_{m,sat} \equiv \frac{\partial I_{D,sat}}{\partial V_G}$$

C_{ox}=3fF/um^2
W/L=10
T=300 K

u_n=1000cm^2/V.s
n=4/3

Ampli de tension avec résistance de charge





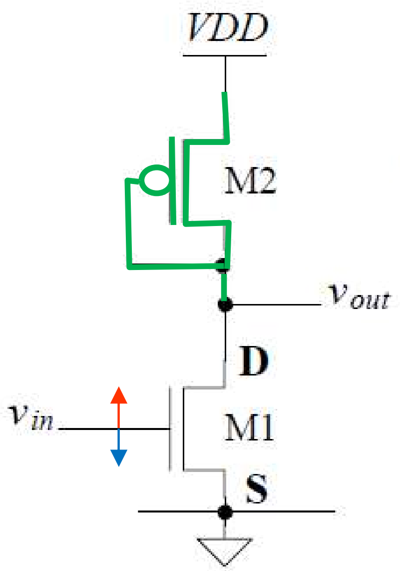
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

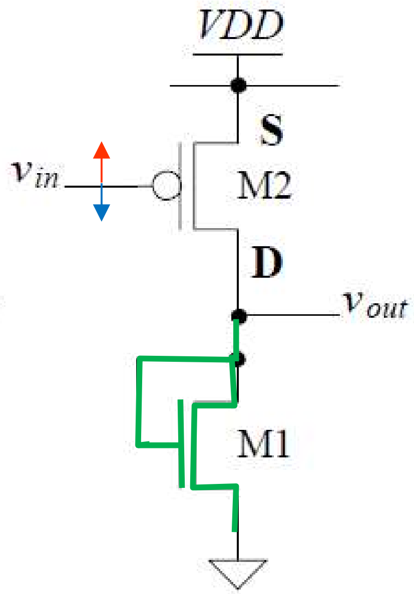
Gain

$$\frac{V_{out}}{V_{in}} = -g_{m1} \cdot R$$

Ampli de tension
avec résistance active

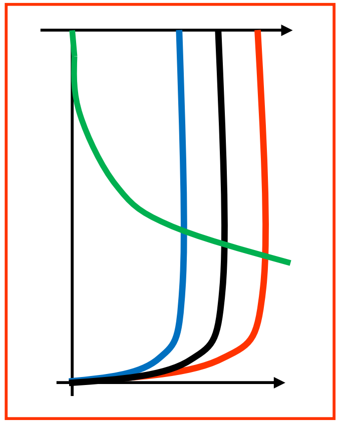
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press





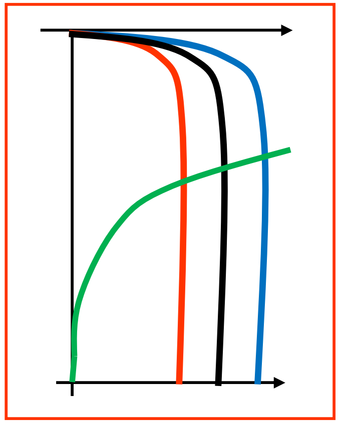
$$V_{out} = -\frac{g_{m1}}{g_{m2}} \cdot V_{in}$$

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}/I_D}{g_{m2}/I_D}$$



$$V_{out} = -\frac{g_{m2}}{g_{m1}} \cdot V_{in}$$

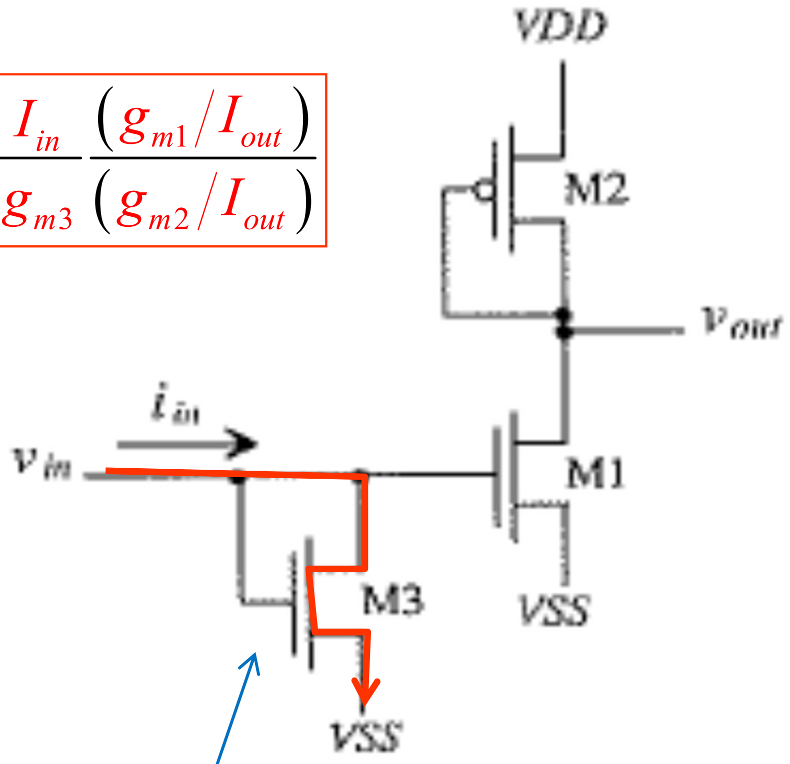
$$\frac{V_{out}}{V_{in}} = -\frac{g_{m2}/I_D}{g_{m1}/I_D}$$



R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

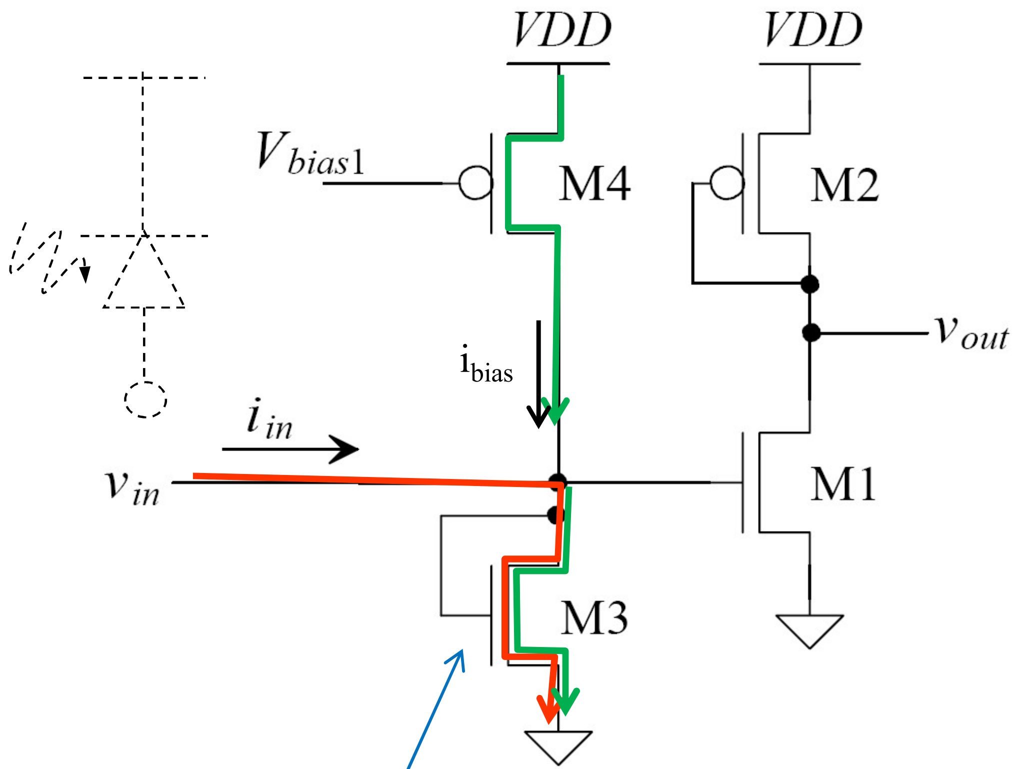
Principe

$$\boxed{V_{out} = -\frac{I_{in}}{g_{m3}} \frac{\left(g_{m1}/I_{out}\right)}{\left(g_{m2}/I_{out}\right)}}$$



Résistance → convertit le courant en tension

Biasing

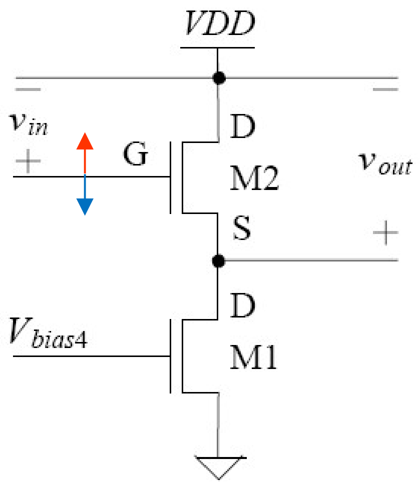


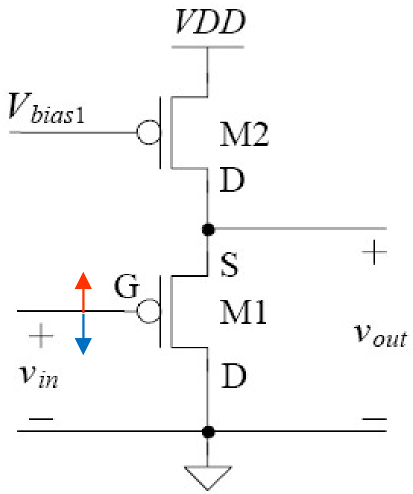
Résistance → convertit le courant en tension

Source follower: current source load

R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

Seulement NMOS

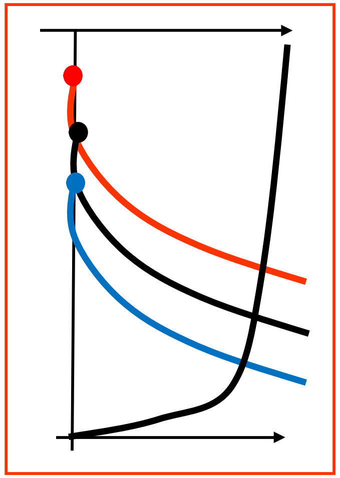


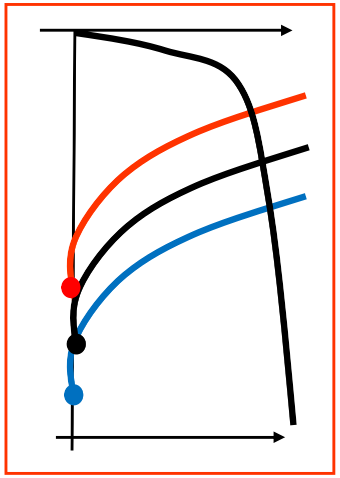


Seulement PMOS

$$\frac{V_{out}}{V_{in}} = R_{out} \cdot g_{m2} \cong 1$$

$$R_{out} = R_{0,1} \left\| \frac{1}{g_{m2}} \cong \frac{1}{g_{m2}} \right.$$

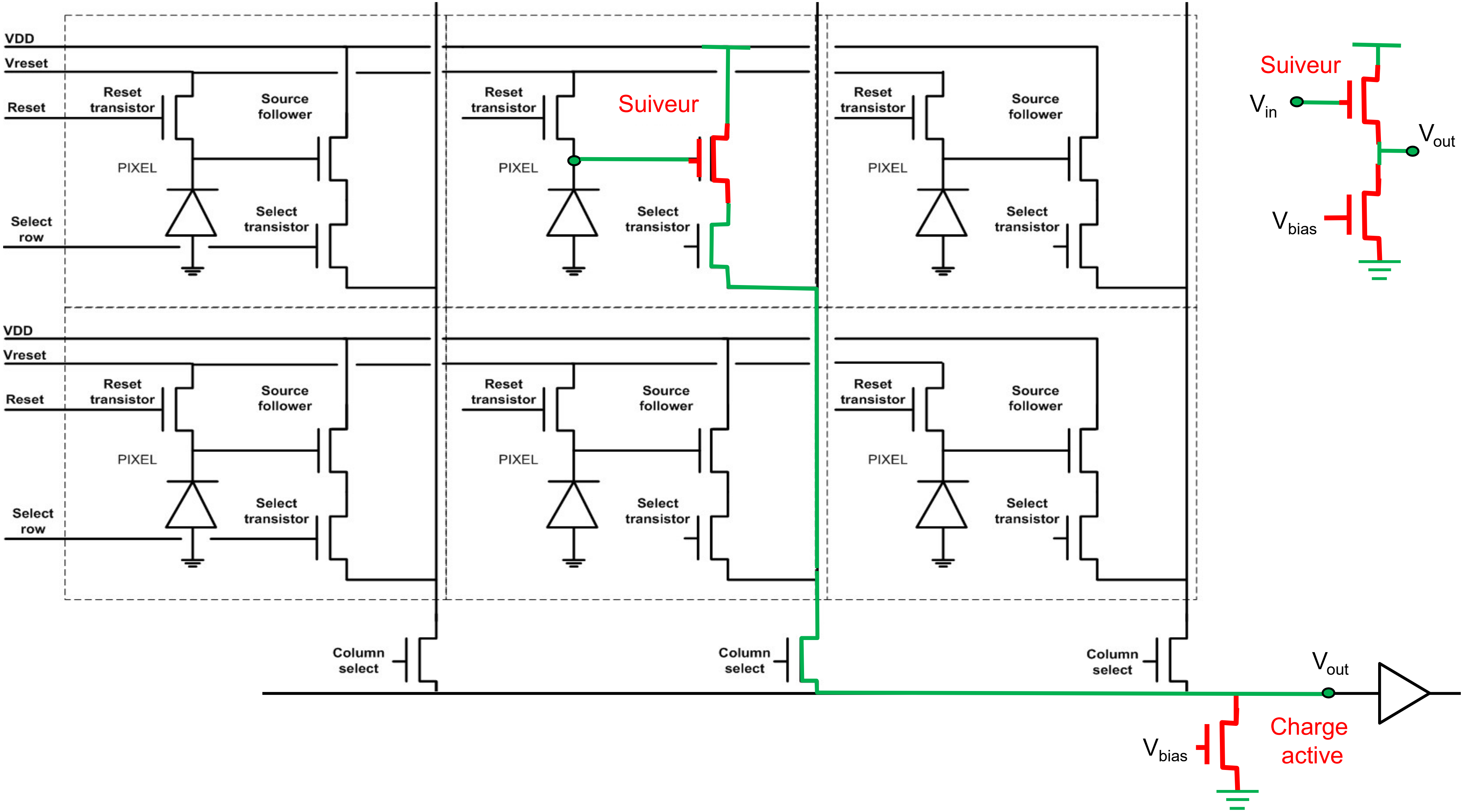




$$\frac{V_{out}}{V_{in}} = R_{out} \cdot g_{m1} \cong 1$$

$$R_{out} = R_{0,2} \left\| \frac{1}{g_{m1}} \cong \frac{1}{g_{m1}} \right.$$

Exemple d'utilization du suiveur NMOS: Standard 3T APS CMOS camera



Ampli de tension en boucle fermée

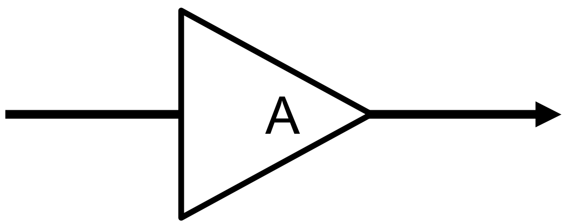
Ampli de tension: catégories

<u>En boucle ouverte</u>

- Résistance de charge
  ou
  Résistance active

- Gain modeste

- Point de travail par couplage capacitif

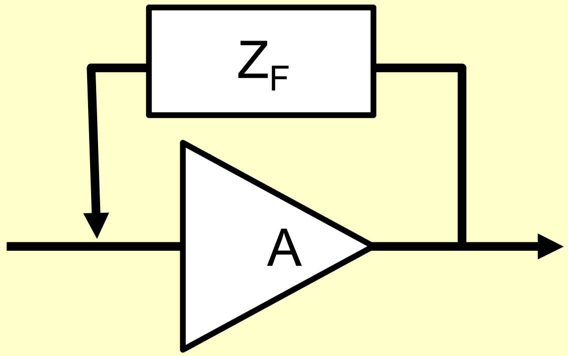


En boucle fermée

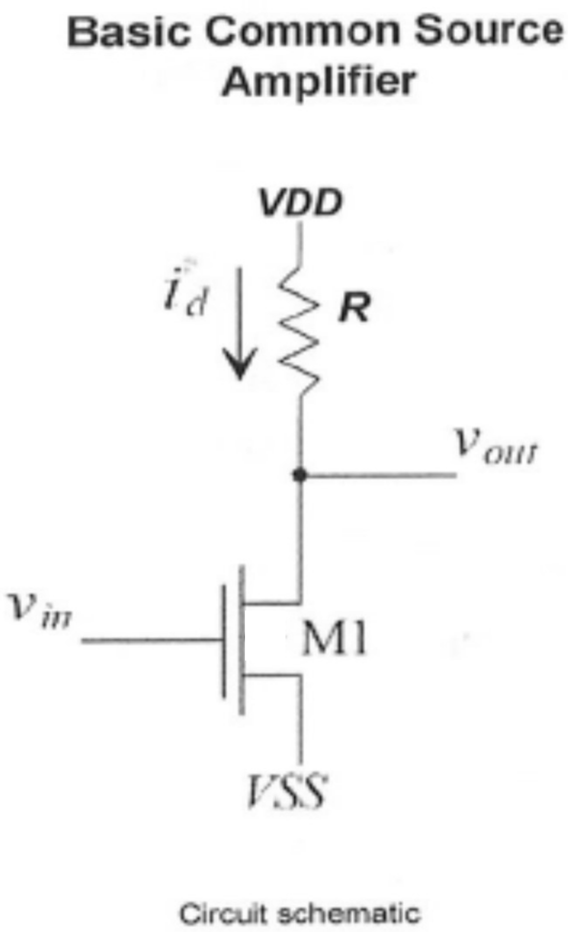
- Source de courant comme charge

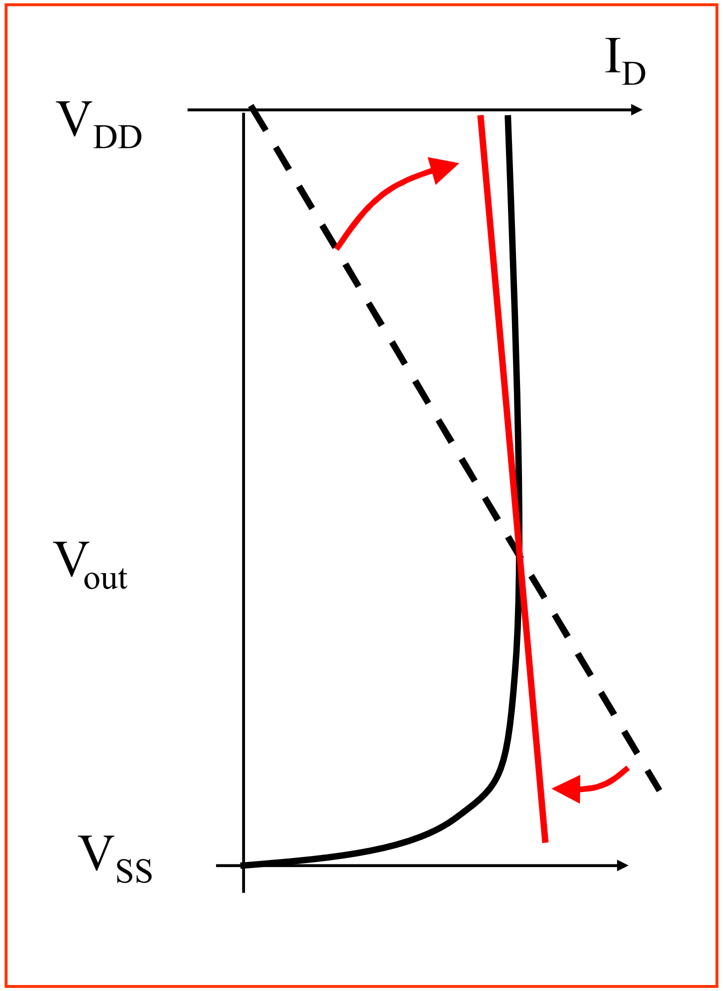
- Gain en boucle ouverte
  très important
  Gain final déterminé par le feedback

- Point de travail fixé par une boucle de feedback



Ampli de tension avec charge idéale



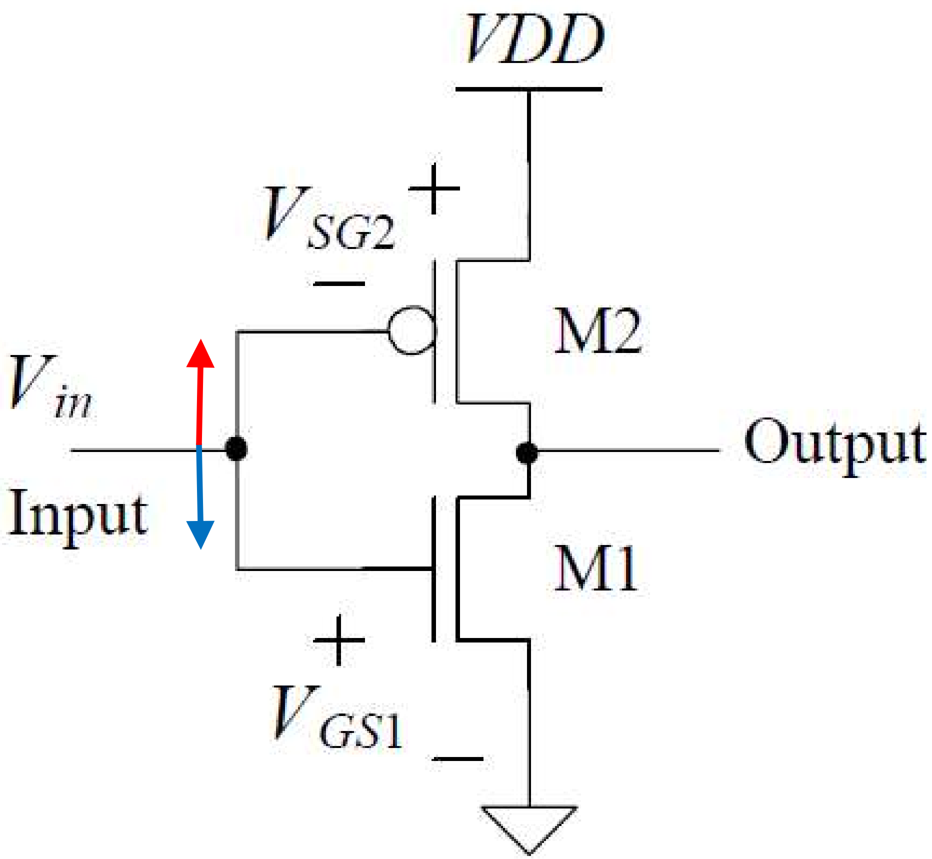


R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

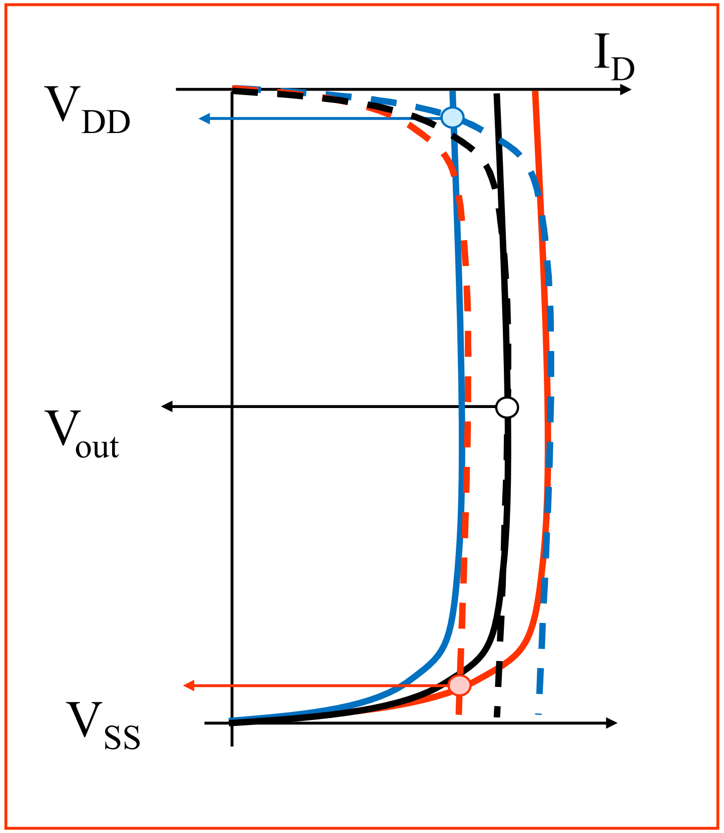
Gain

$$\frac{V_{out}}{V_{in}} = -g_{m1} \cdot R$$

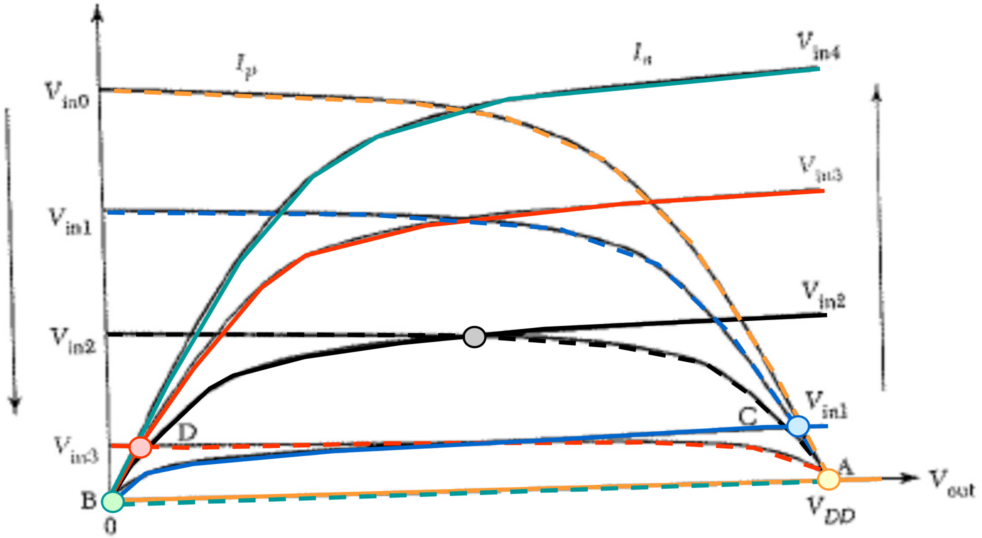
Inverseur CMOS comme ampli de tension (1)

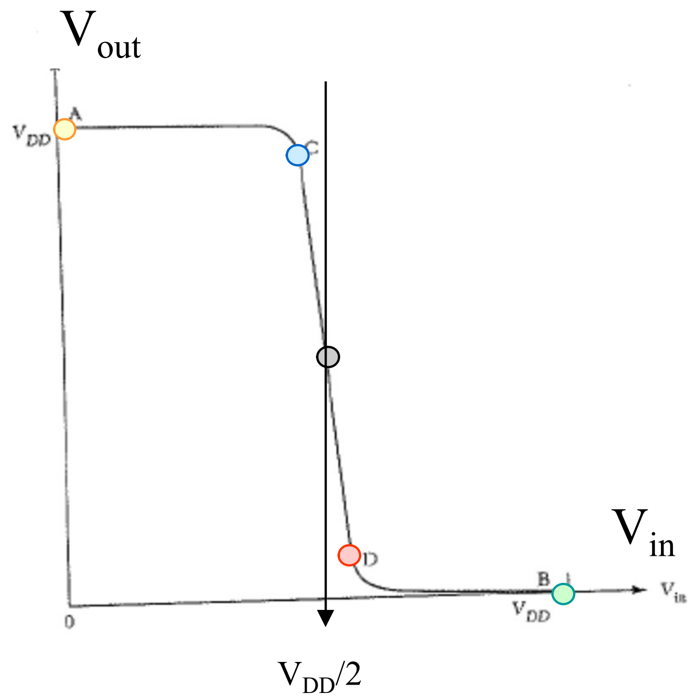


R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press



Inverseur CMOS comme ampli de tension (2)



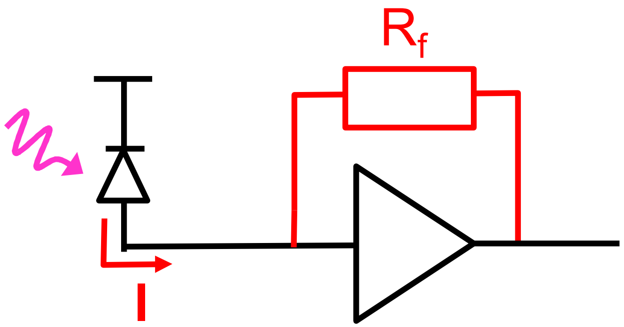


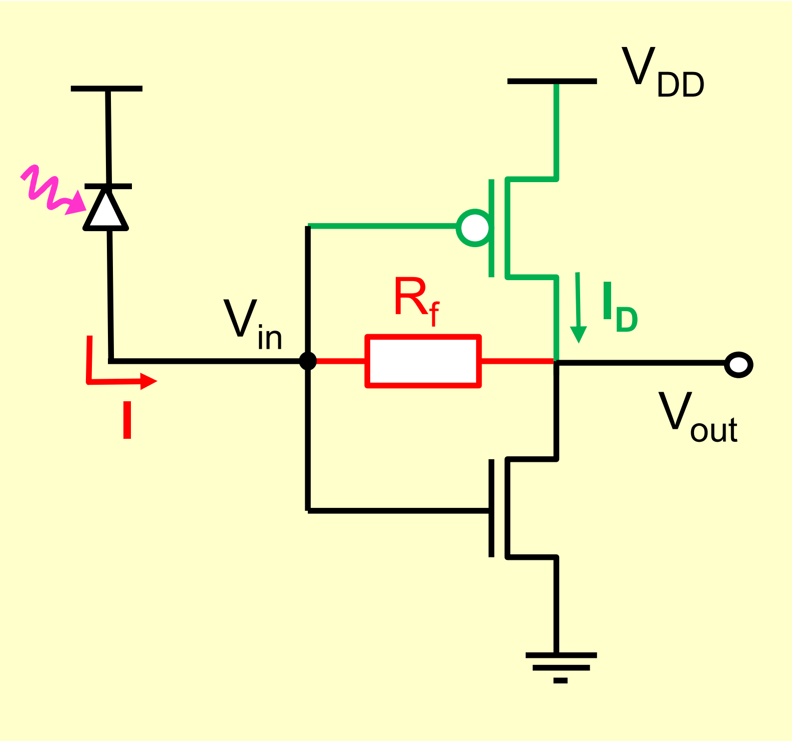
Gain

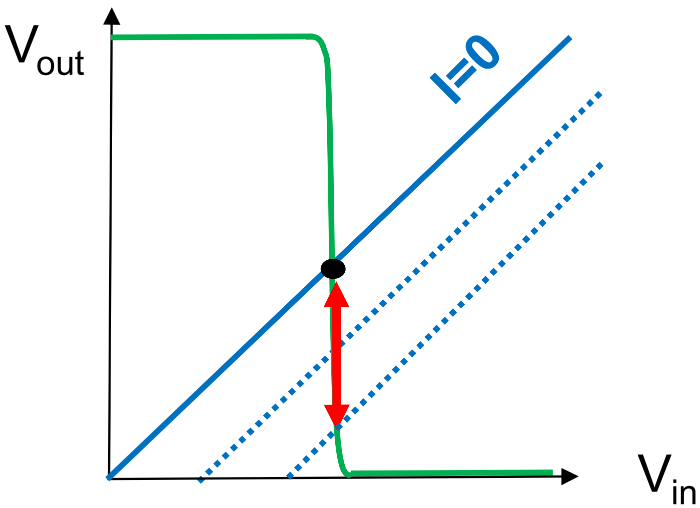
$$\frac{V_{out}}{V_{in}} = -\frac{(g_{m1}+g_{m2})}{g_{DS,1}+g_{DS,2}} = -\left[\frac{g_{m1}}{I_D}+\frac{g_{m2}}{I_D}\right]\cdot\left(\left|V_{A1}\right|^{-1}+\left|V_{A2}\right|^{-1}\right)^{-1}$$

S. Sze, « semiconductor devices, physics and technology », Wiley

Feedback loop dans un transimpédance



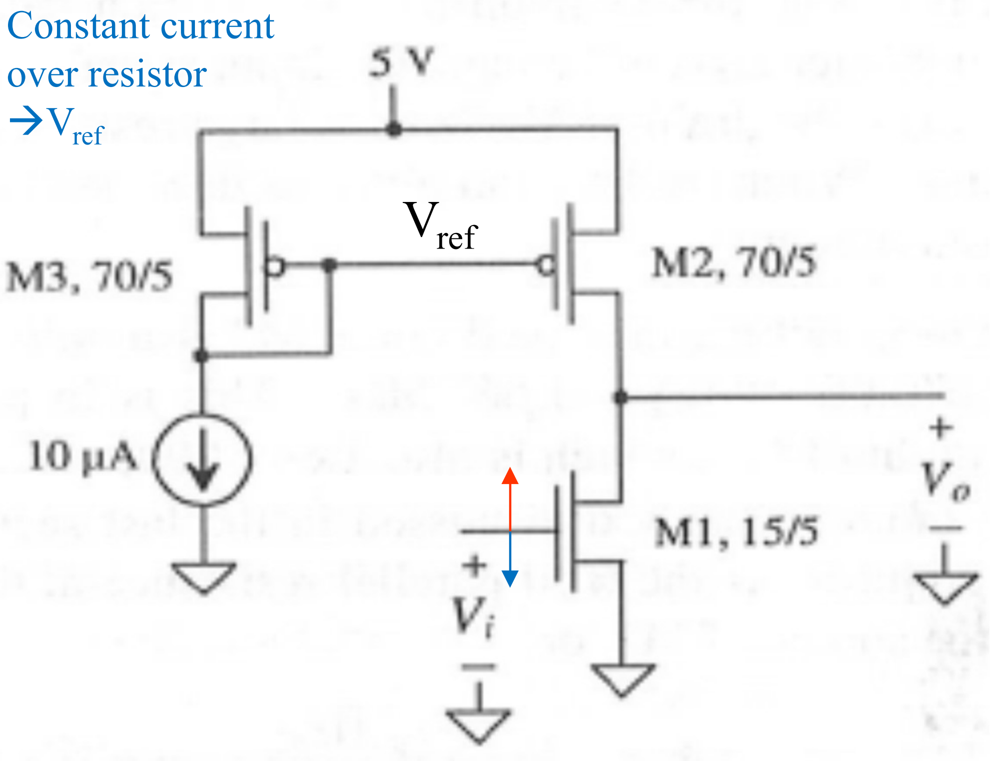


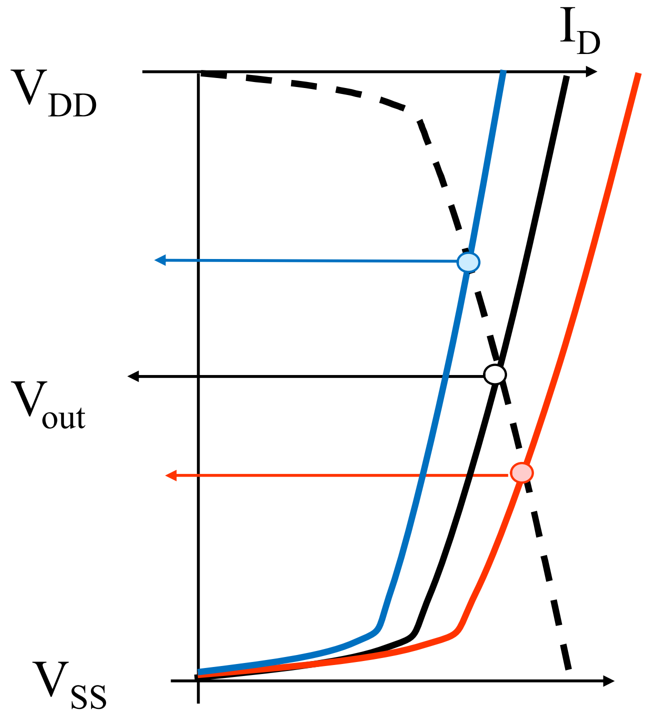


Current source load → huge gain → feedback loop

Ampli de tension chargé par une source de courant

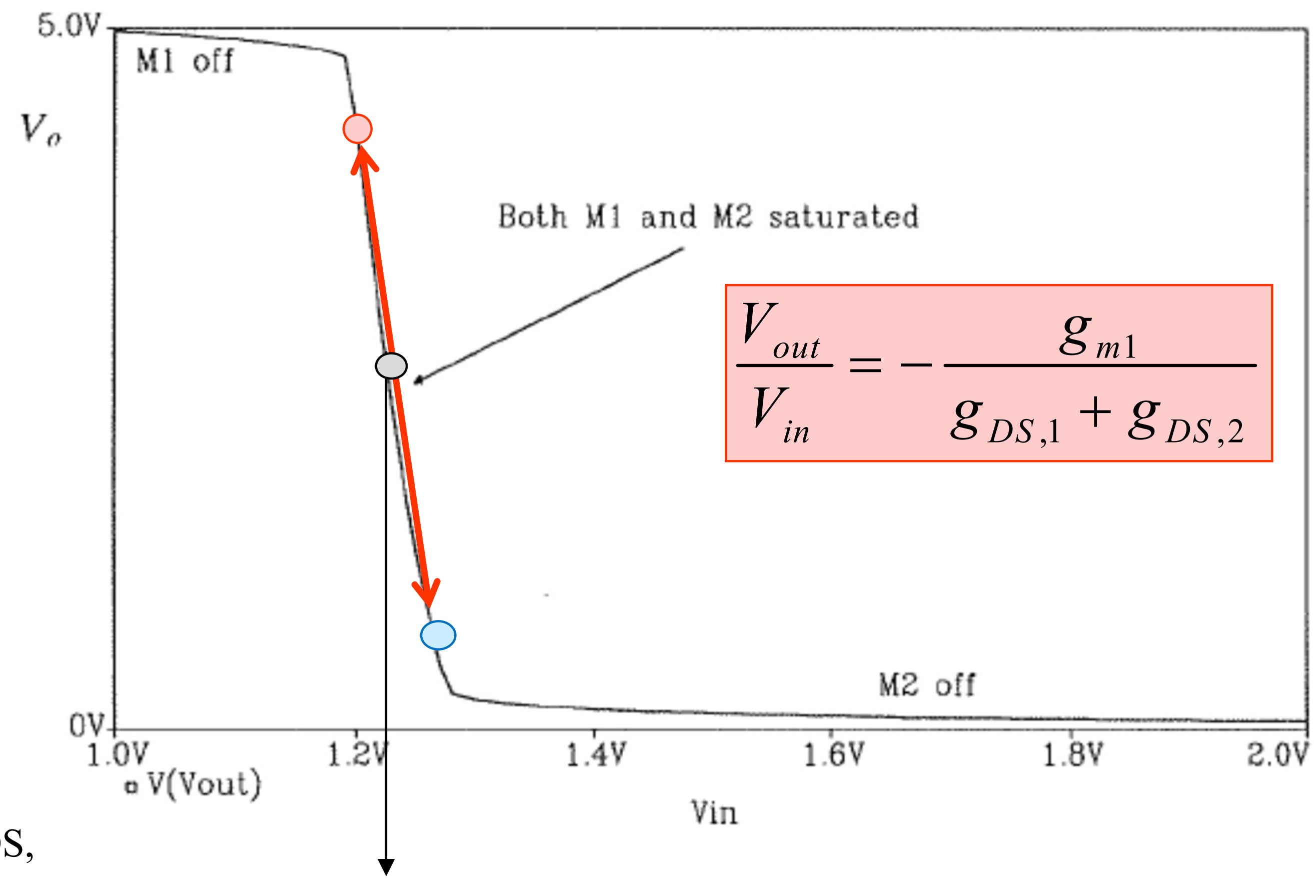
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press





$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{DS,1}+g_{DS,2}} = -\left[\frac{g_{m1}}{I_D}\right]\cdot\left(\left|V_{A1}\right|^{-1}+\left|V_{A2}\right|^{-1}\right)^{-1}$$

Ampli de tension chargé par une source de courant: caractéristique de transfert



$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{DS,1} + g_{DS,2}}$$

R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

Le point de travail peut être choisi lors du design.

Ampli de tension

Design de W/L

Importance du paramètre g_m/I_D

Ampli de tension

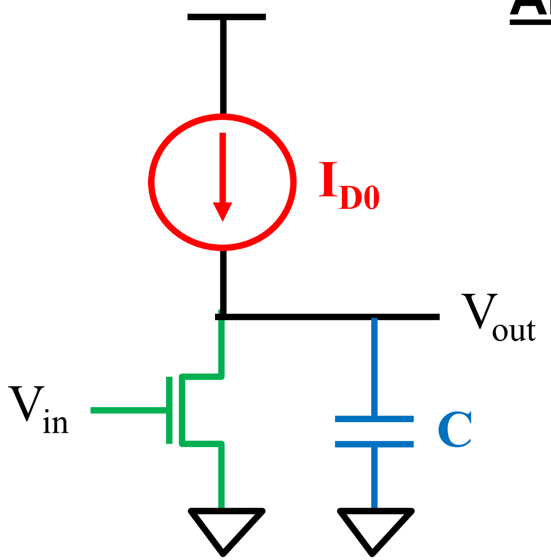
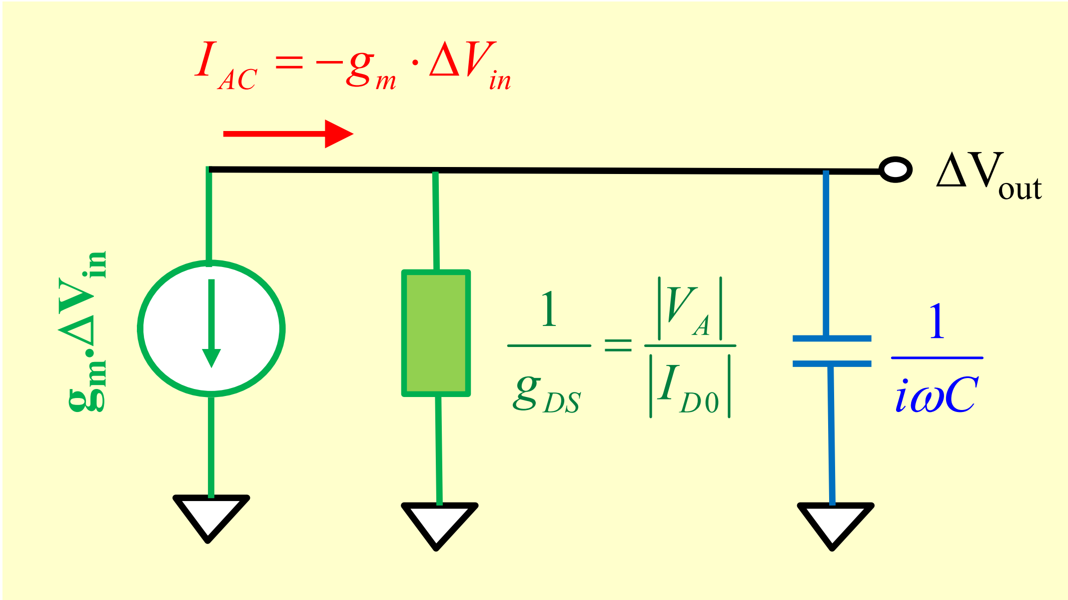


Schéma AC
petit signal



Gain

$$A_V = -g_m \cdot R_{DS} = -|V_A| \cdot \frac{g_m}{I_{D0}}$$

$\Rightarrow$ Déterminer V_G-V_{M0} $\Rightarrow$ Déterminer $\frac{I_{D0}}{(W/L)}$ $\Downarrow$

Bande passante

$$2\pi\Delta f = \frac{1}{R_{DS}C} = \frac{1}{|V_A| \cdot C} \cdot |I_{D0}|$$

$\Rightarrow$ Déterminer I_{D0} $\Rightarrow$ **W/L**

Gain en tension et rapport g_m/I_D

$$A_V = -g_m \cdot R_{DS} = -\left|V_A\right| \cdot \frac{g_m}{I_{D0}}$$

Le rapport g_m/I_D ne dépend que de (V_G-V_{M0}) et de paramètres physiques et technologiques

Inversion faible

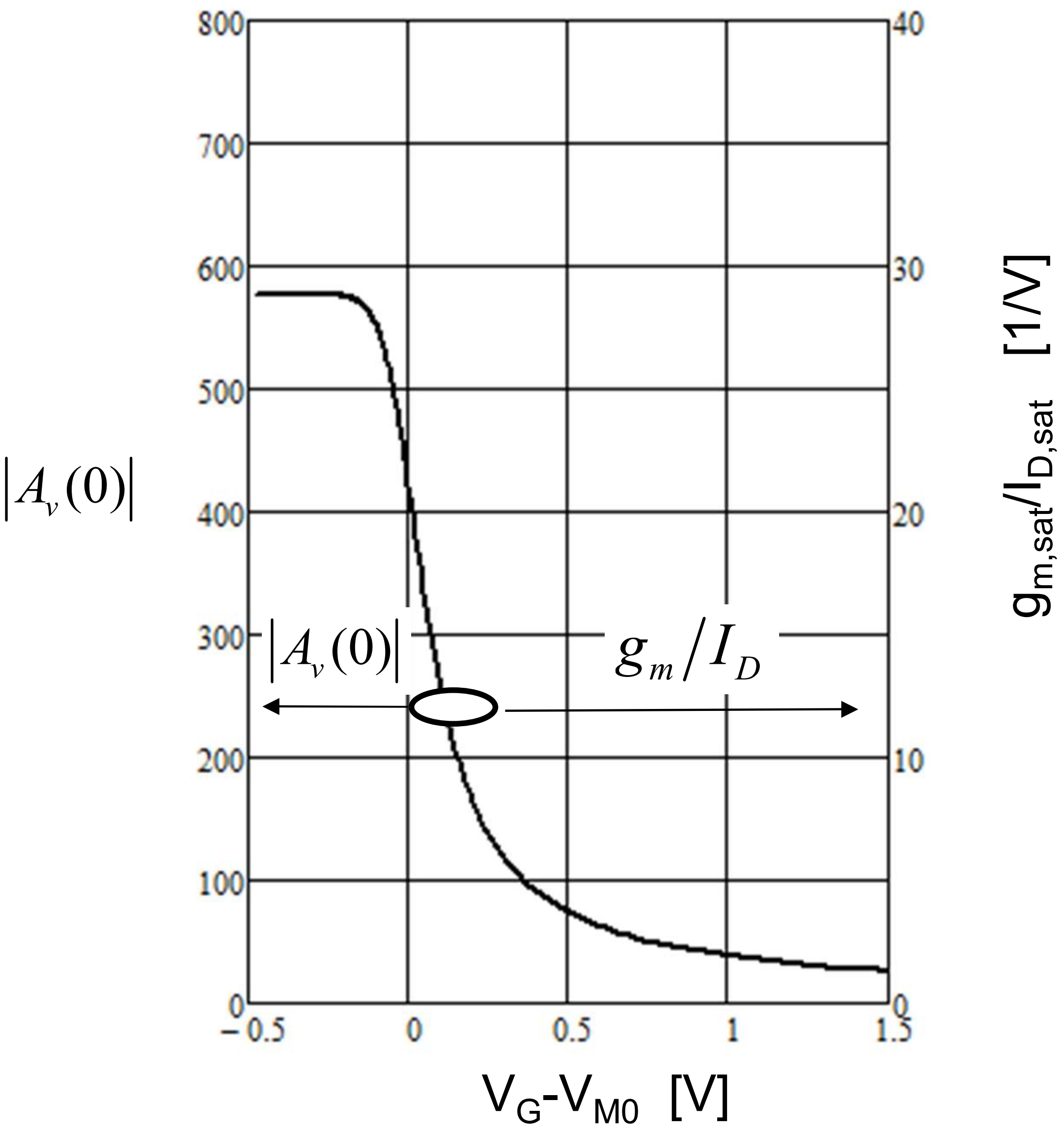
$$\frac{g_m}{I_D} \cong \frac{1}{n \cdot U_{th}}$$

Inversion forte

$$\frac{g_m}{I_D} \cong \frac{2}{V_G - V_{M0}}$$

⇒ **Pour un gain donné on peut déterminer la valeur de (V_G-V_{M0})**

Transconductance et gain en tension A_v



$$|A_v(0)| = |V_A| \cdot \frac{g_m}{I_D}$$

C_{ox}=3fF/um^2 u_n=1000cm^2/V.s
n=4/3 VA= - 20V
U_T=26mV

Rapport $I_D/(W/L)$

Le rapport $I_D/(W/L)$ ne dépend que de $(V_G\text{-}V_{M0})$ et de paramètres physiques et technologiques

Inversion faible

$$\frac{I_D}{(W/L)} \cong \left(2n\mu_n C_{ox} U_{th}^2\right) \cdot e^{\frac{V_G - V_{M0}}{nU_{th}}}$$

Inversion forte

$$\frac{I_D}{(W/L)} \cong \left(\frac{\mu_n C_{ox}}{2n}\right) \cdot \left(V_G - V_{M0}\right)^2$$

⟹ **Pour un gain donné on peut déterminer la valeur de** $\frac{I_D}{(W/L)}$

Bande passante et rapport W/L

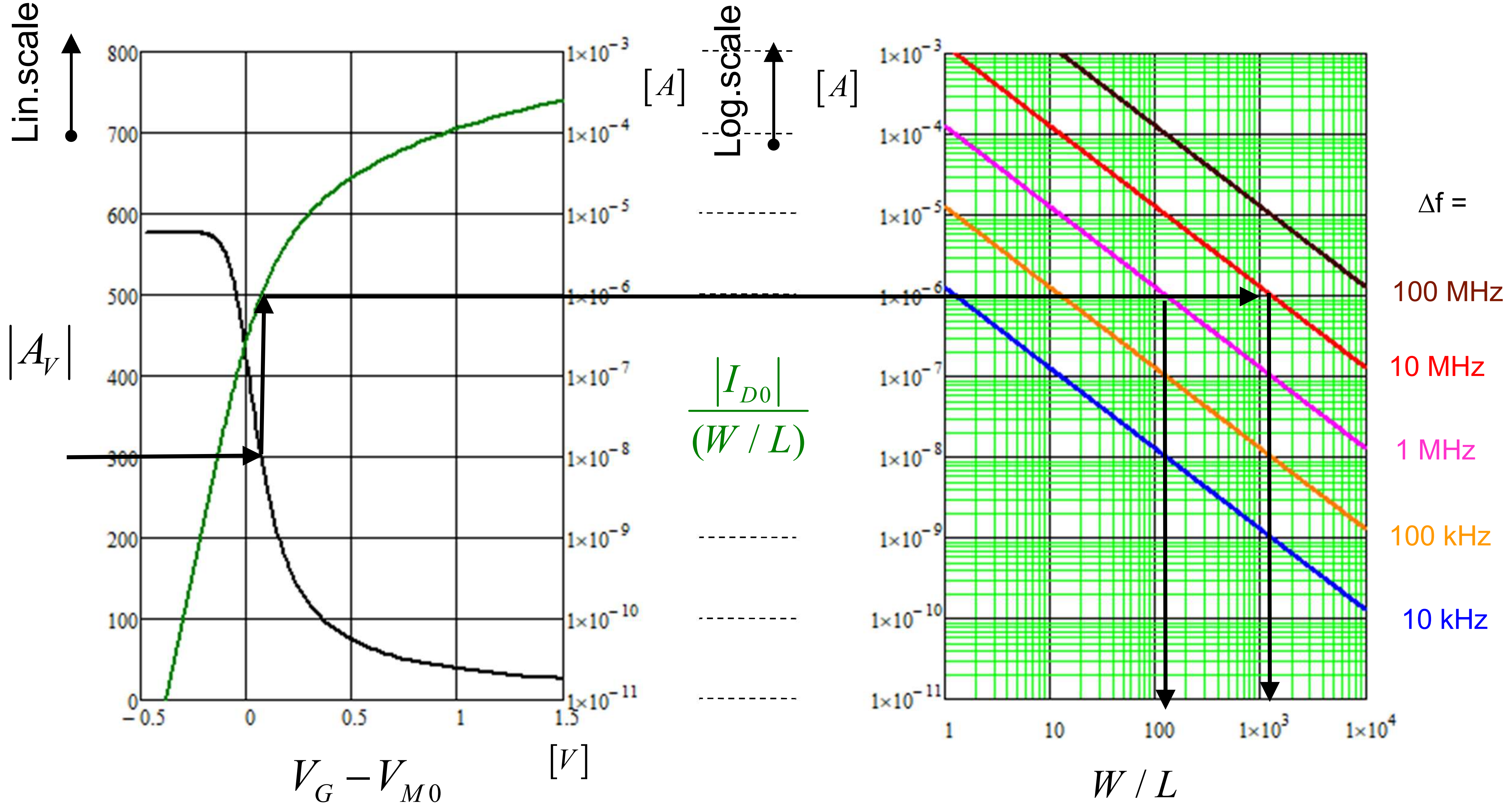
$$2\pi\Delta f = \frac{1}{R_{DS}}\frac{1}{C} = \frac{|I_{D0}|}{|V_A|}\cdot\frac{1}{C}$$

$$\Downarrow$$

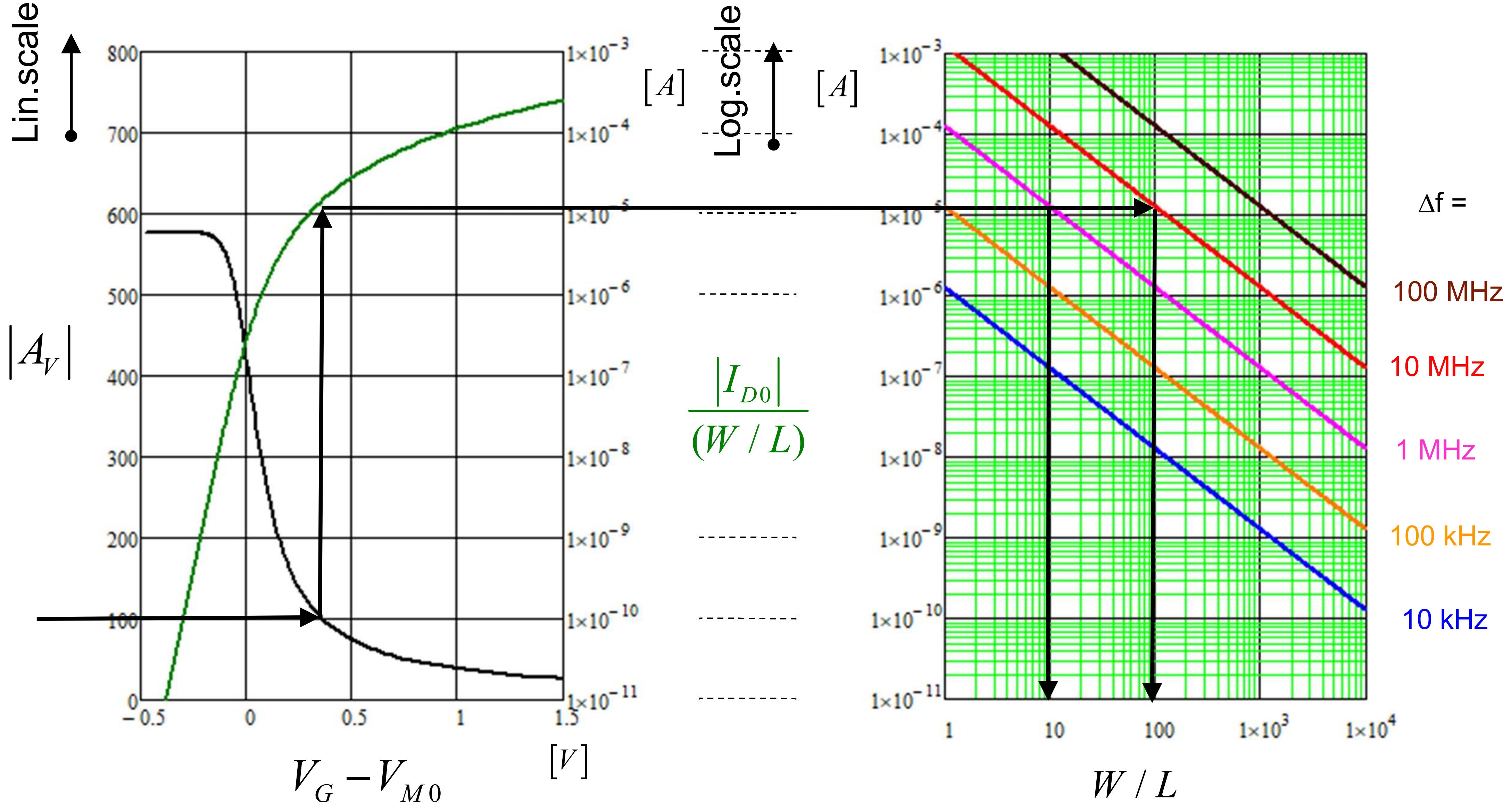
$$\frac{I_D}{(W/L)} = \left(2\pi|V_A|C\right)\cdot\Delta f\cdot\frac{1}{(W/L)}$$

$\Rightarrow$ **La valeur $\frac{I_D}{(W/L)}$ et la bande passante Δf donnent le rapport W/L**

C_{ox}=3fF/um^2 u_n=1000cm^2/V.s
V_A= - 20V n=4/3
C=1pF U_T=26mV



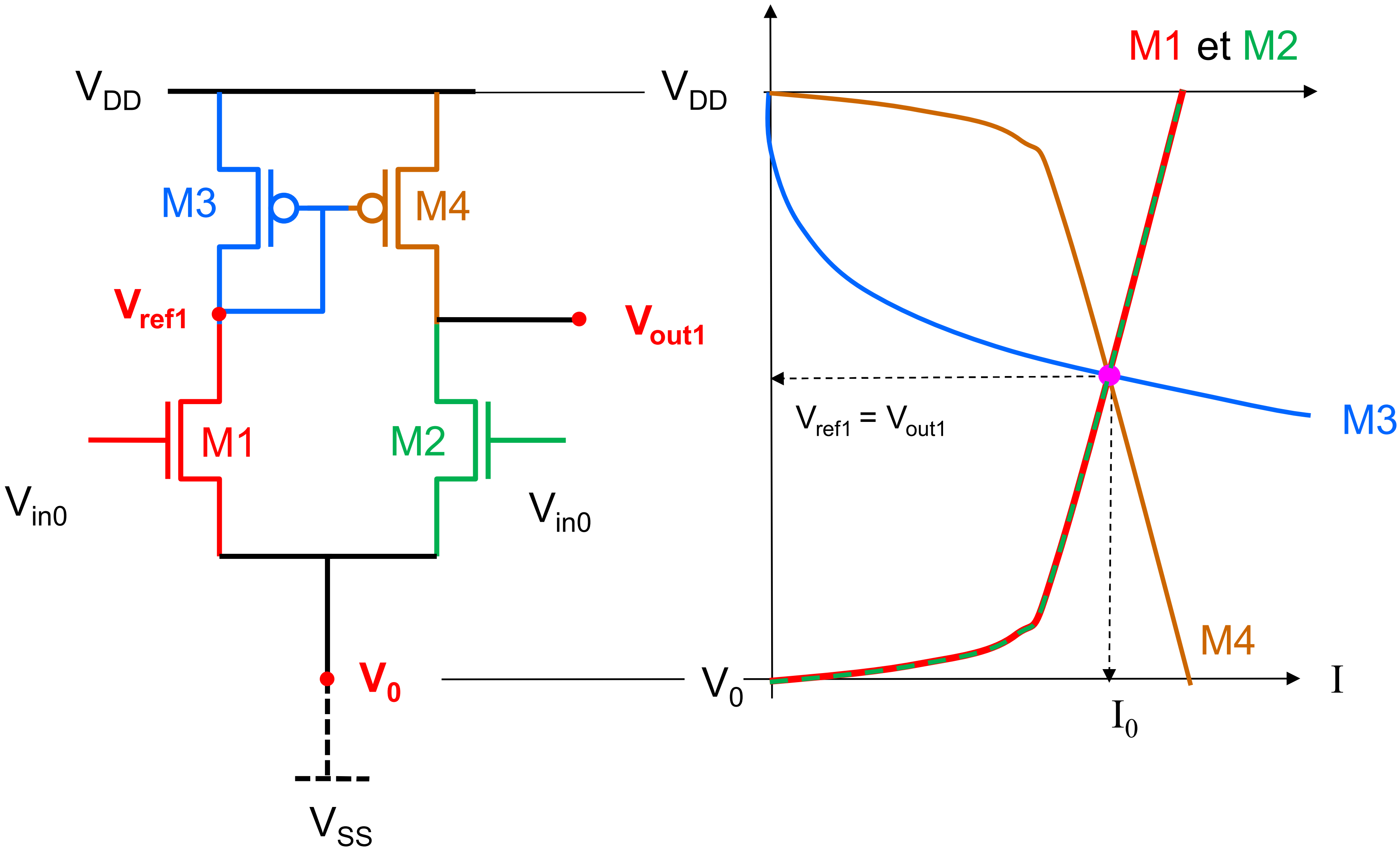
C_{ox}=3fF/um^2 u_n=1000cm^2/V.s
V_A= - 20V n=4/3
C=1pF U_T=26mV



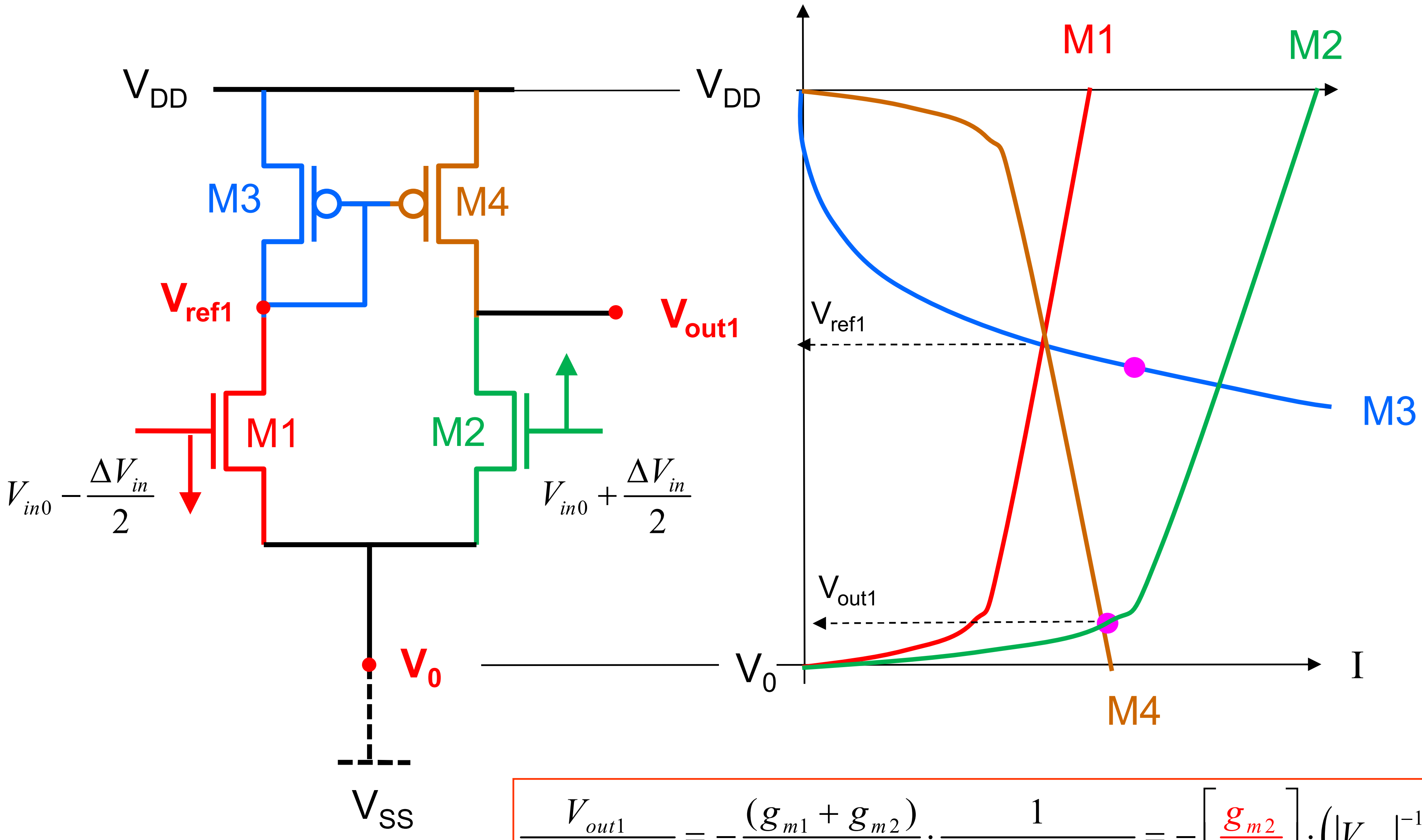
Ampli différentiel

Et Opam

Differential amplifier: point de travail

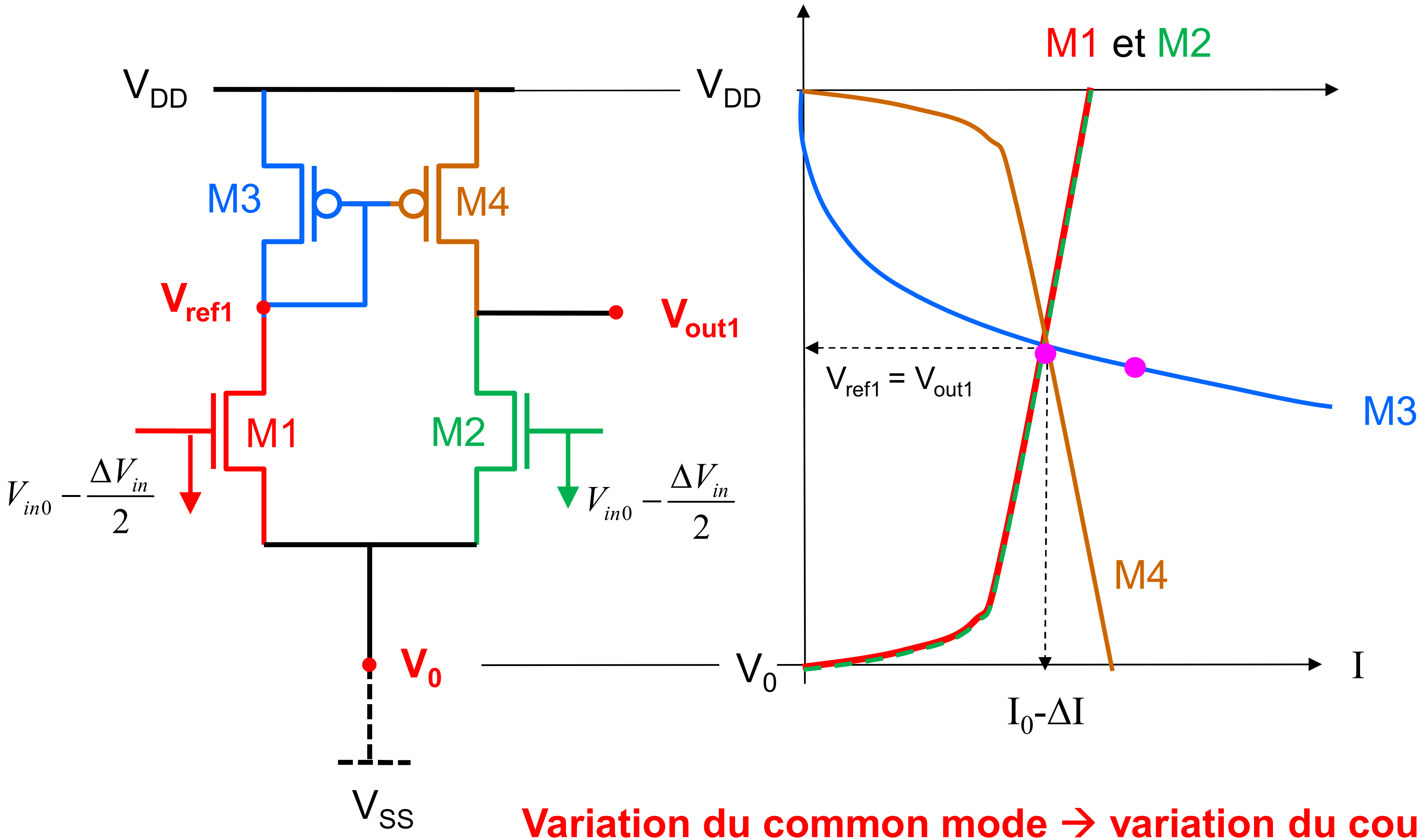


Differential amplifier:
analyse du mode différentiel



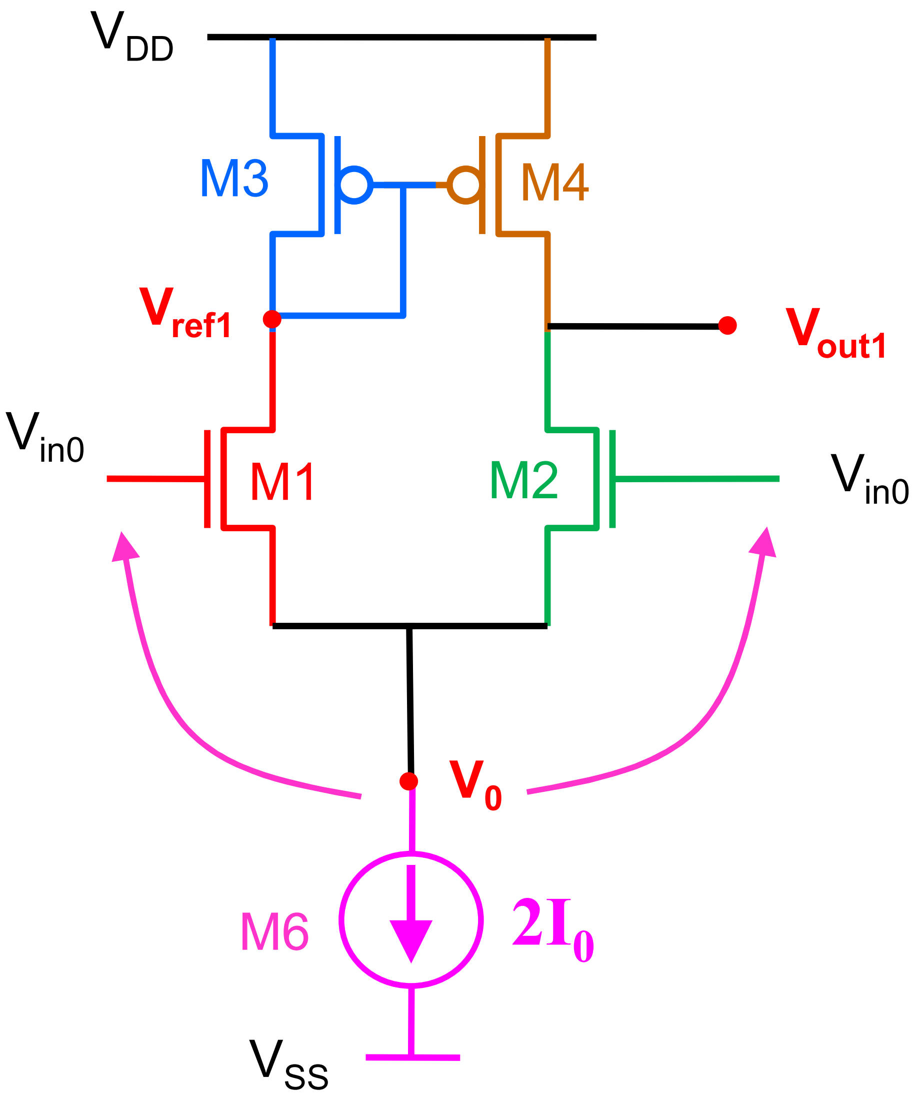
$$\frac{V_{out1}}{V_{in,2} - V_{in,1}} = -\frac{(g_{m1} + g_{m2})}{2} \cdot \frac{1}{g_{DS,4} + g_{DS,2}} = -\left[\frac{g_{m2}}{I_{D2}}\right] \cdot \left(|V_{A4}|^{-1} + |V_{A2}|^{-1}\right)^{-1}$$

Differential amplifier: analyse du mode commun



Variation du common mode → variation du courant
→ Variation du gain du mode différentiel

Differential amplifier: introduction d'une source de courant



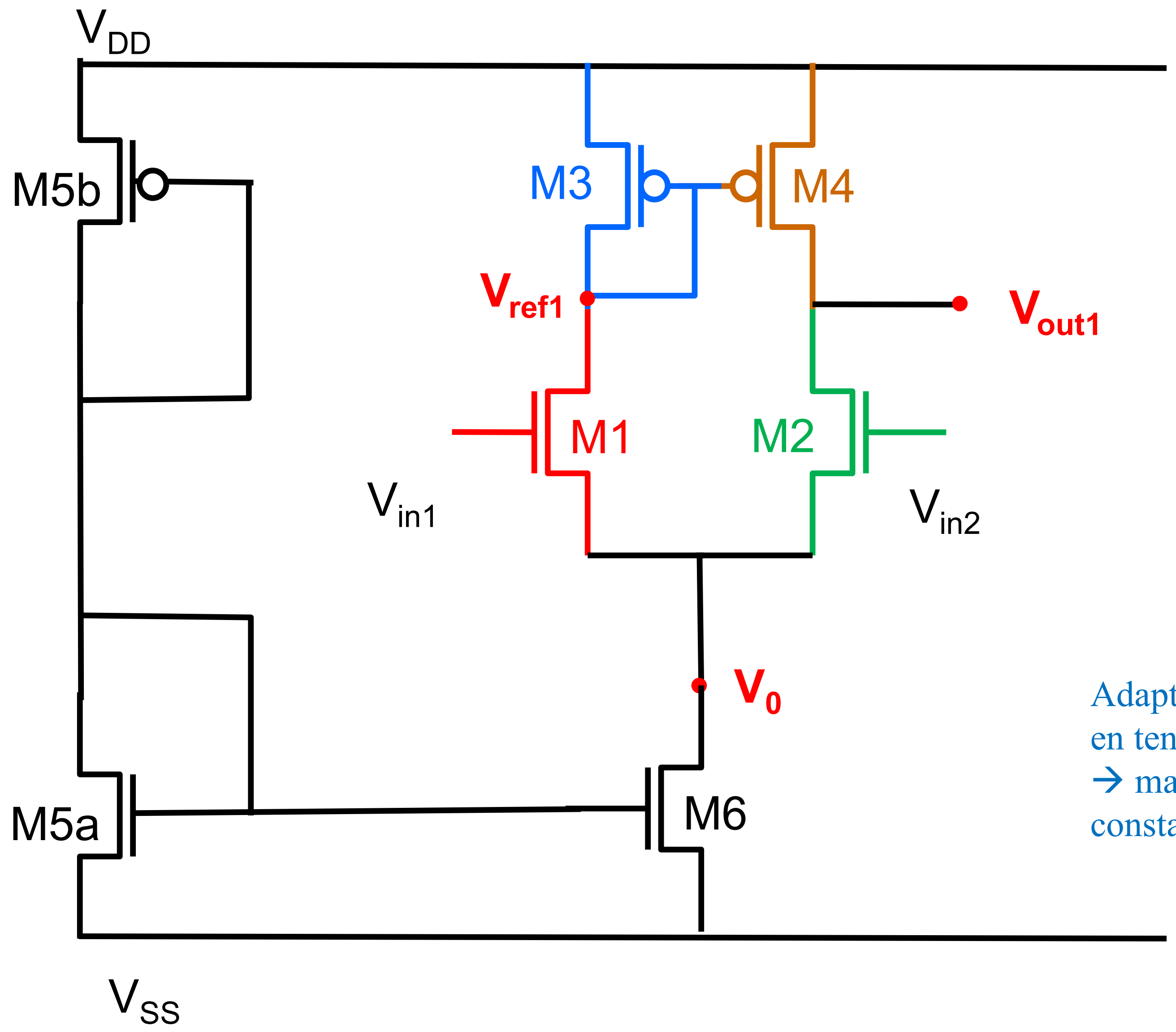
Ajouter une source de courant

→ Maintenir la tension V_{in0}-V_0 constante

→ Le gain différentiel est fixe

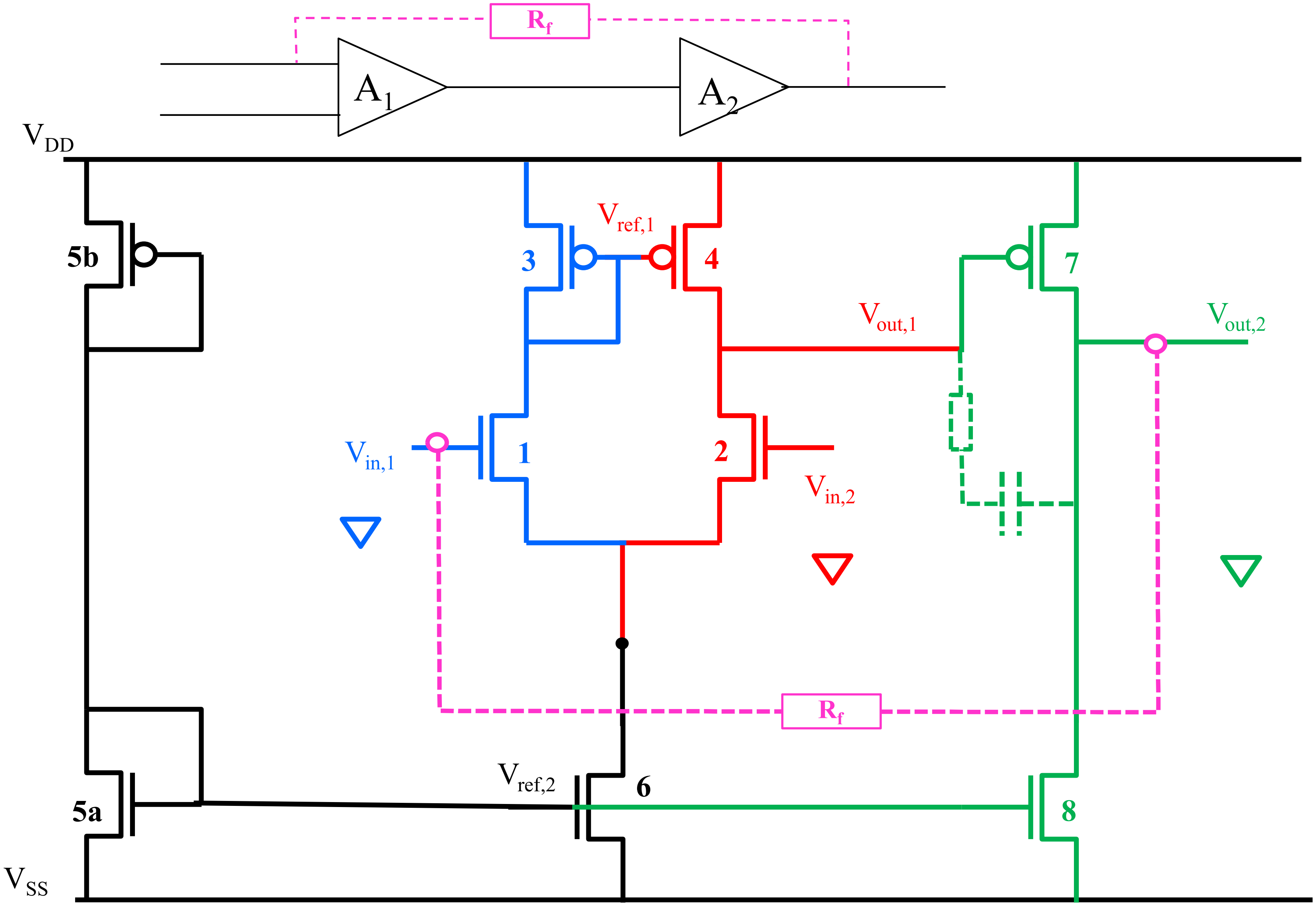
$$\frac{g_{m1,2}}{I_0} = \frac{2}{\left(V_{in0} - V_0\right) - V_{M0}} = \left(\sqrt{2\frac{W}{L}\mu_n C_{ox} n}\right) \cdot \frac{1}{\sqrt{I_0}}$$

Differential amplifier: introduction d'une source de courant



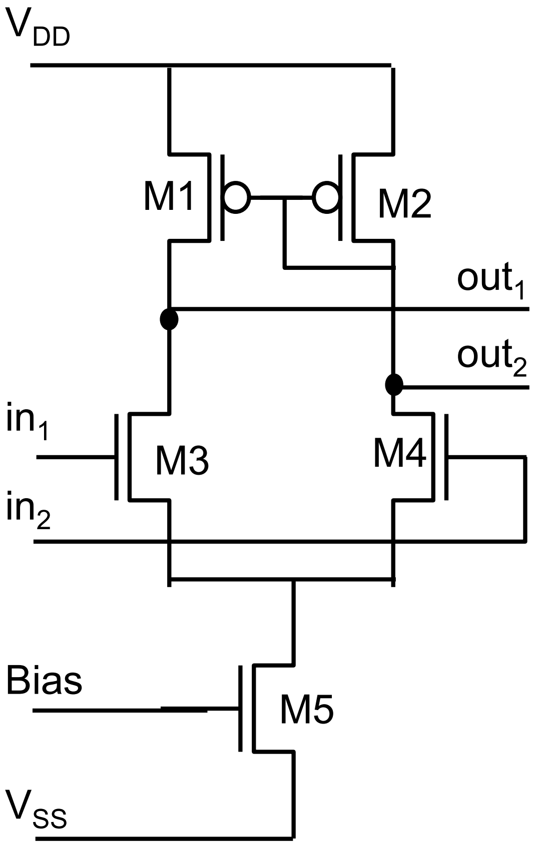
Adapter la tension en V_0 en tenant I_6 constant
→ maintenir g_{m1} et g_{m2} constantes.

Op-Amp: two stages (2)

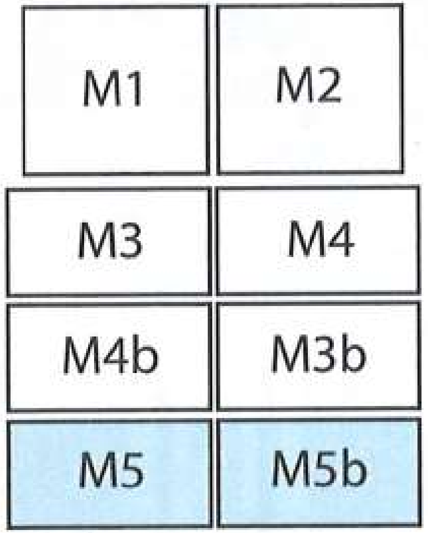


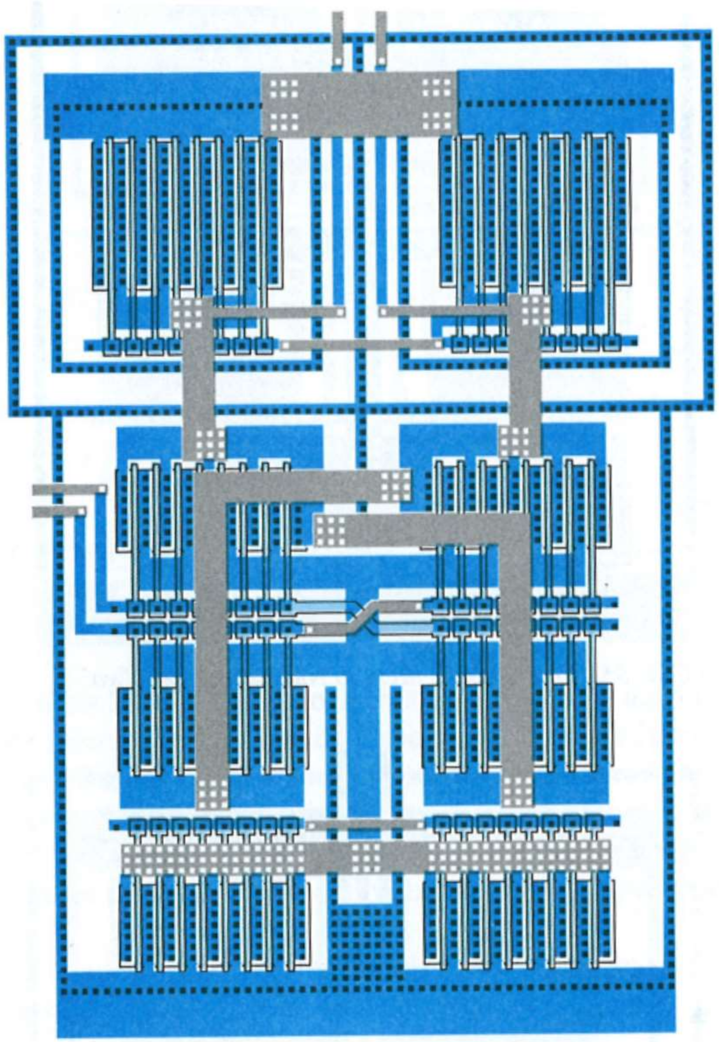
Exemple de layout

Schématique



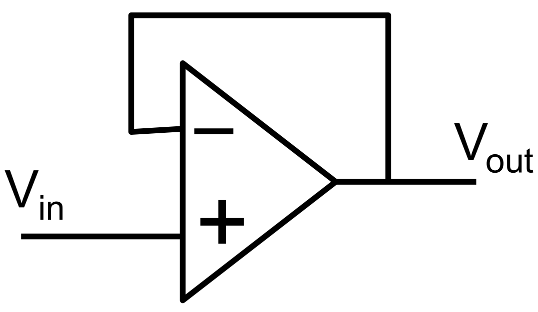
Ampli différentiel



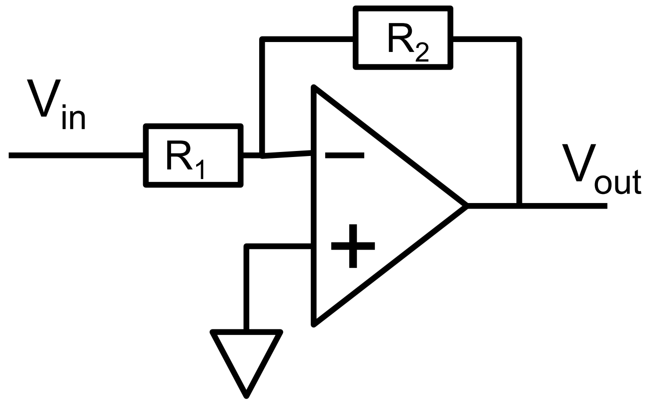


Ch. Saint, « IC mask design »,
2002 McGraw-Hill

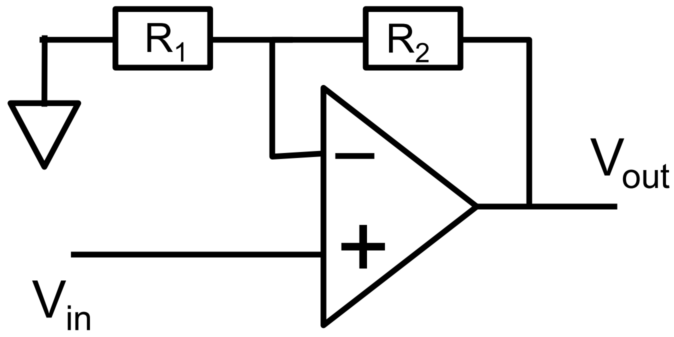
Exemples: Opam avec boucle de feedback



Suiveur



Ampli inverseur



Ampli non-inverseur

$$V_{out} = V_{in}$$

$$V_{out} = -\frac{R_2}{R_1} \cdot V_{in}$$

$$V_{out} = \left(\frac{R_1 + R_2}{R_1} \right) \cdot V_{in}$$

. . .

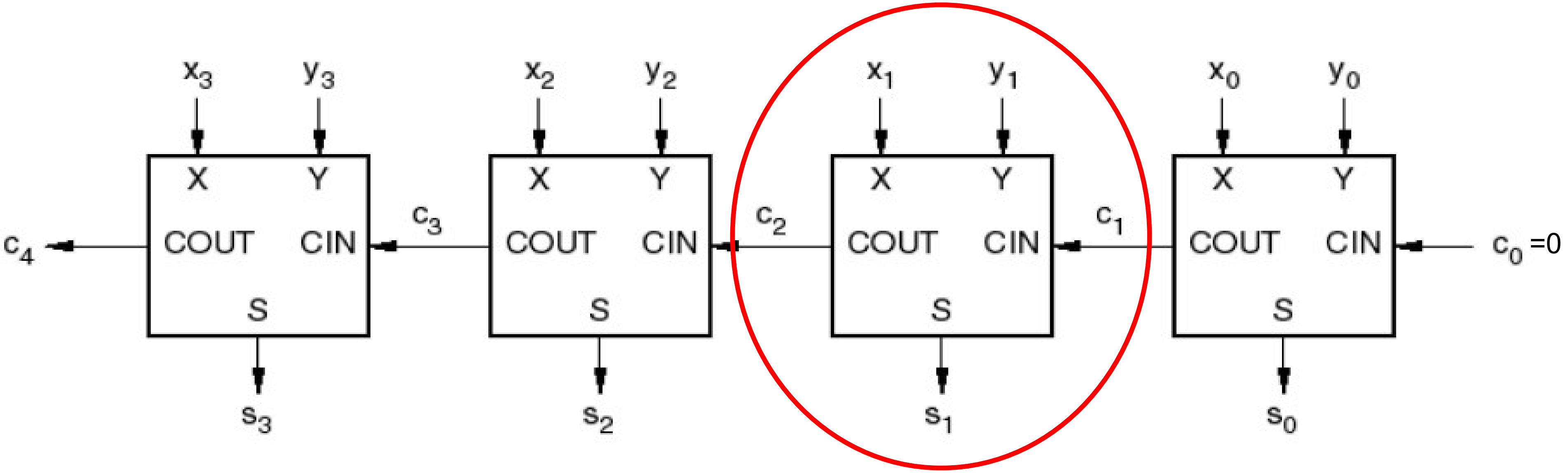
Exercice E12.2: Addition binaire

Principe

$$
\begin{array}{rccccc}
 & c_4 & c_3 & c_2 & c_1 & 0 \\
 & & x_3 & x_2 & x_1 & x_0 \\
+ & & y_3 & y_2 & y_1 & y_0 \\
\hline
= & c_4 & s_3 & s_2 & s_1 & s_0
\end{array}
$$

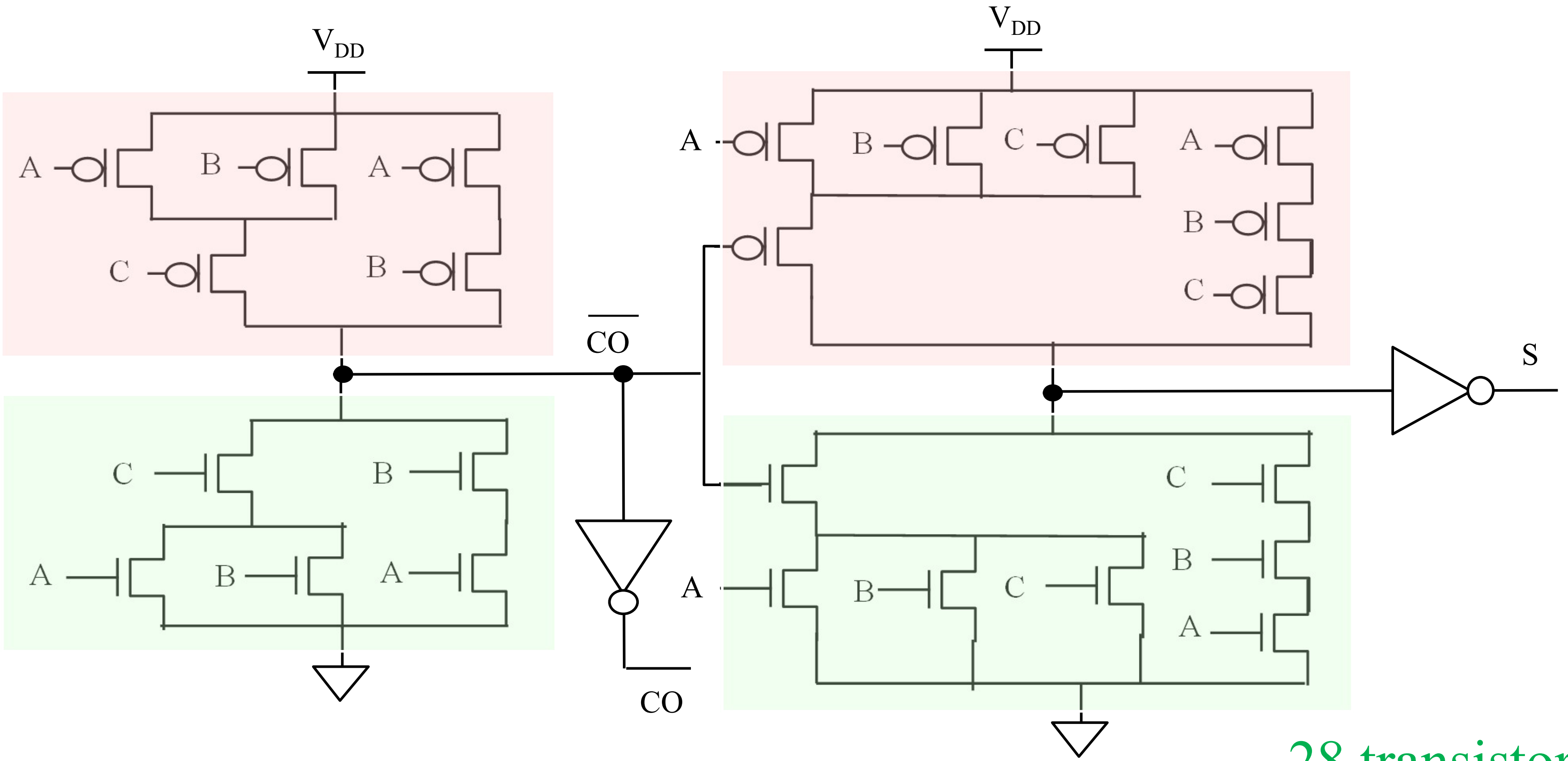
Exemple d'addition binaire:
1101 + 1001 = 10110

$$
\begin{array}{rccccc|l}
 & 1 & 0 & 0 & 1 & 0 & C \\
 & & 1 & 1 & 0 & 1 & A \\
+ & & 1 & 0 & 0 & 1 & B \\
\hline
= & 1 & 0 & 1 & 1 & 0 & S
\end{array}
$$



Exercice E12.2: « Full adder »

Calculez la table de vérité et montrez qu'elle correspond à une addition binaire

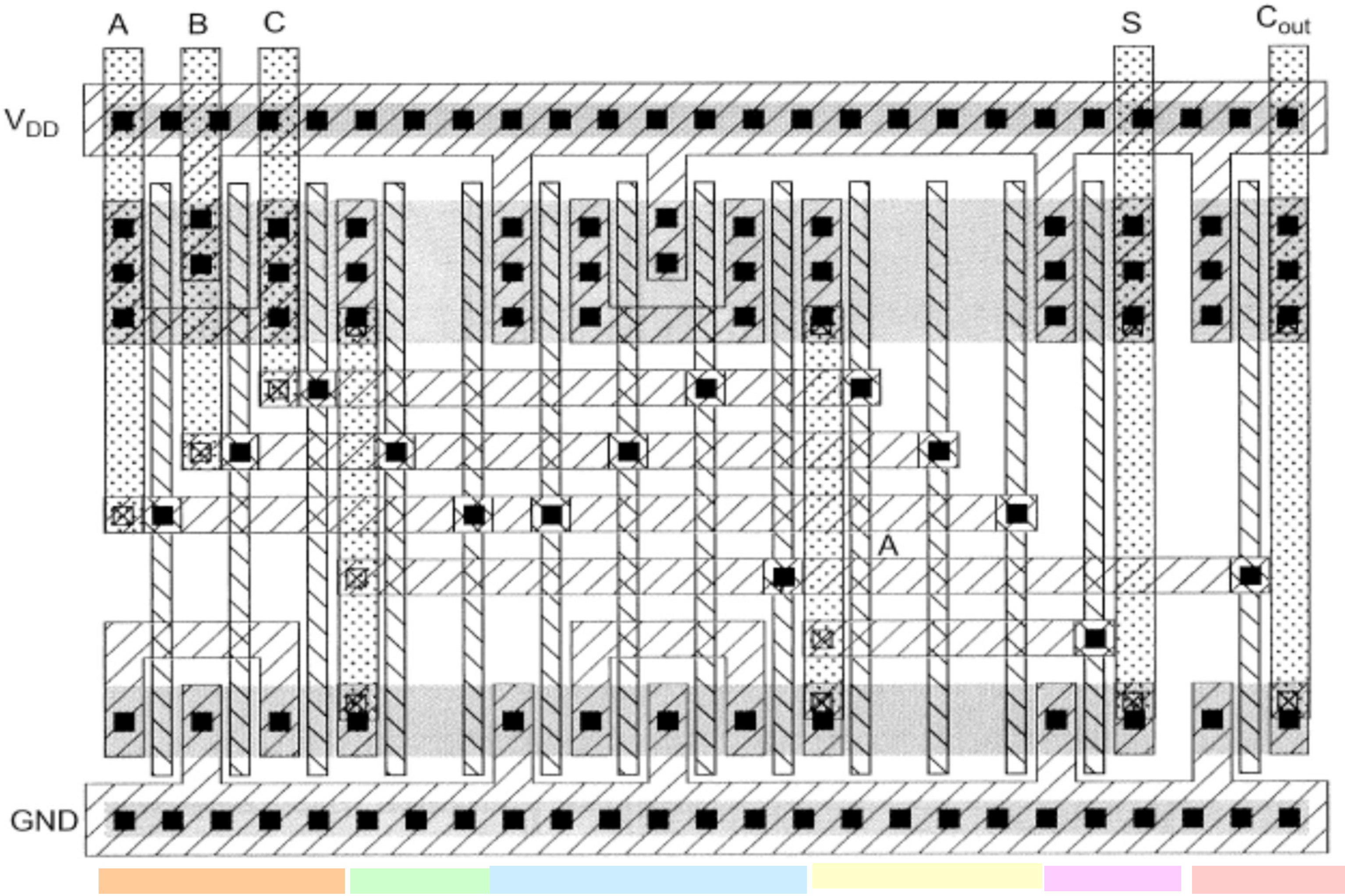


28 transistors

Zimmermann, Fichtner, IEEE journal of solid-state circuits, Vol. 32, No. 7, pp. 1-12.

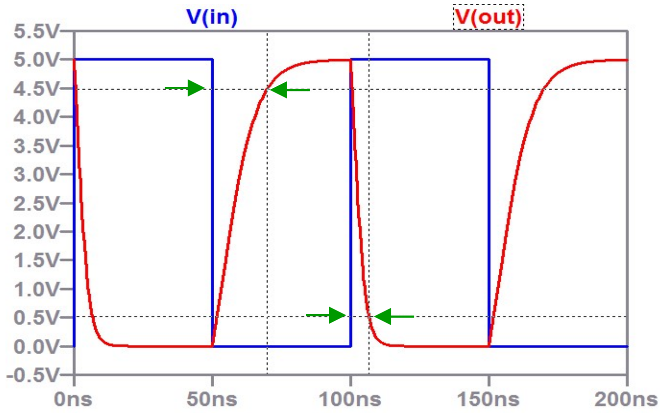
Layout du « full adder » de l'exercice E12.2

Weste/Harris, « CMOS VLSI design », Addison-Wesley

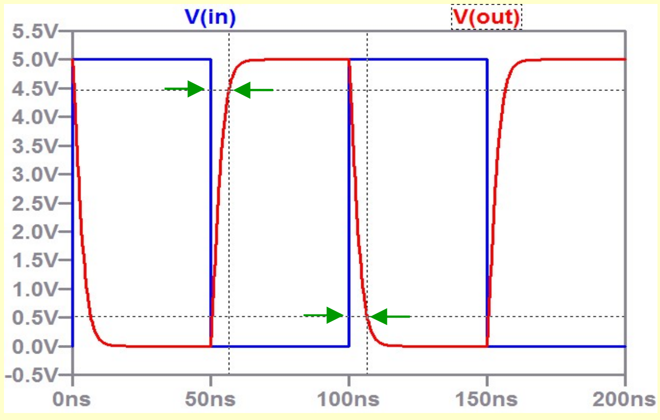


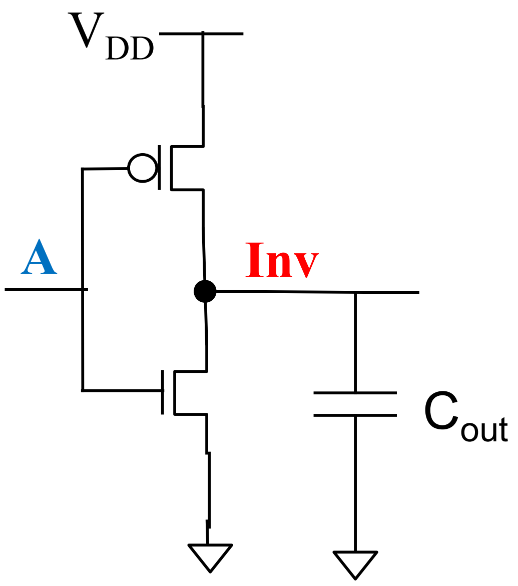
Exercice 12.3: dimensionnement (1)

Wp=Wn

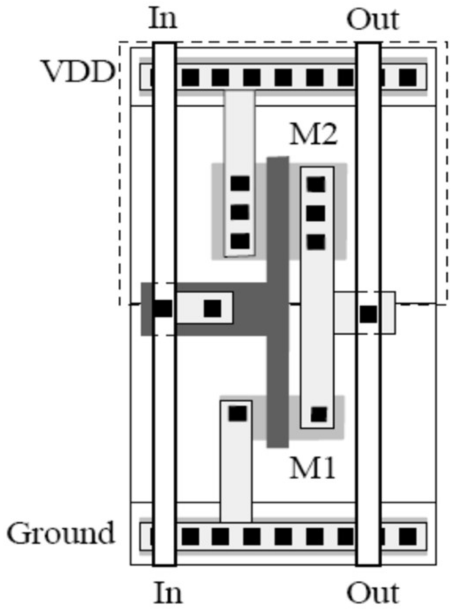


Wp= 3 Wn





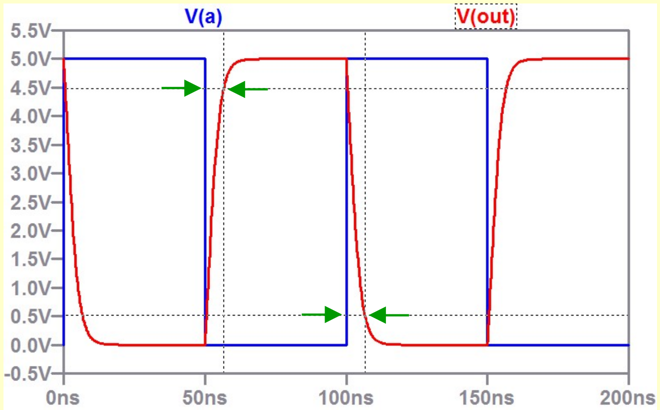
Inverseur



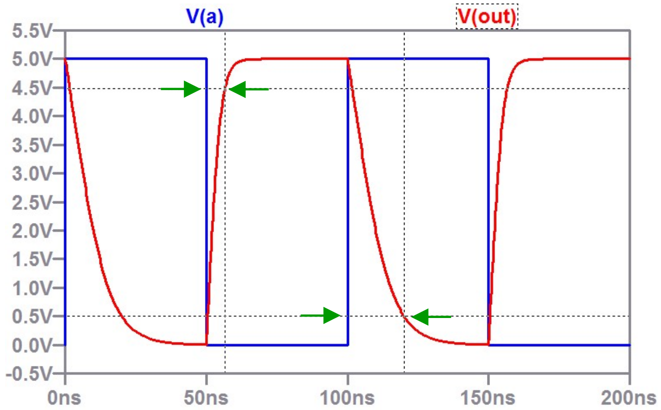
Wp= 3 Wn

Exercice 12.3: dimensionnement (2)

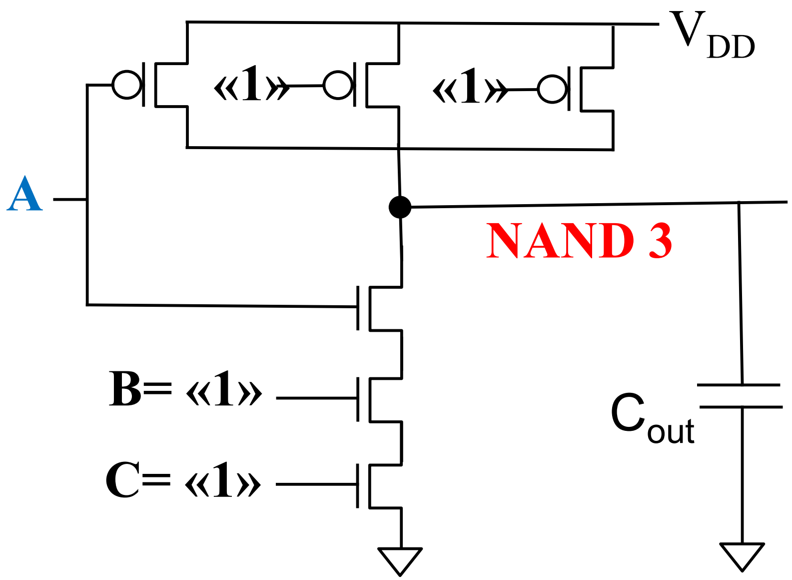
Wp= Wn

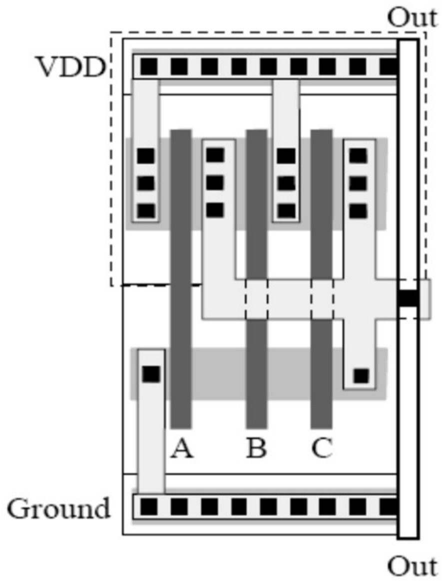


Wp= 3 Wn



NAND 3

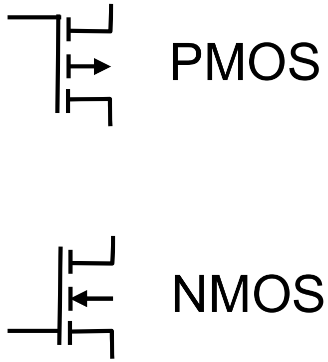


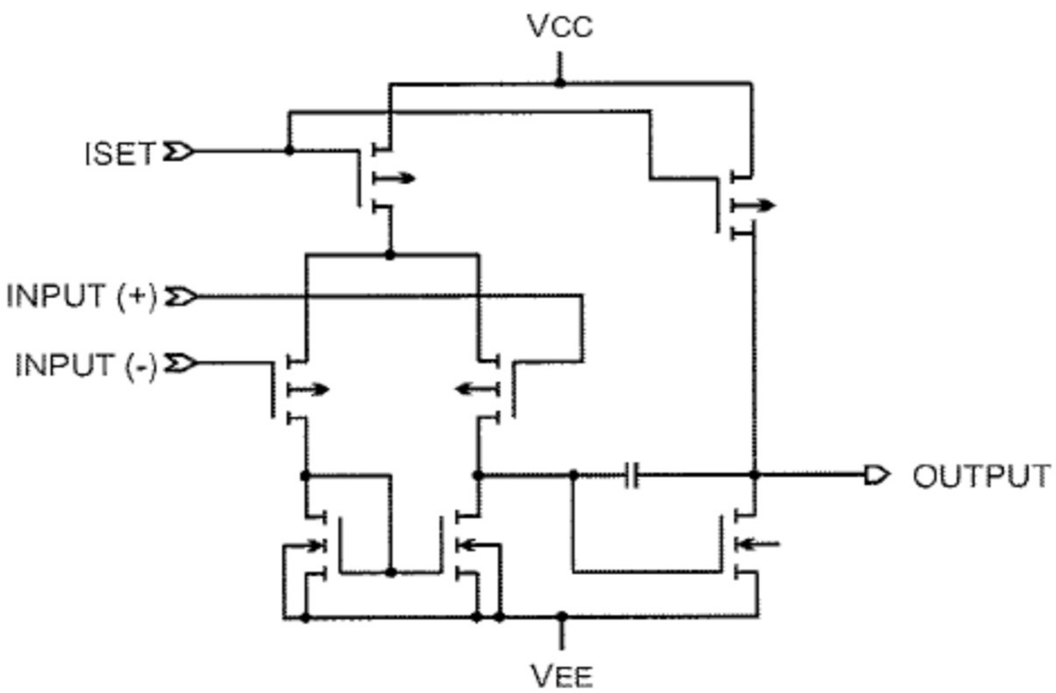


Wp= 3 Wn

Exercice 13.1 A

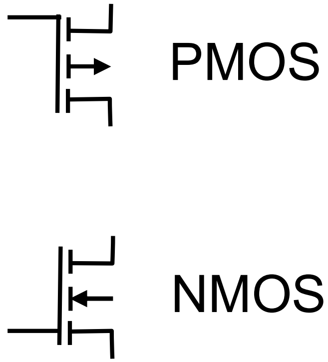
Interprétez ce schéma:



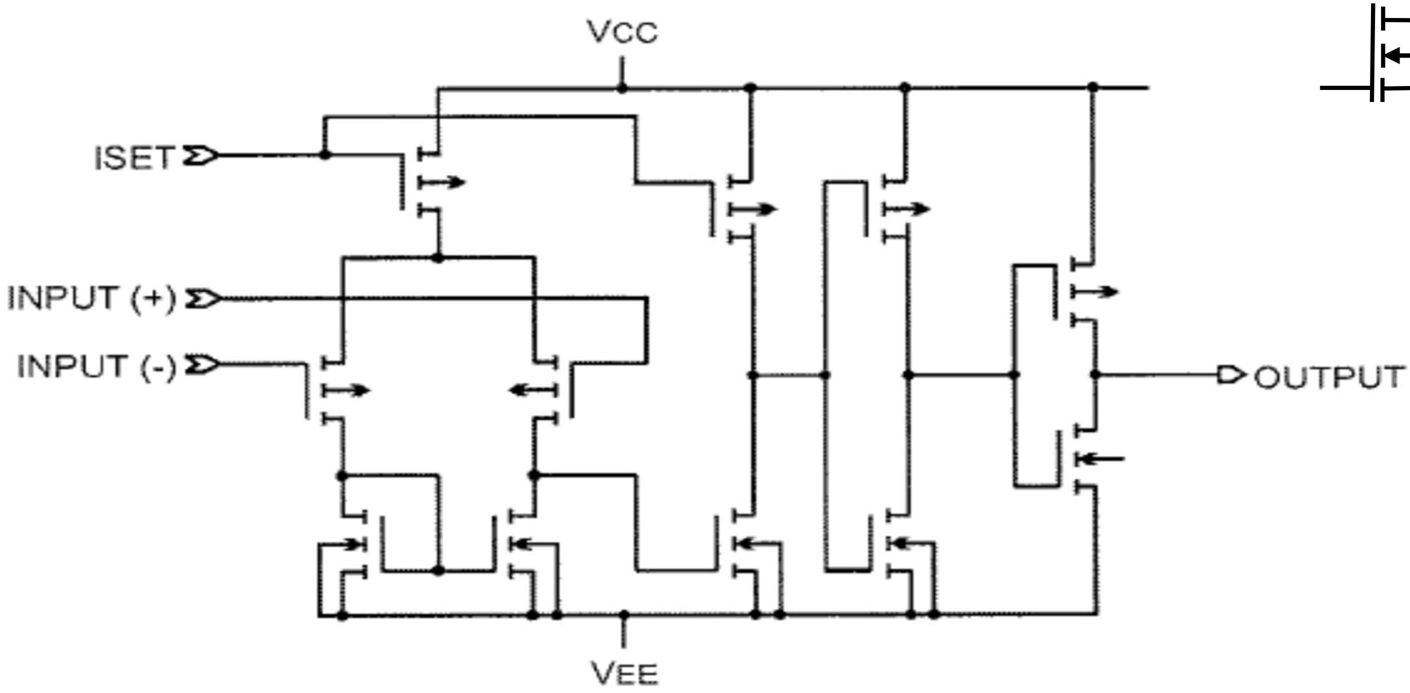


MC14573 from Motorola Semiconductor

Exercice 13.1 B



Interprétez ce schéma:



MC14574 from Motorola Semiconductor

Exercice E13.2:
Ampli de tension avec NMOS

Utilisez un NMOS comme ampli de tension.
Inspirez-vous du chapitre 7 sur les BJT.
Remplacez le transistor bipolaire par un NMOS !