PHYSIQUE DES COMPOSANTS SEMI-CONDUCTEURS

XII) Circuits digitaux en CMOS

P.A. Besse

EPFL

Chapitre 12: «Circuits digitaux en CMOS »

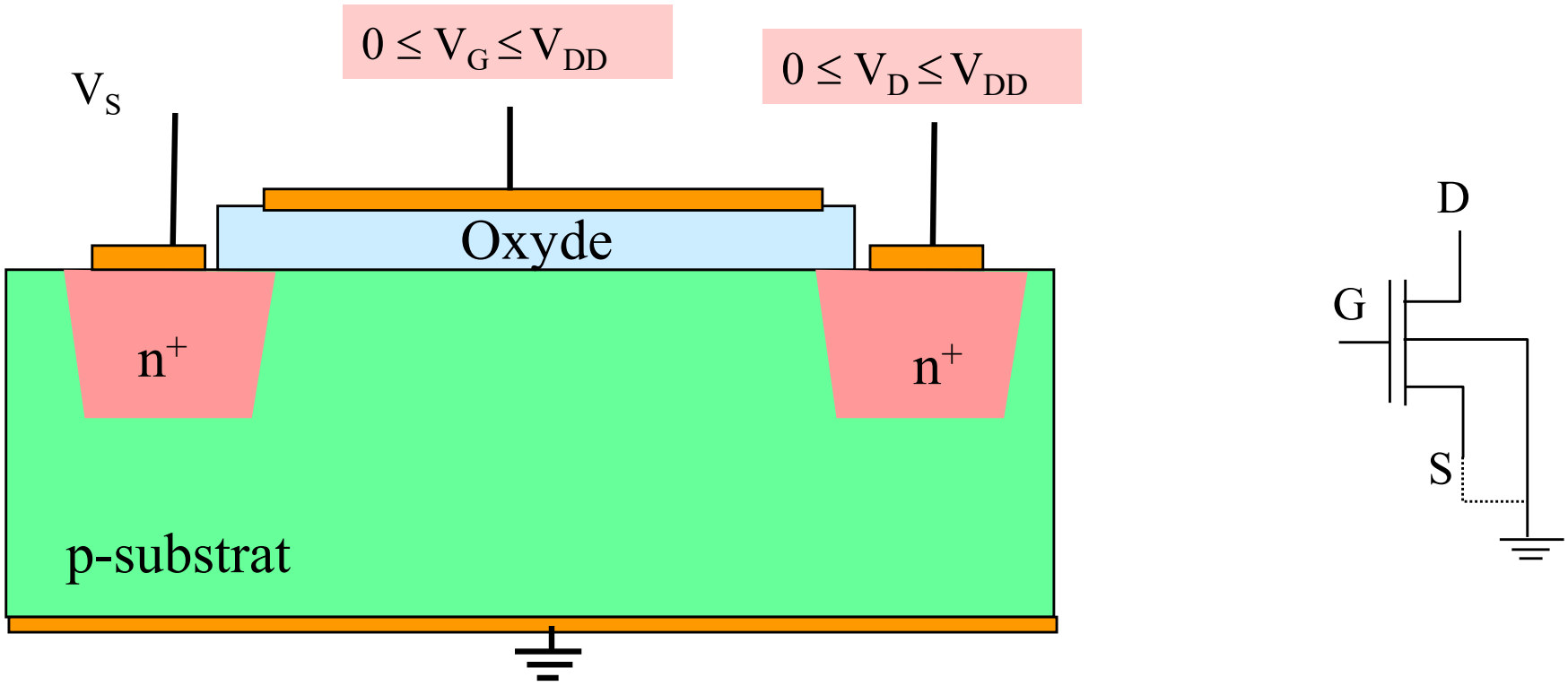
- Principe de design des circuits CMOS

- Inverseur CMOS

- Portes logiques 2x1 et logique CMOS à plusieurs entrées

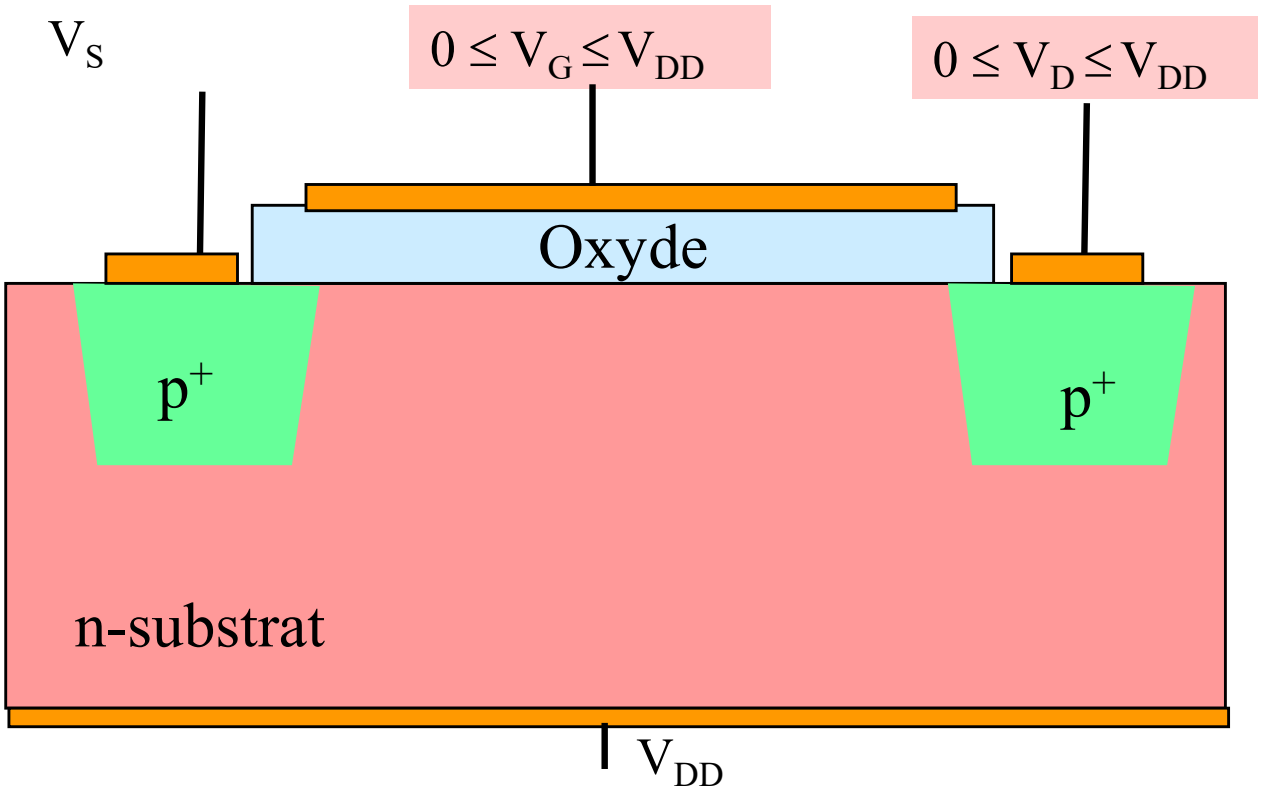
- Ring oscillator et SRAM

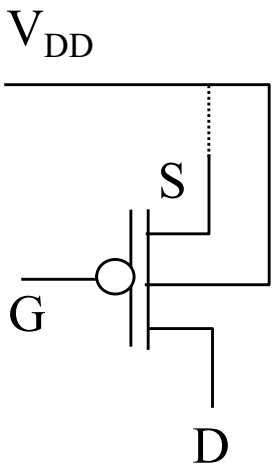
Structure NMOS



- Substrat p (ou p-tub) au potentiel le plus bas.
- Gate et drain variables entre 0 et V_{DD}.
- La source est à un potentiel inférieur au drain.

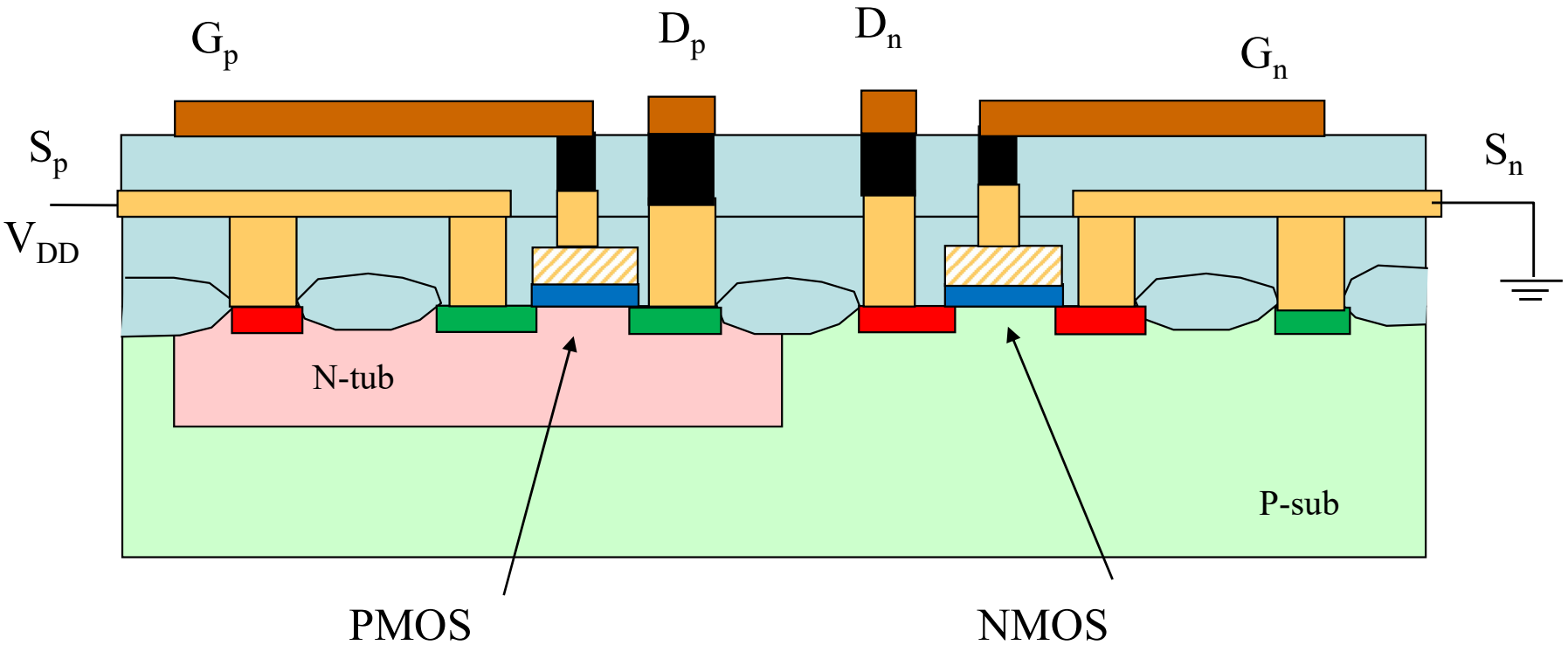
Structure PMOS





- Substrat n (ou n-tub) au potentiel le plus haut (V_{DD}).
- Gate et drain variables entre 0 et V_{DD}.
- La source est à un potentiel supérieur au drain.

Structure CMOS

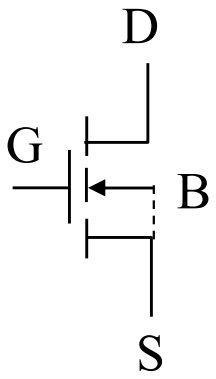


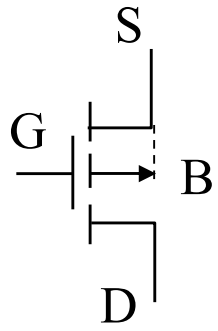
CMOS: symboles

NMOS

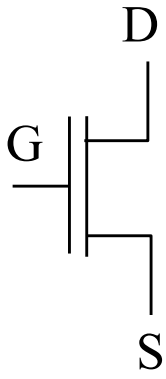
PMOS

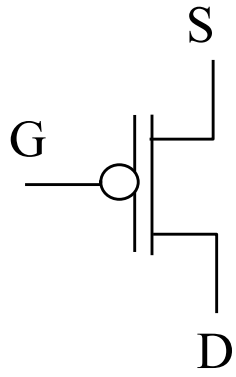
analogique



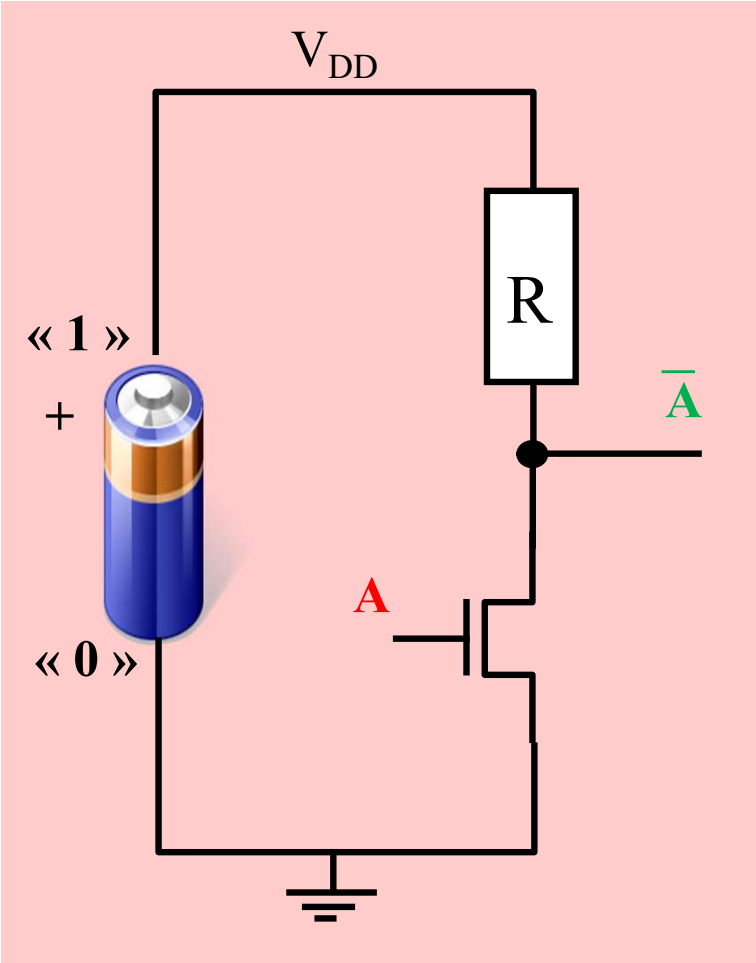


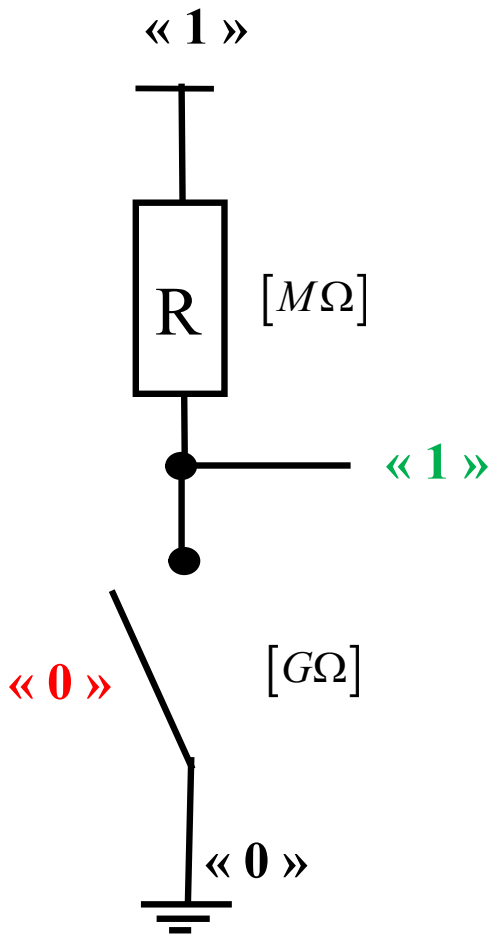
digital

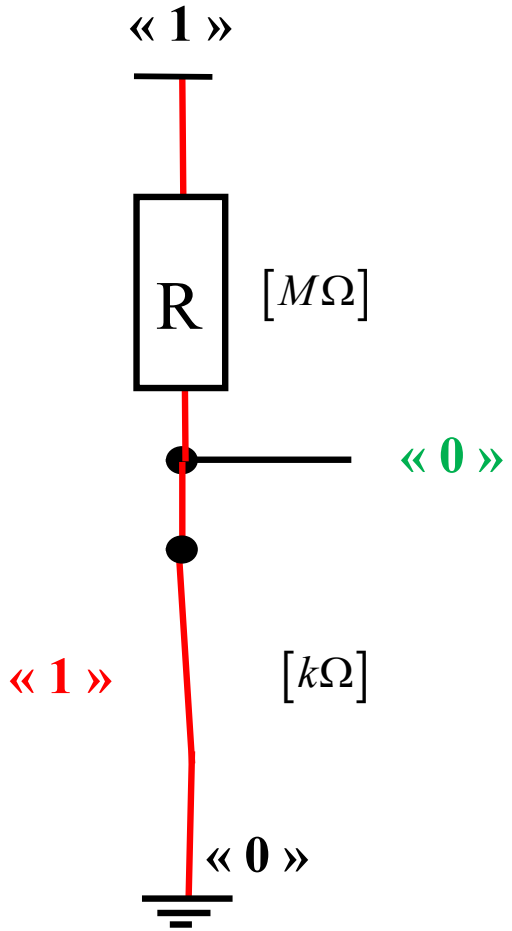




Inverseur NMOS







Consommation

Problème 1

Problème 1: «NMOS logic»

Etudiez ce schéma en logique NMOS
Quelle condition doit-on poser sur la valeur de R ?

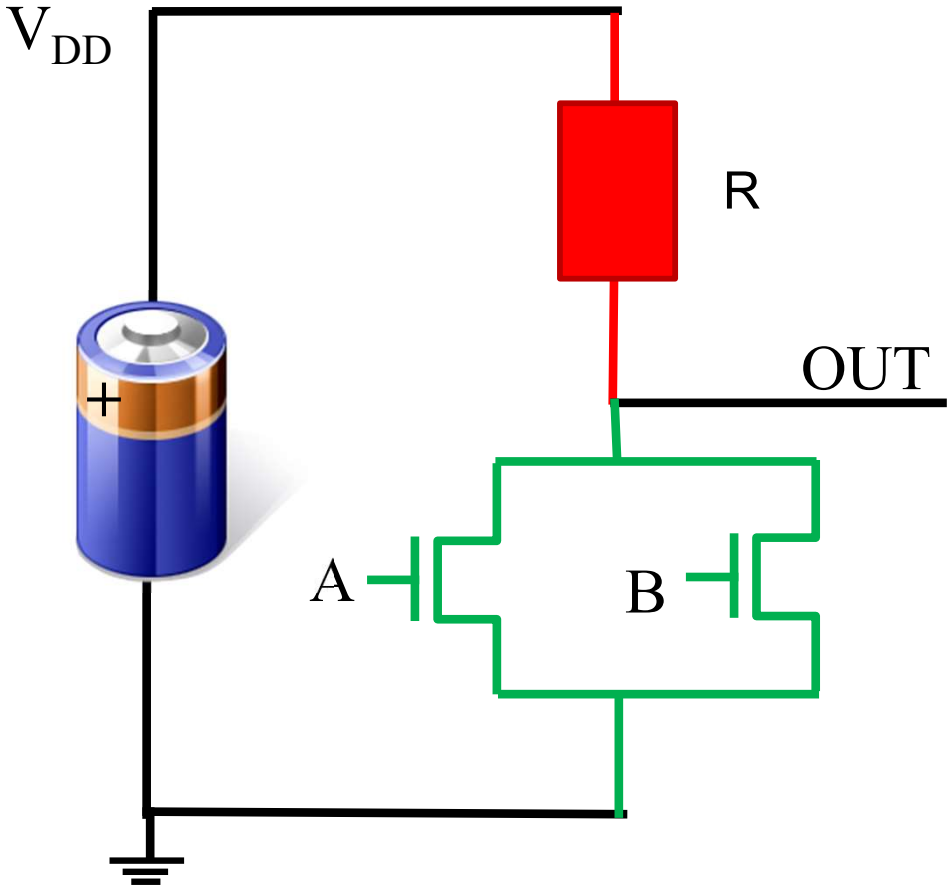


Table de vérité

A	B	Out
0	0	
0	1	
1	0	
1	1	

Réponse 1

Etudiez cet schéma

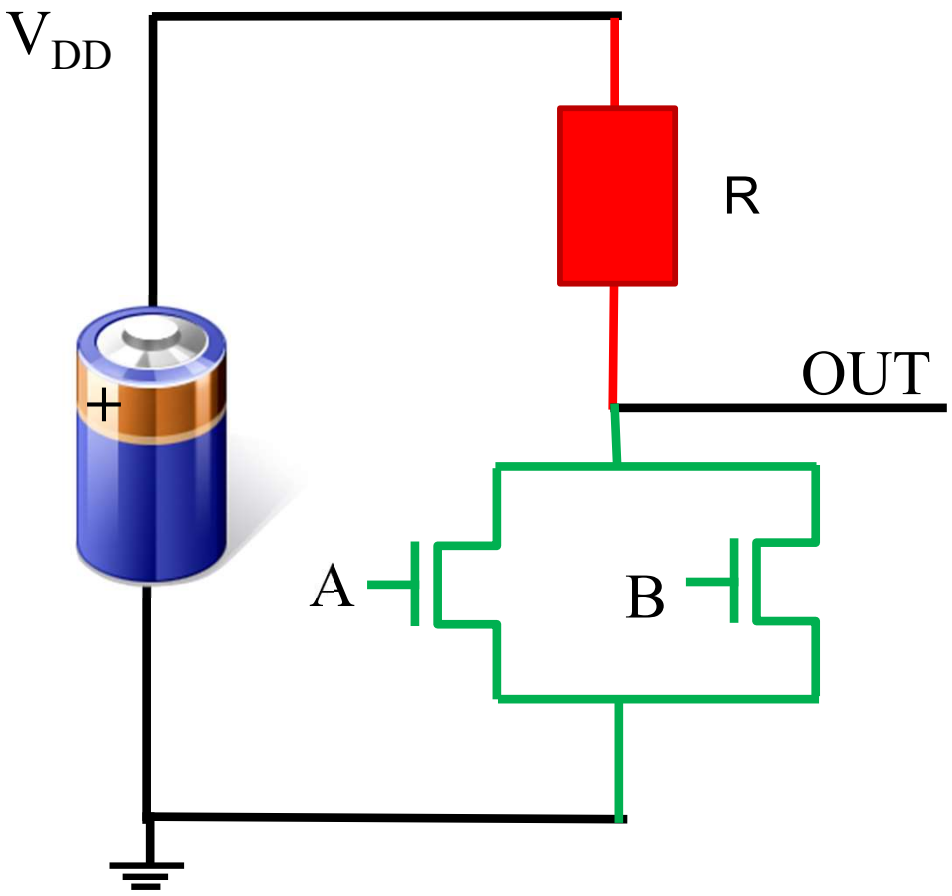


Table de vérité

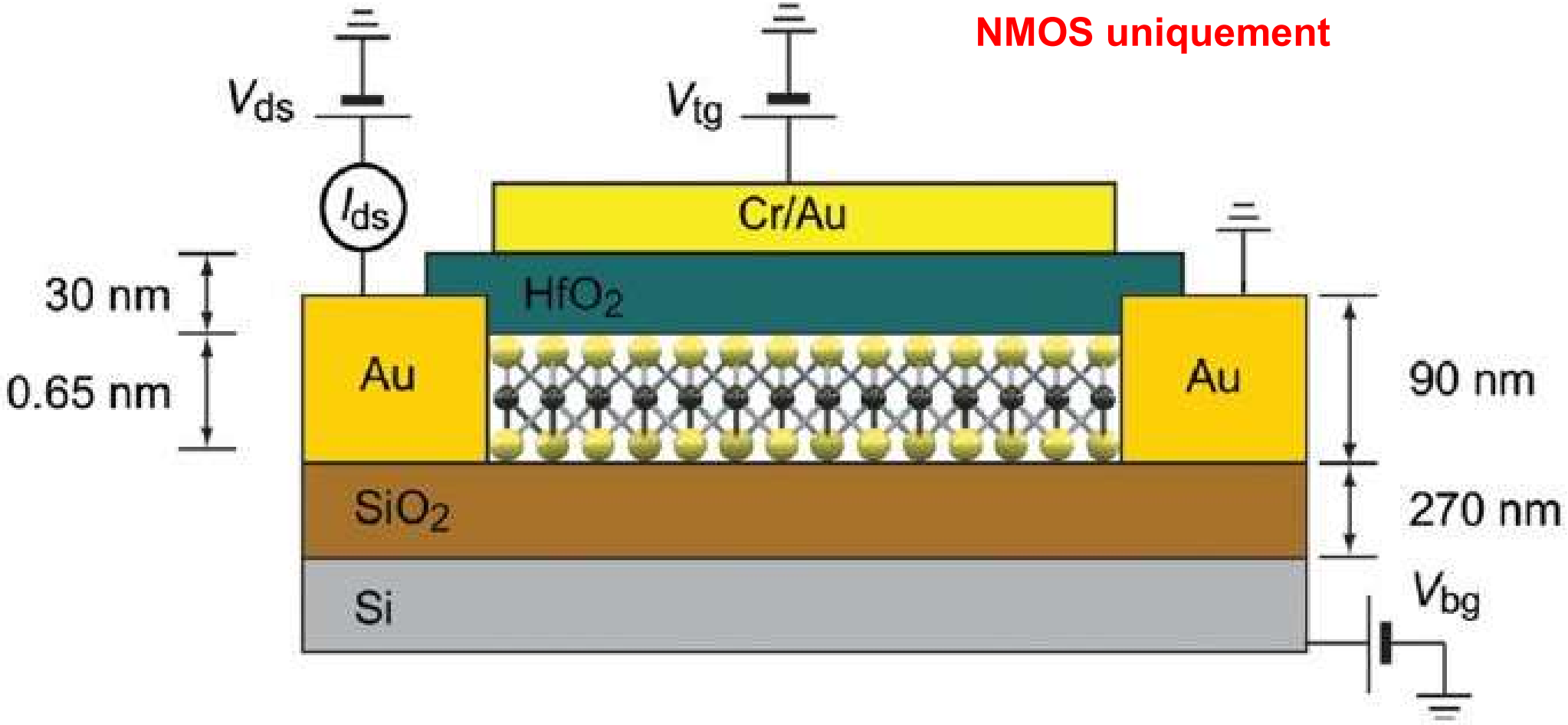
NOR gate

A	B	Out	
0	0	**1**	
0	1	**0+**	⇦
1	0	**0+**	⇦
1	1	**0**	⇦

Courant assez élevé

Puce électronique en Mobyldénite (A. Kis, LANES, EPFL)

Structure de base
NMOS uniquement

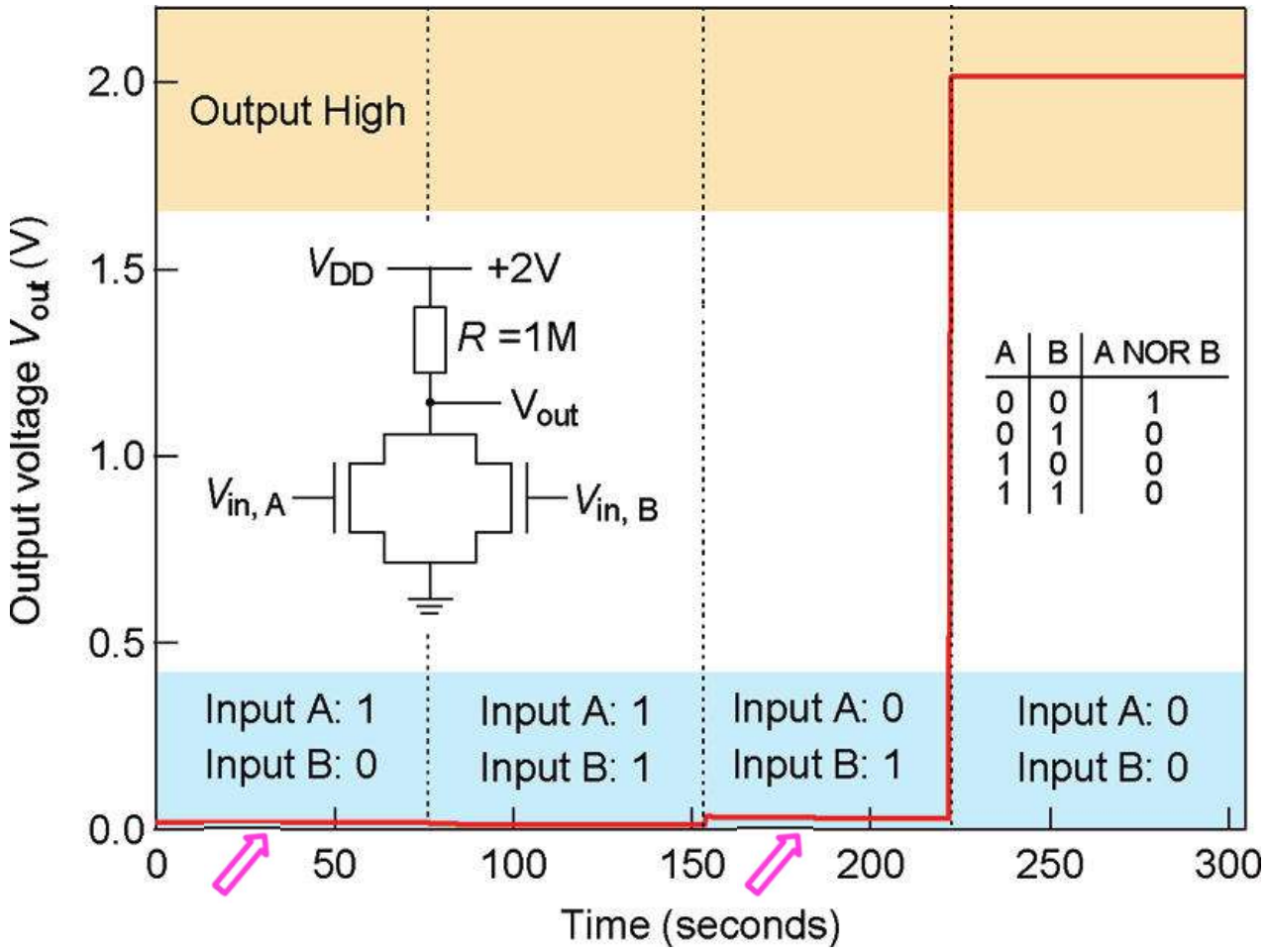


B. Radisavljevic et al. "Small-signal amplifier based on single-layer MoS2", Appl. Phys. Lett. 101, (2012)

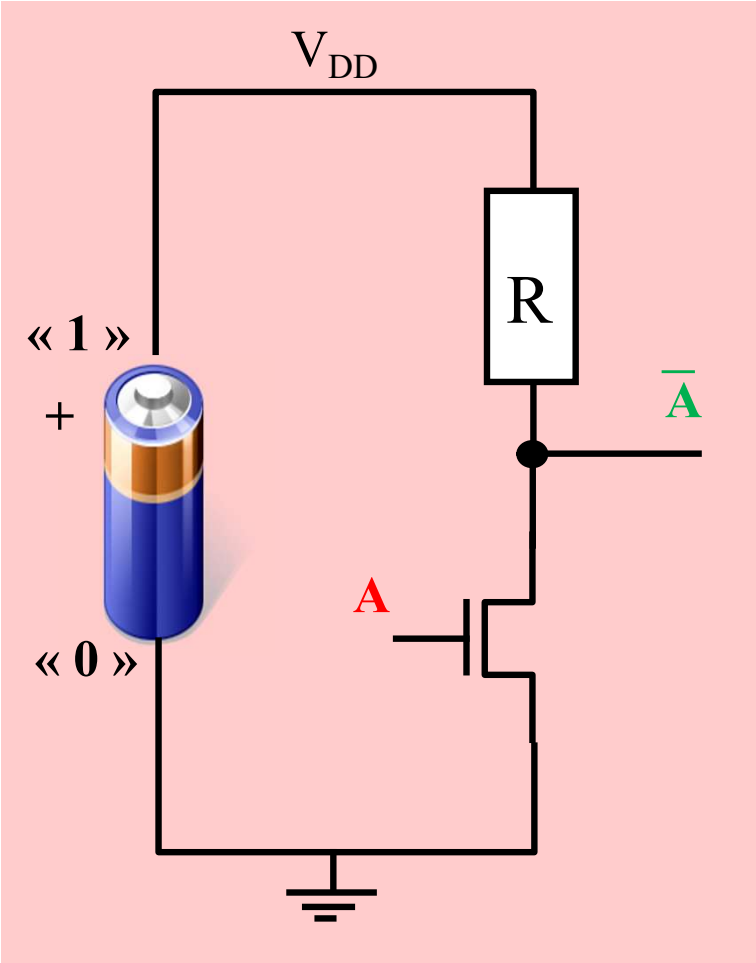
Puce électronique en Mobyldénite (A. Kis, LANES, EPFL, Déc. 2011)

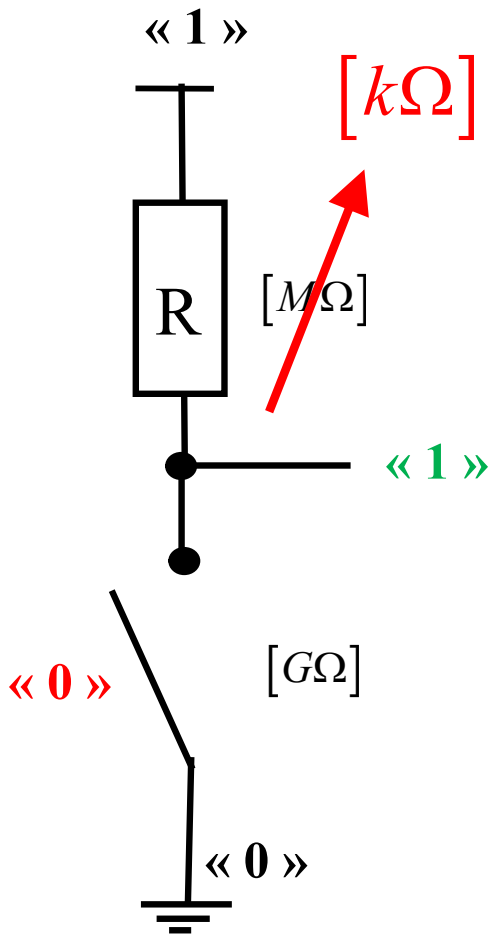
B. Radisavljevic et al., « Integrated Circuits and Logic Operations Based on Single-Layer MoS_2 » *ACS Nano*, 2011, 5 (12), pp 9934–9938

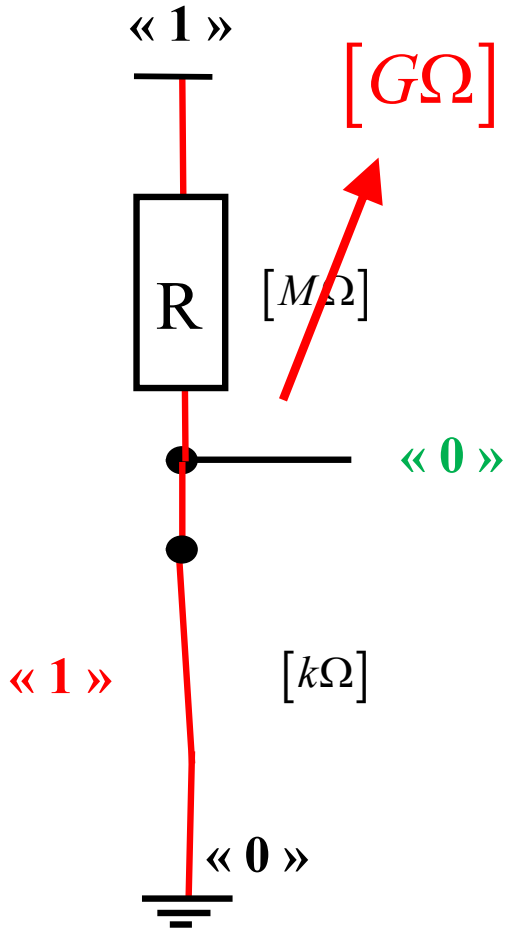
NOR gate avec uniquement des NMOS



Inverseur NMOS





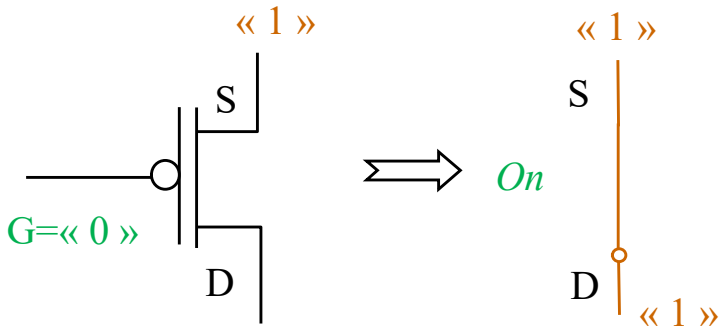


Circuits digitaux: interrupteur CMOS

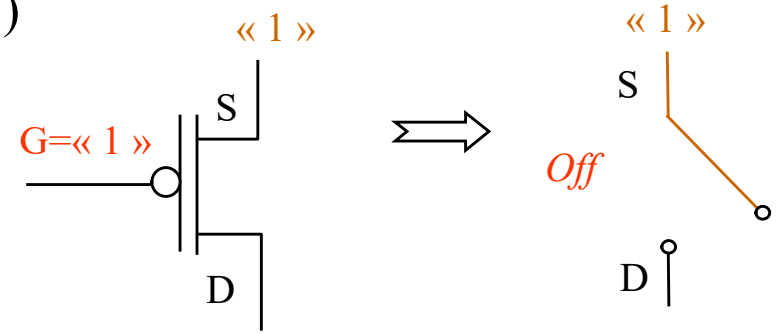
“0” sur les gates **“1” sur les gates**

PMOS

P0)

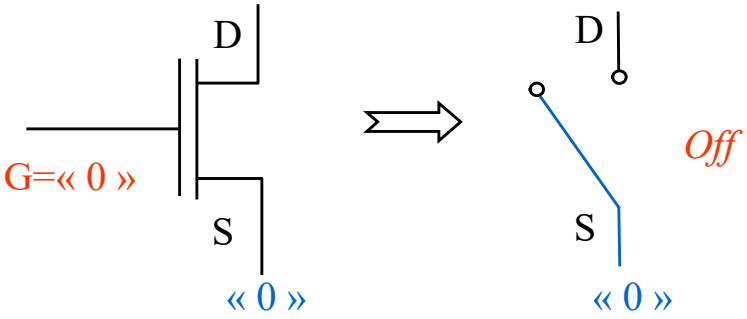


P1)

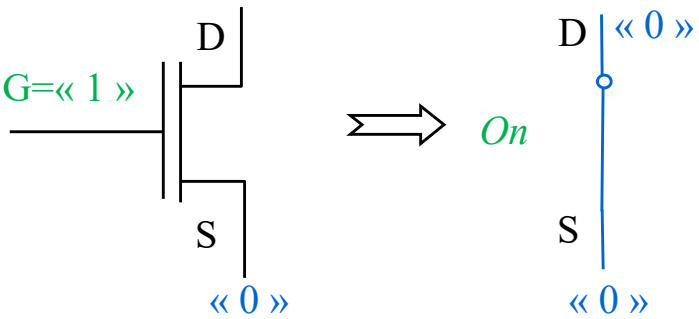


NMOS

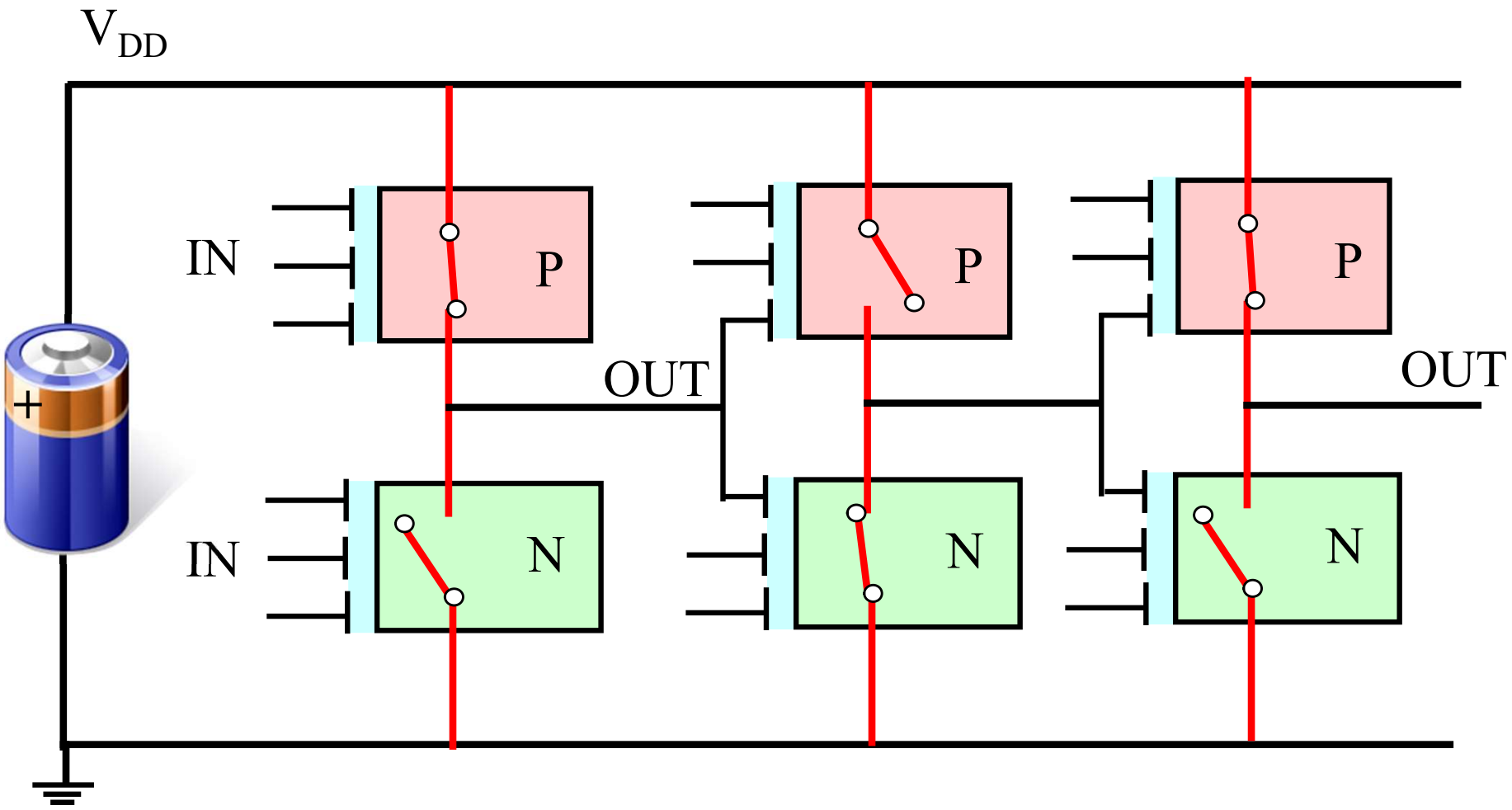
N0)



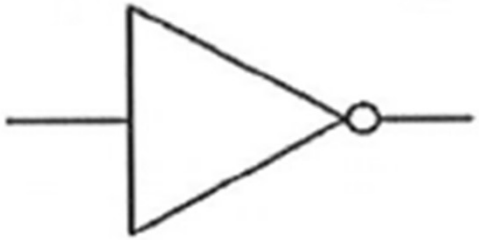
N1)



La complémentarité



Inverter (NOT gate)



Traditional symbol

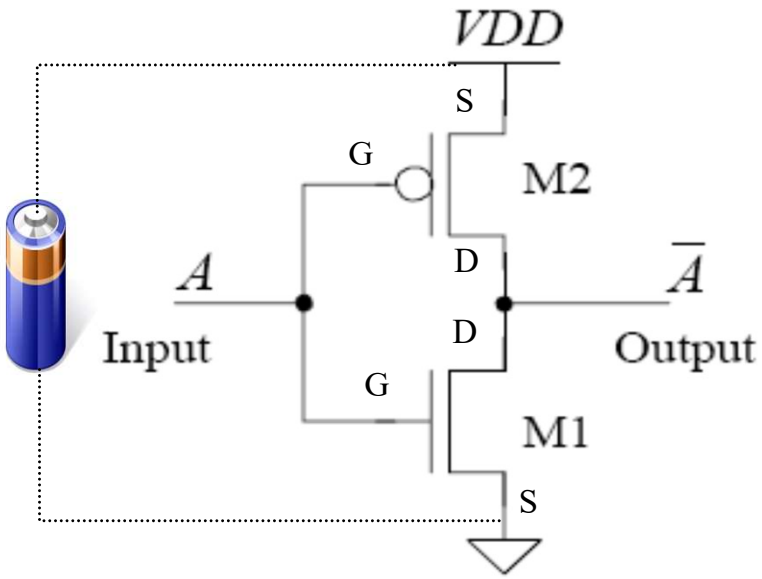
Input A	Output Q
0	1
1	0

Truth Table

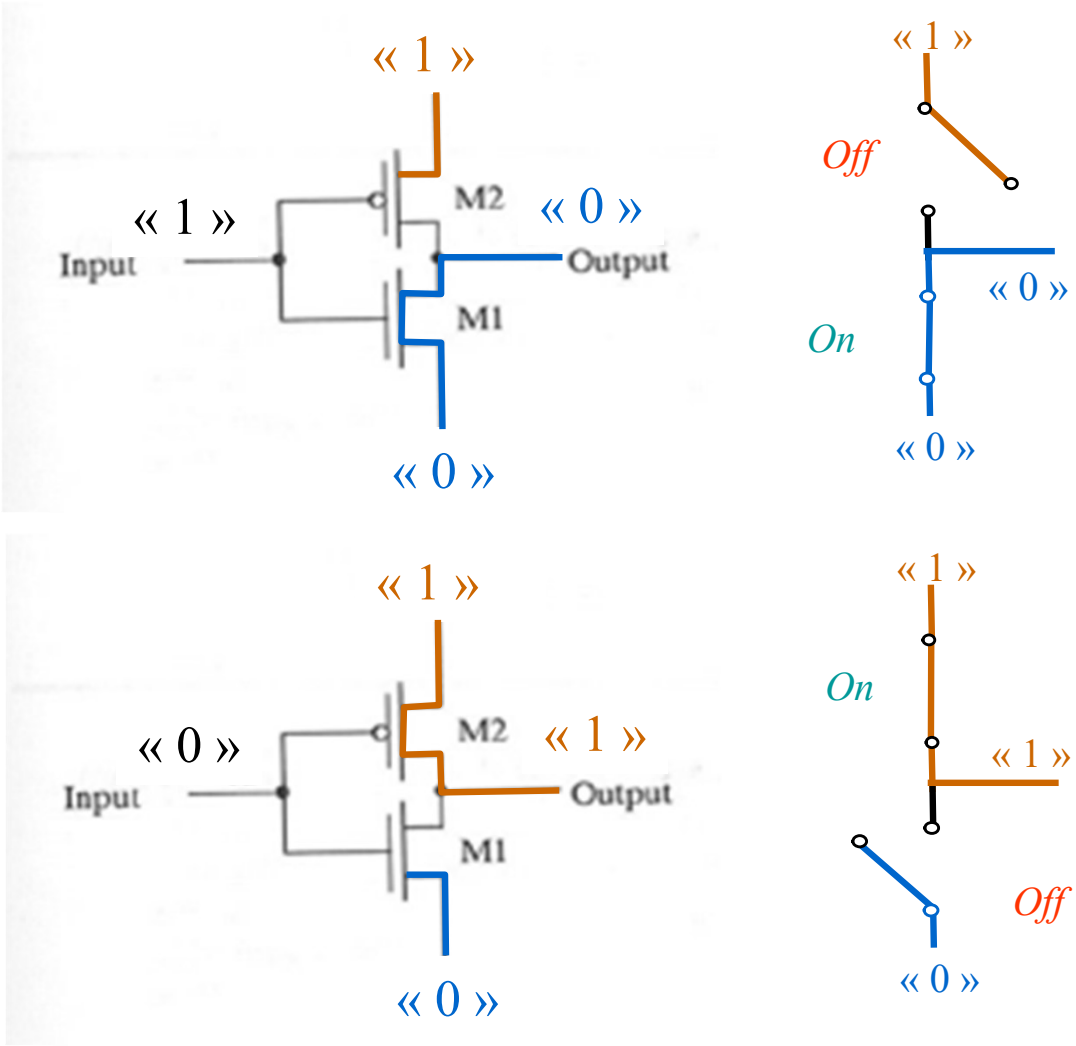
http://www.kpsec.freeuk.com/gates.htm

Inverter CMOS (1)

2 transistors

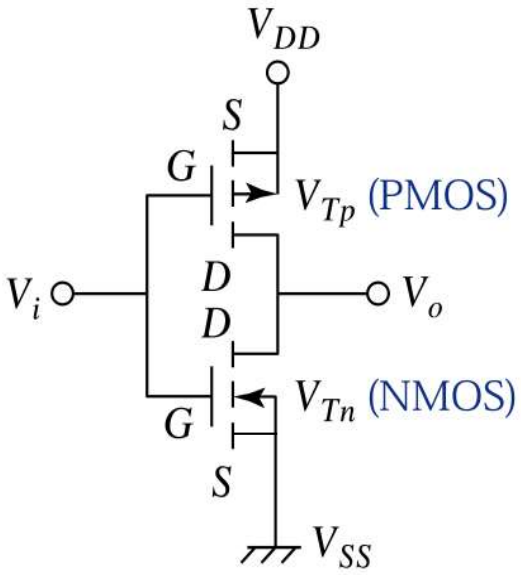


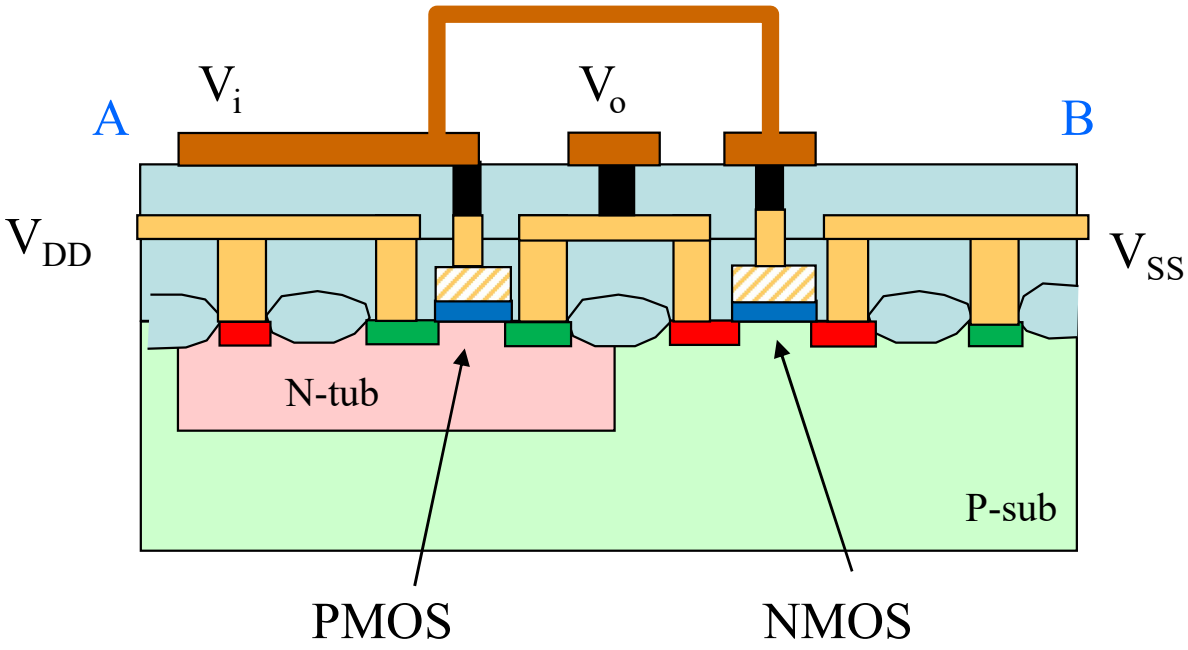
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press



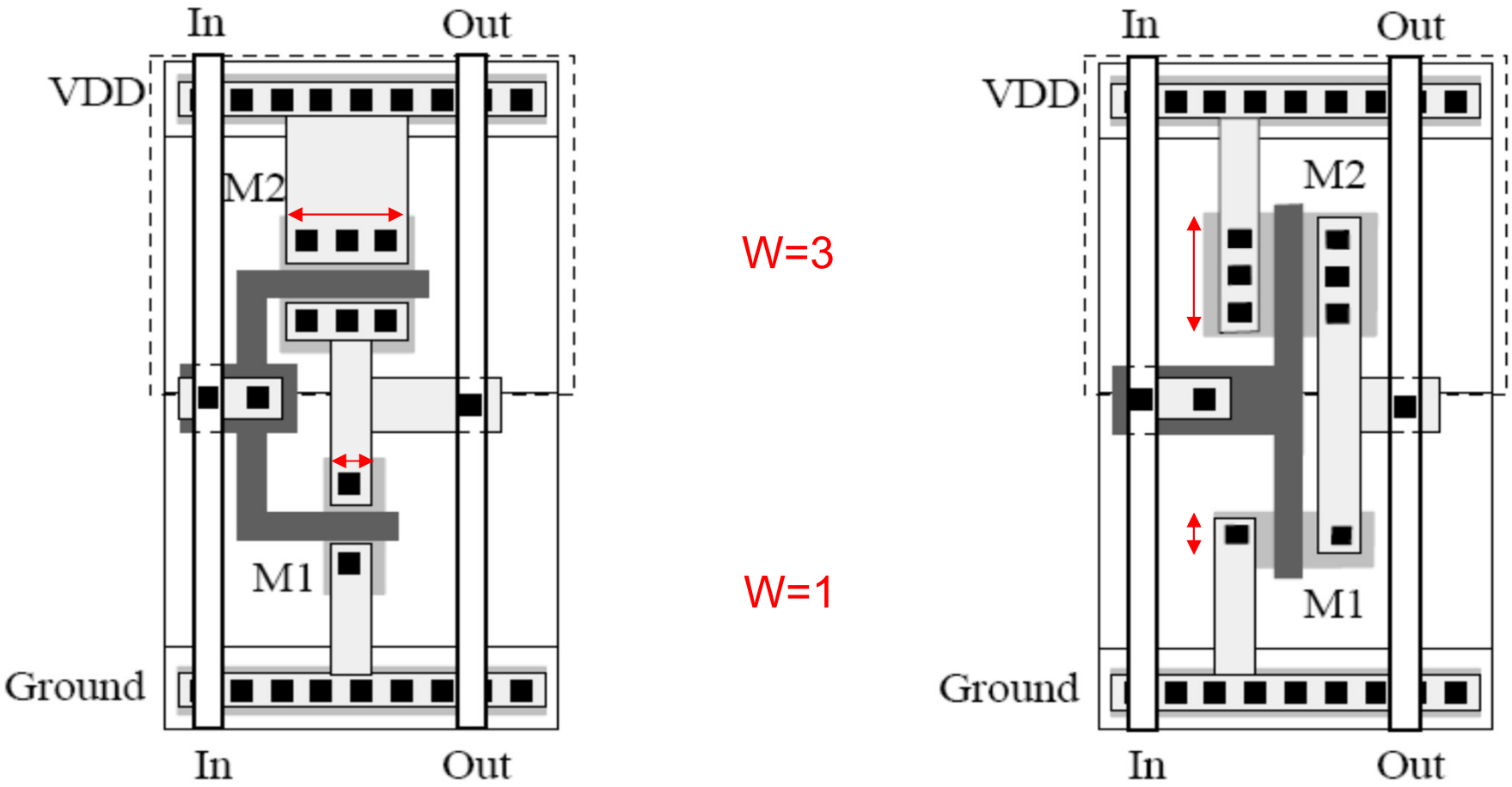
Inverter CMOS (2)

Semiconductor Devices, 2/E by S. M. Sze





Inverter CMOS (3)

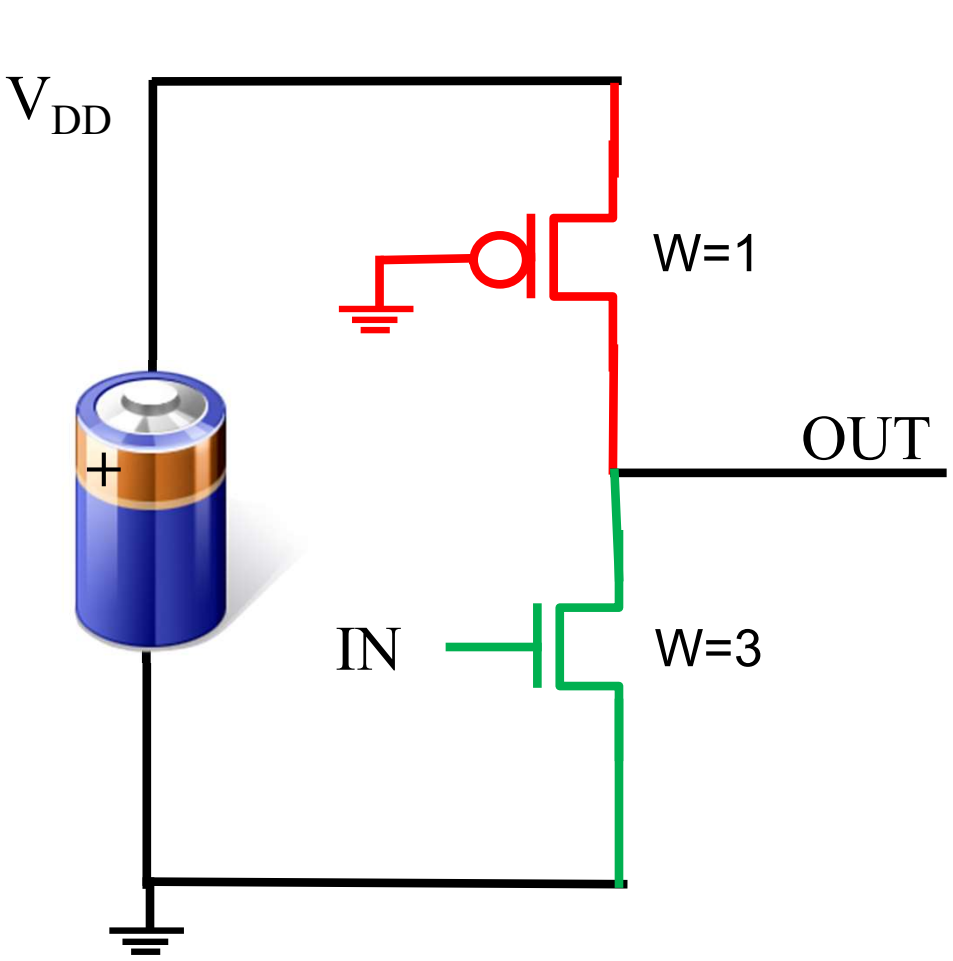


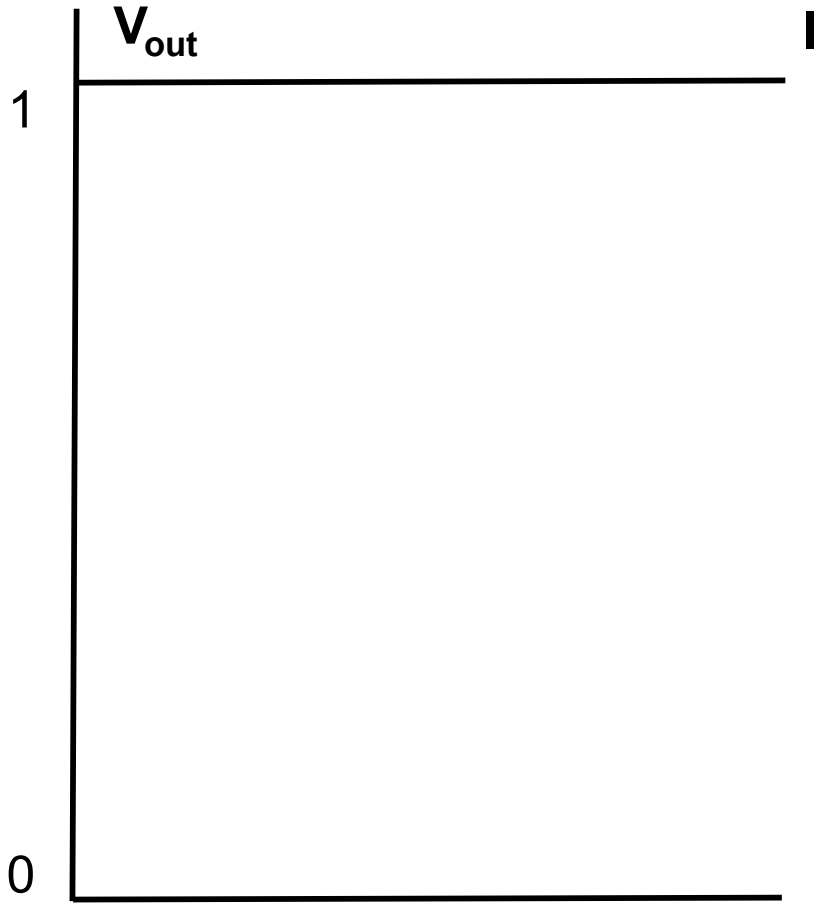
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

Problème 2

Problème 2: «Pseudo-NMOS logic»

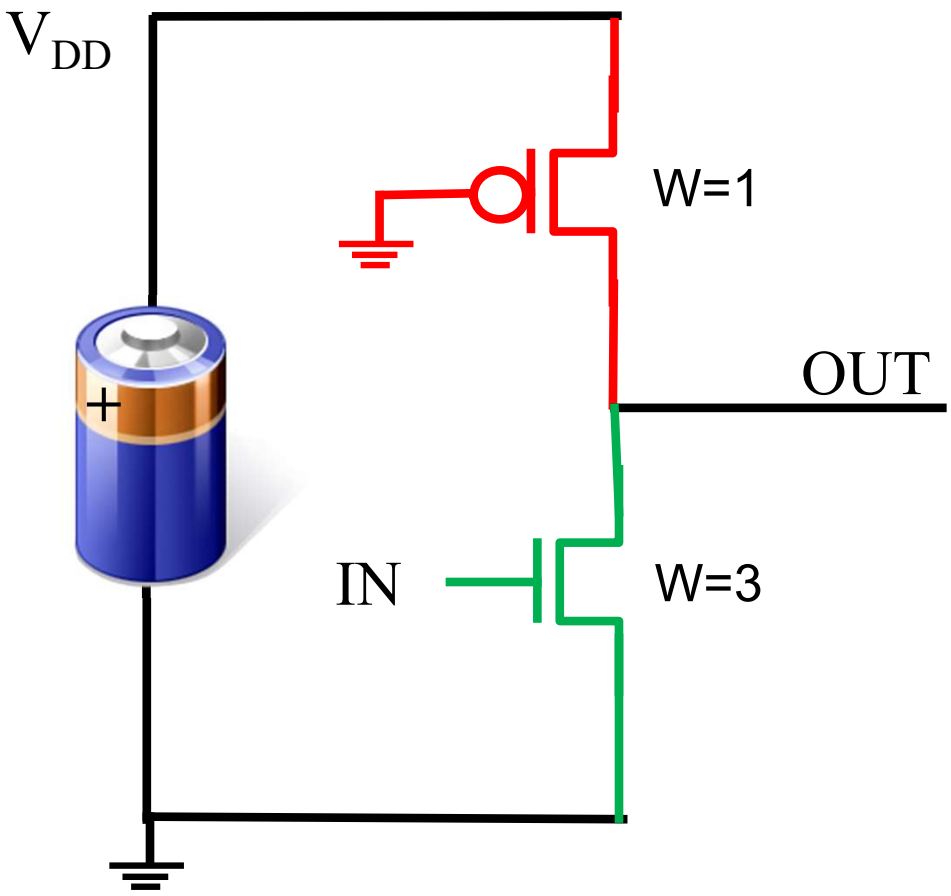
Etudiez cet schéma, quels avantages/désavantages comparé à un CMOS ?

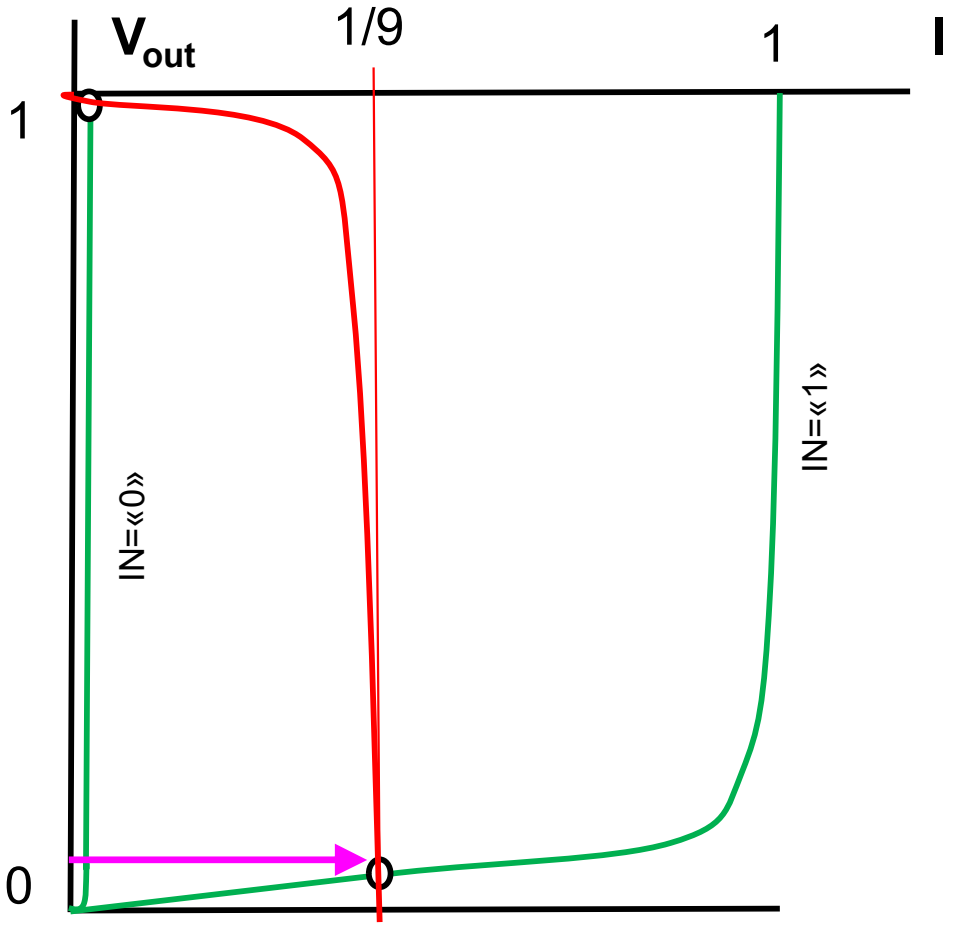




Réponse 2

Etudiez cet schéma, quel désavantage comparé à un CMOS ?

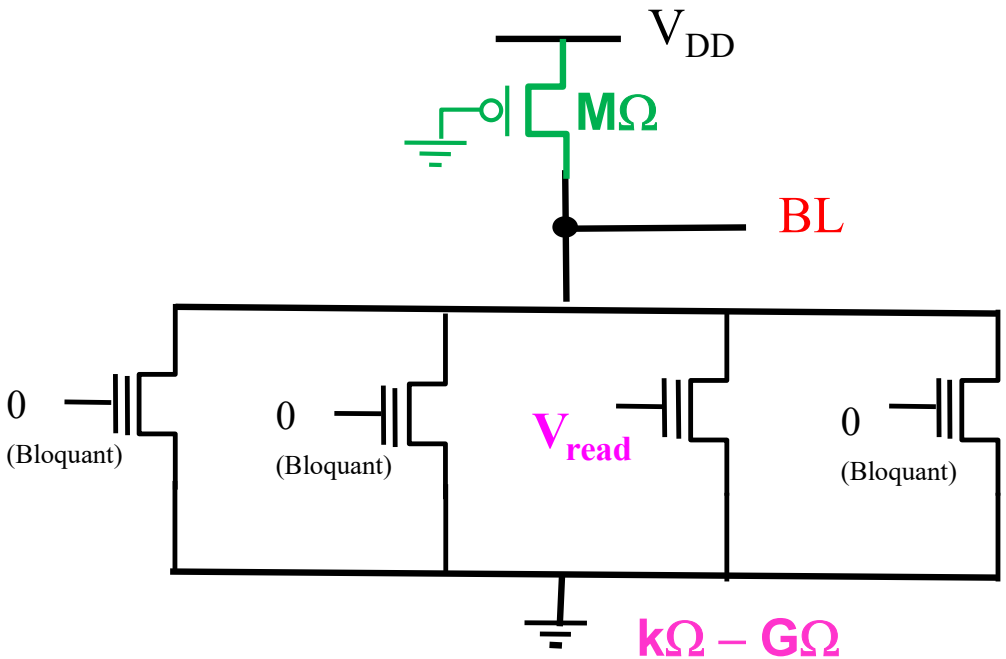




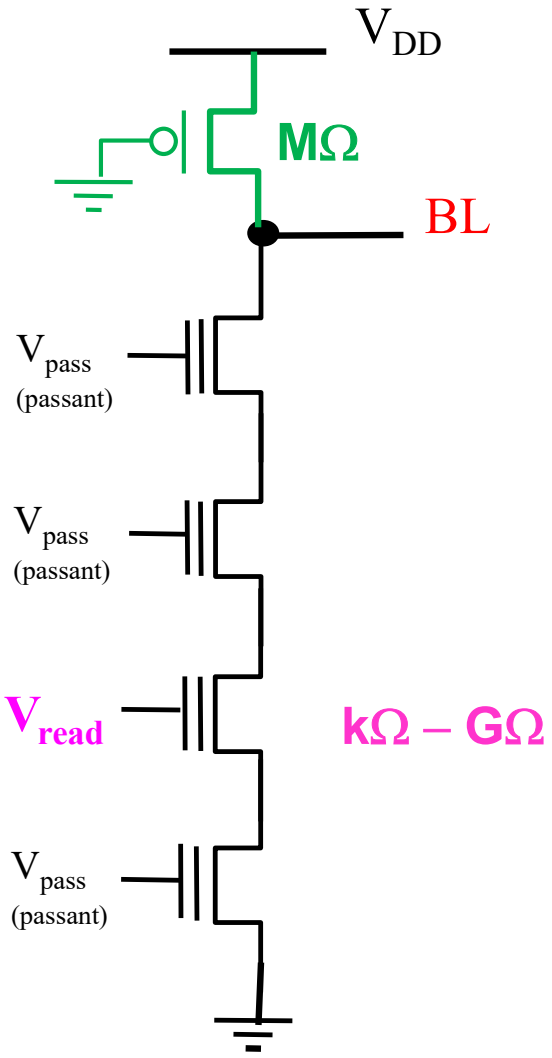
Courant assez élevé

Mémoires floating gate

«NOR»: NMOS en parallèle

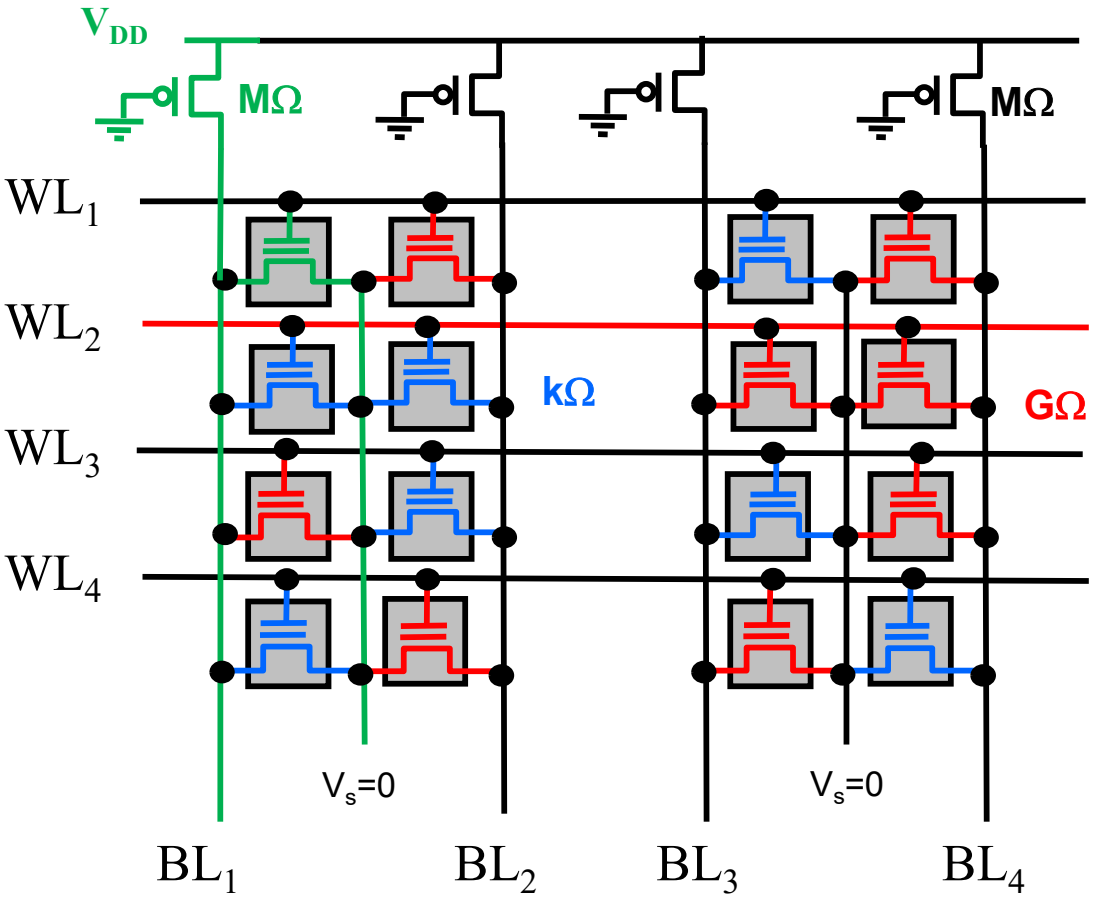


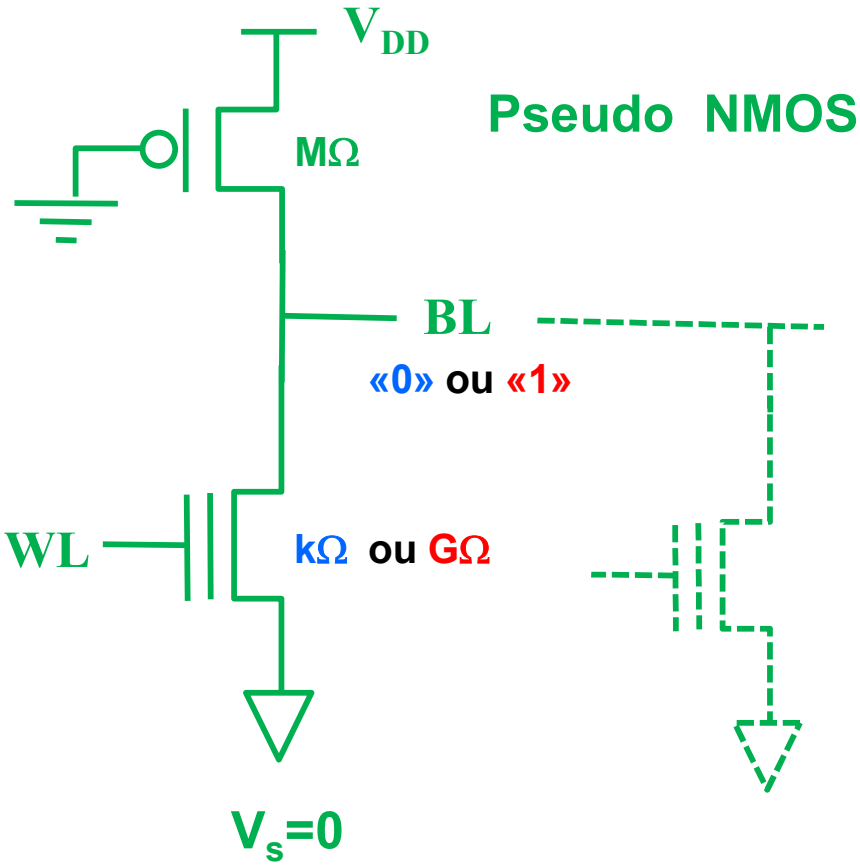
«NAND»: NMOS en série



Mémoires floating gate: Pseudo NMOS

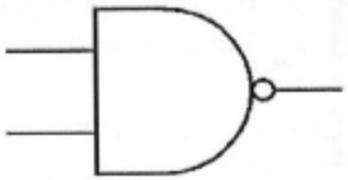
Configuration «NOR»





Logique (1)

NAND



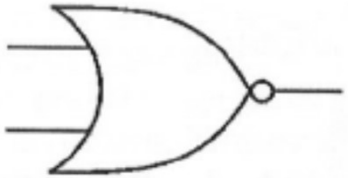
Traditional symbol

Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

http://www.kpsec.freeuk.com/gates.htm

NOR



Traditional symbol

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

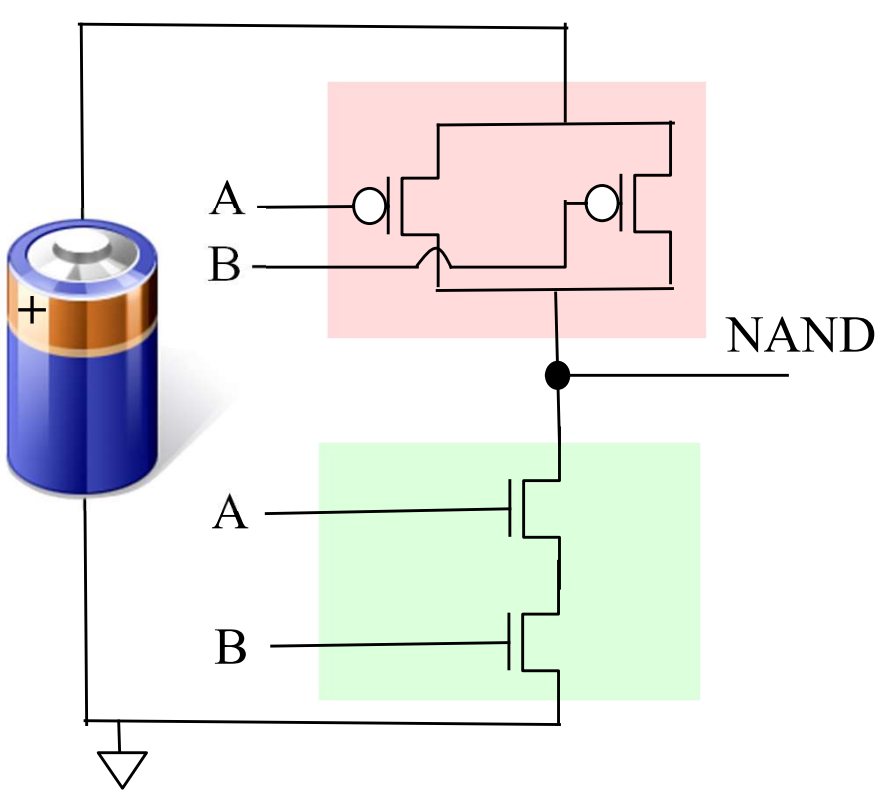
Truth Table

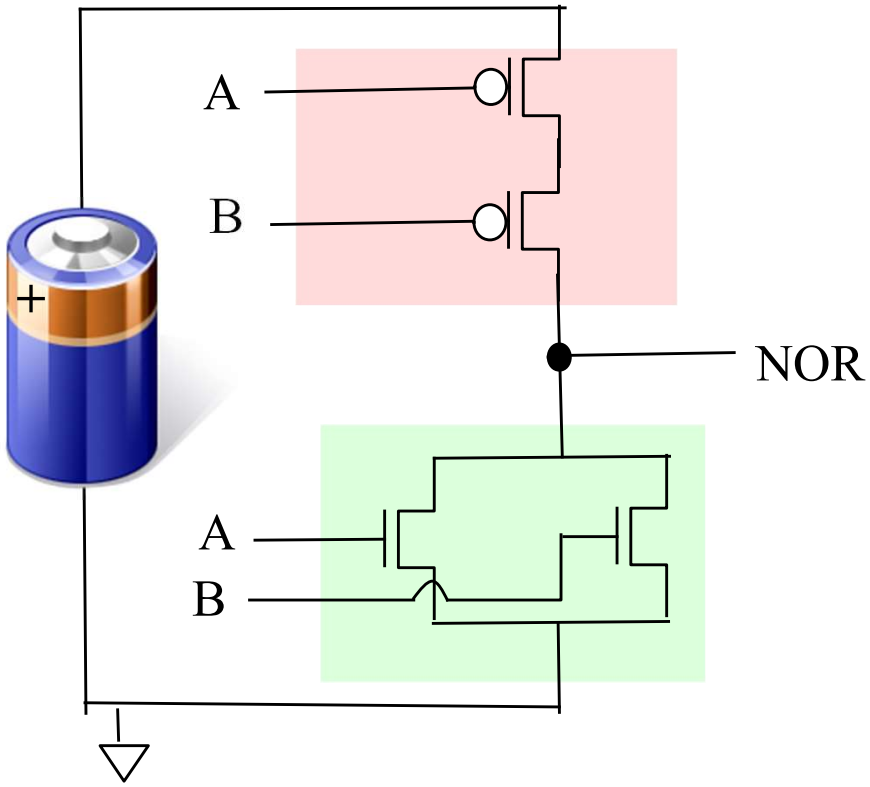
NAND et NOR en CMOS

NAND

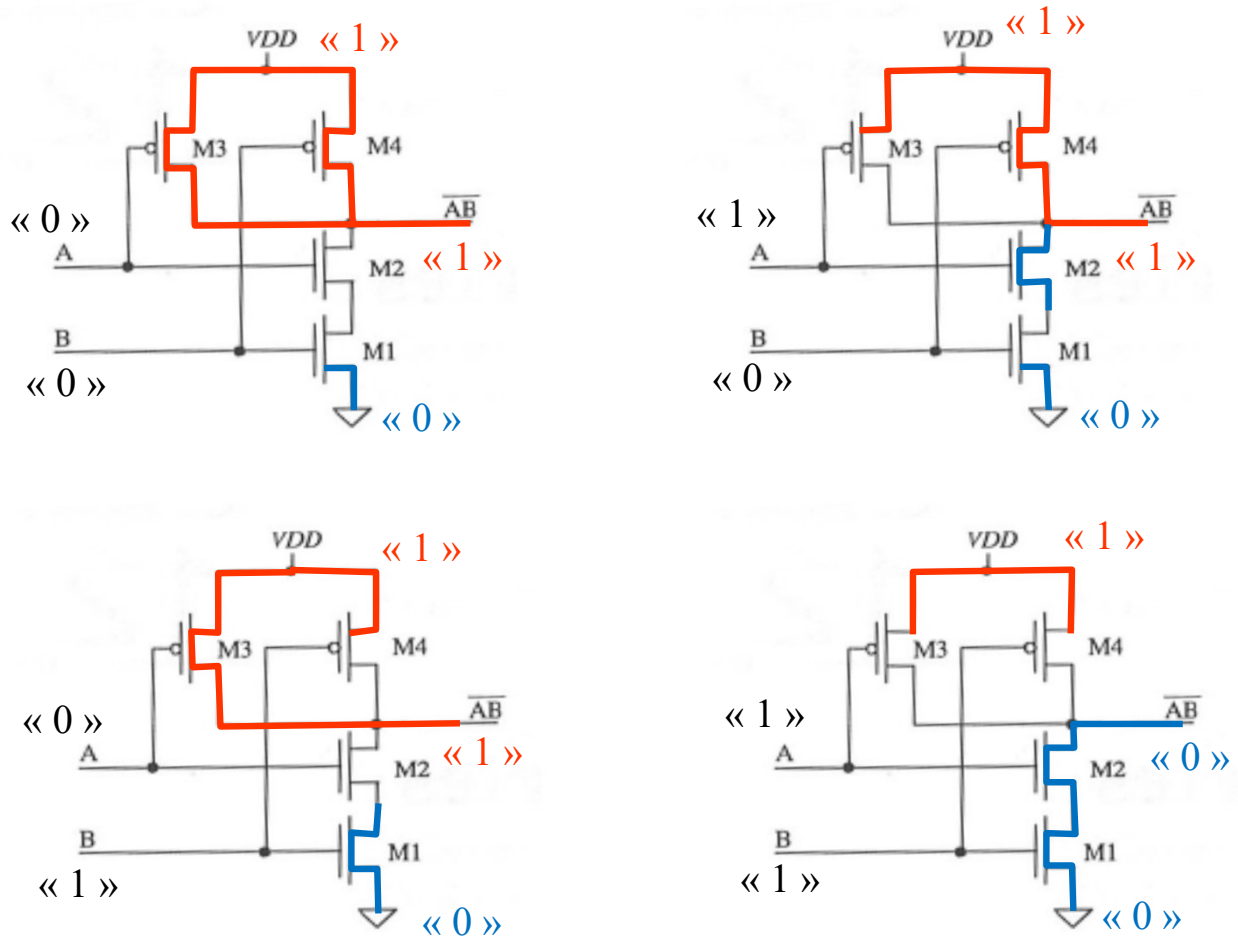
4 transistors

NOR





NAND

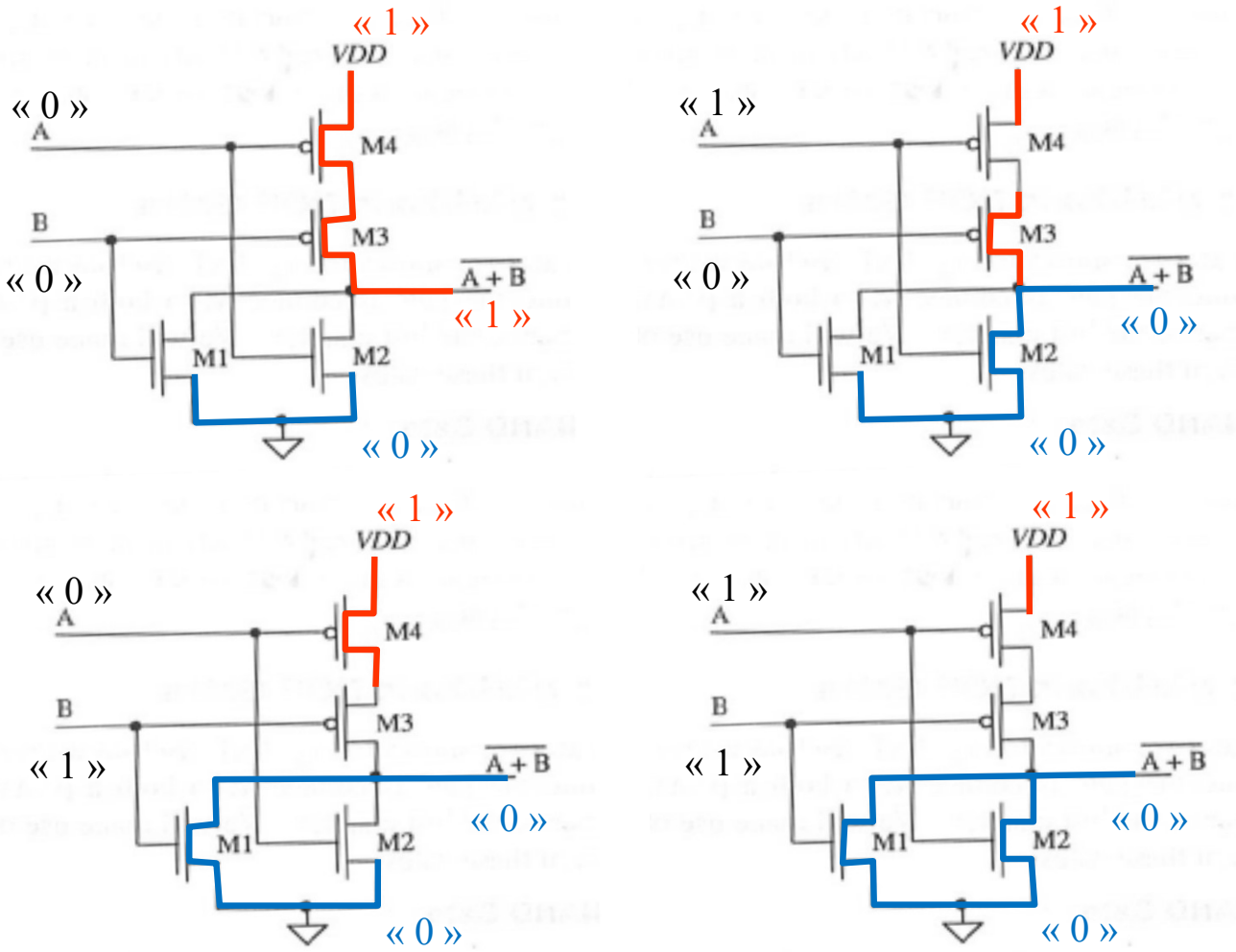


Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

NOR



Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

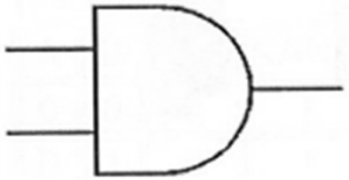
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

Problème 3

Problème (3): « AND et OR »

Utilisez la structure de base d'un circuit CMOS pour construire un «AND» ou un «OR»

AND



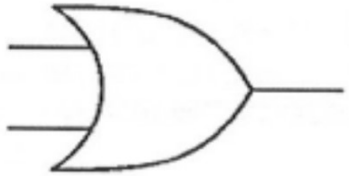
Traditional symbol

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table

http://www.kpsec.freeuk.com/gates.htm

OR



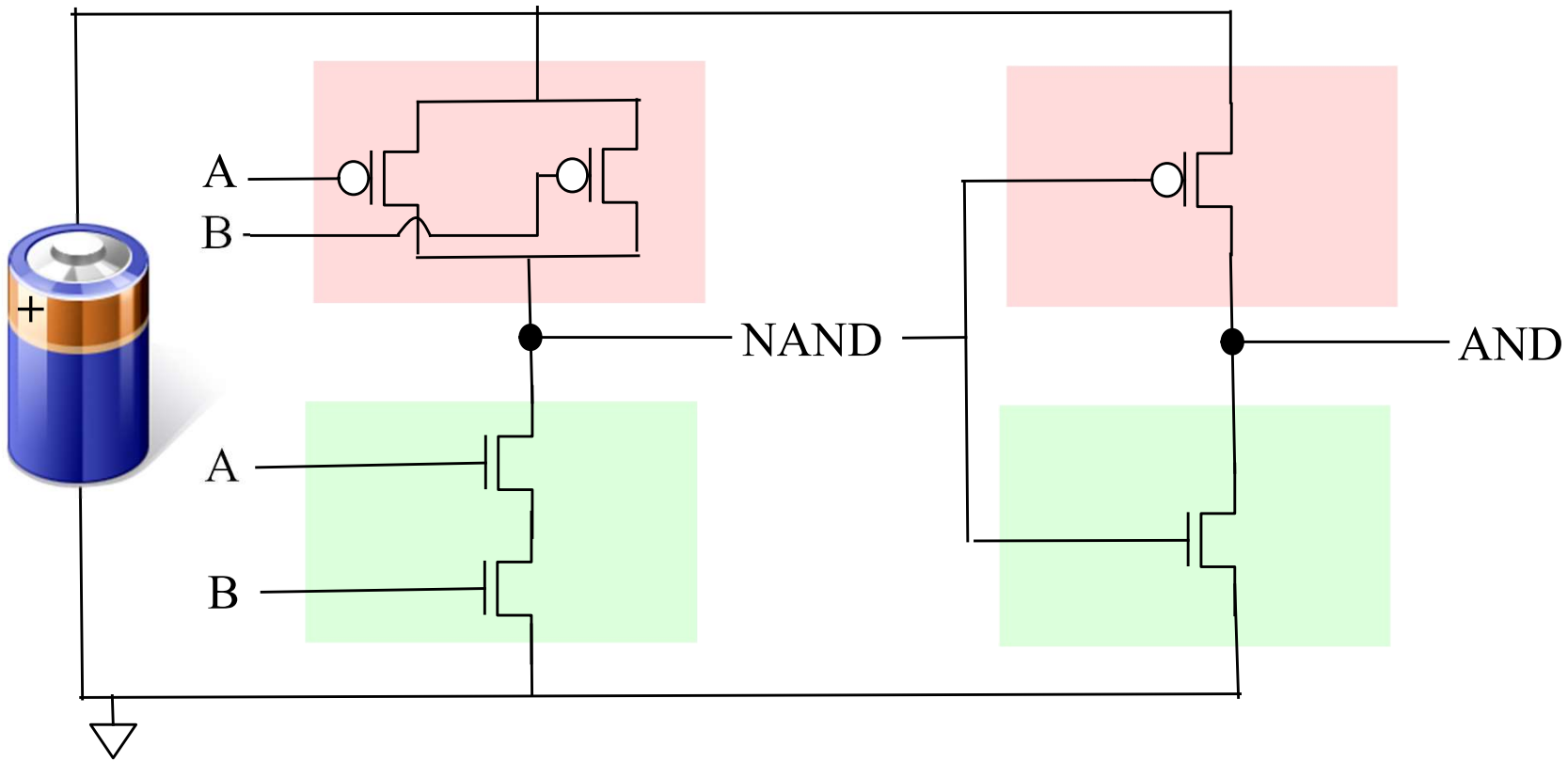
Traditional symbol

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table

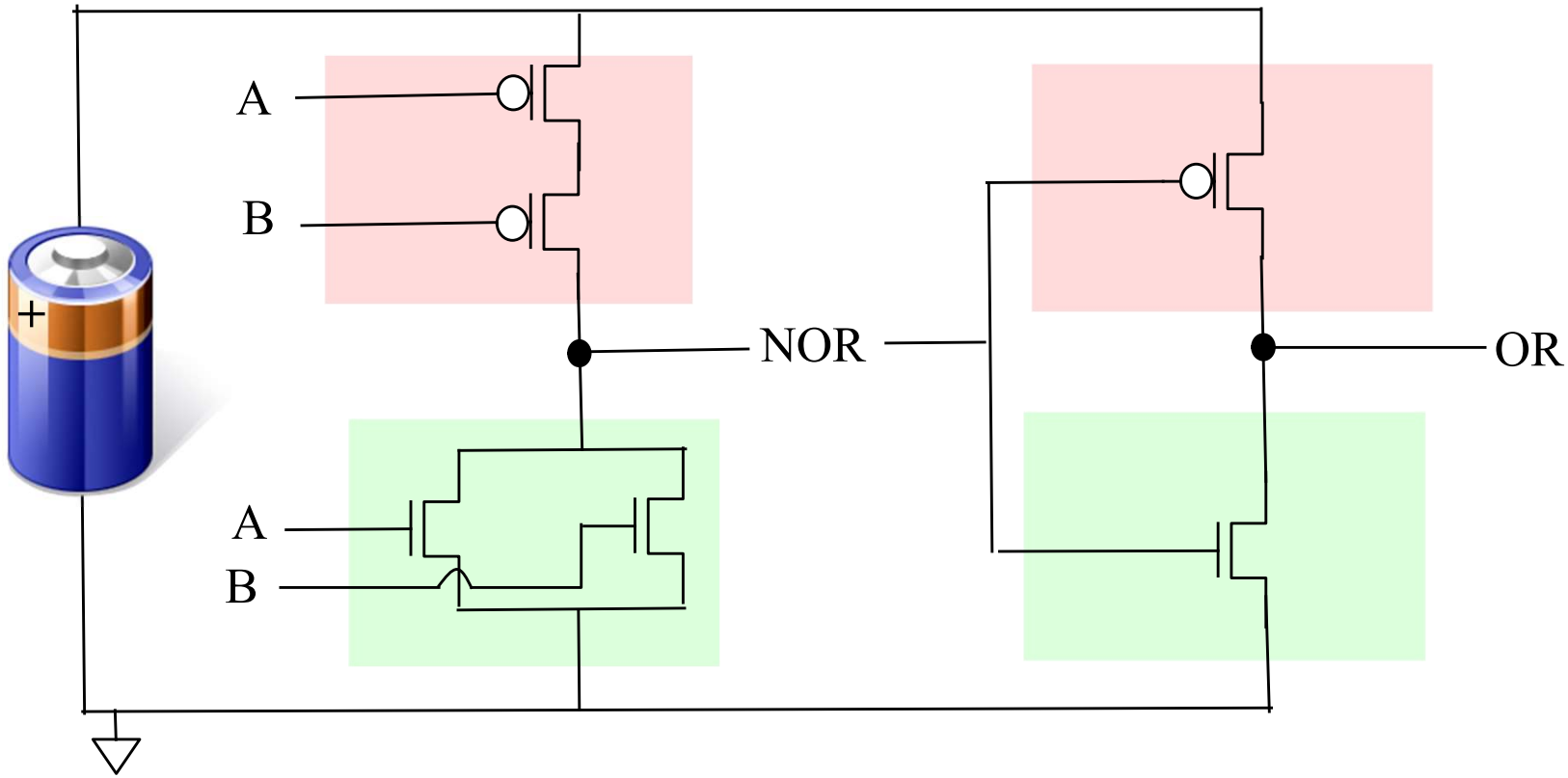
AND en CMOS

AND 6 transistors

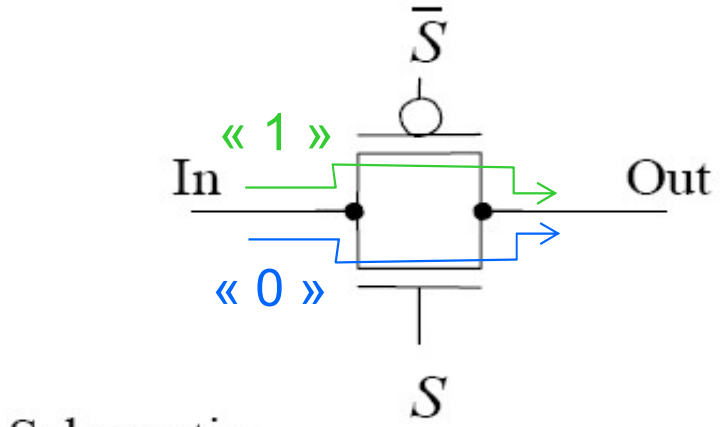


OR en CMOS

OR 6 transistors



Transmission gate



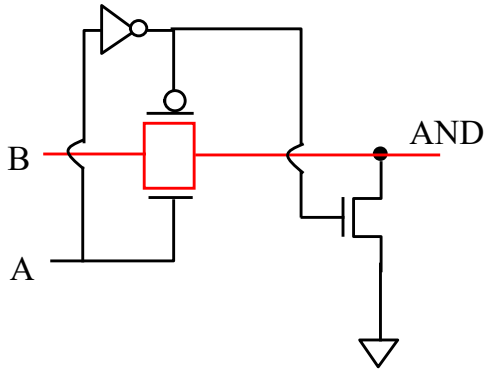
Schematic

	S	IN	OUT
Bloqué	0	0	OFF
	0	1	OFF
Transmis	1	0	0
	1	1	1

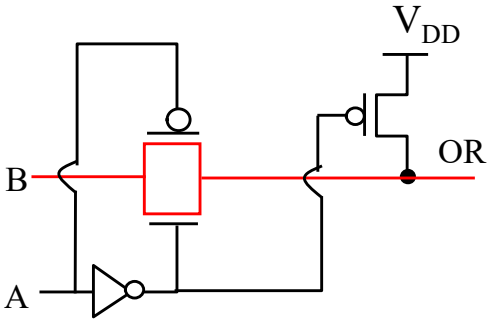
Sans le PMOS, un “1” à l’entrée ne serait pas transmis correctement.

- Le NMOS transmet les “0”.
- Le PMOS transmet les “1”.

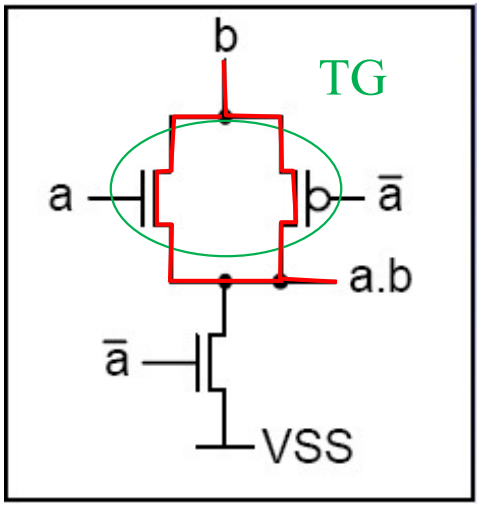
AND et OR en CMOS et Transmission Gate



5 transistors



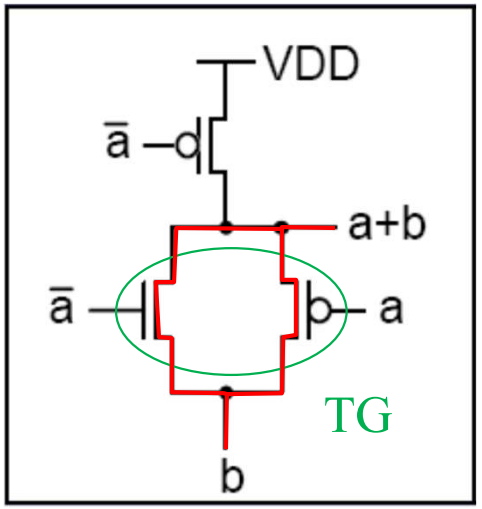
AND



Mais:
Pas d'isolation
→ Transmission du bruit

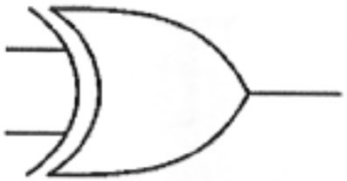
A. Stauffer, cours EPFL.

OR



Logique (3)

XOR



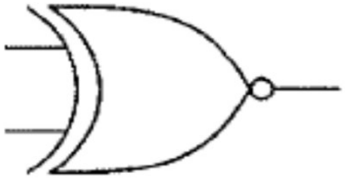
Traditional symbol

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table

http://www.kpsec.freeuk.com/gates.htm

XNOR



Traditional symbol

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	1

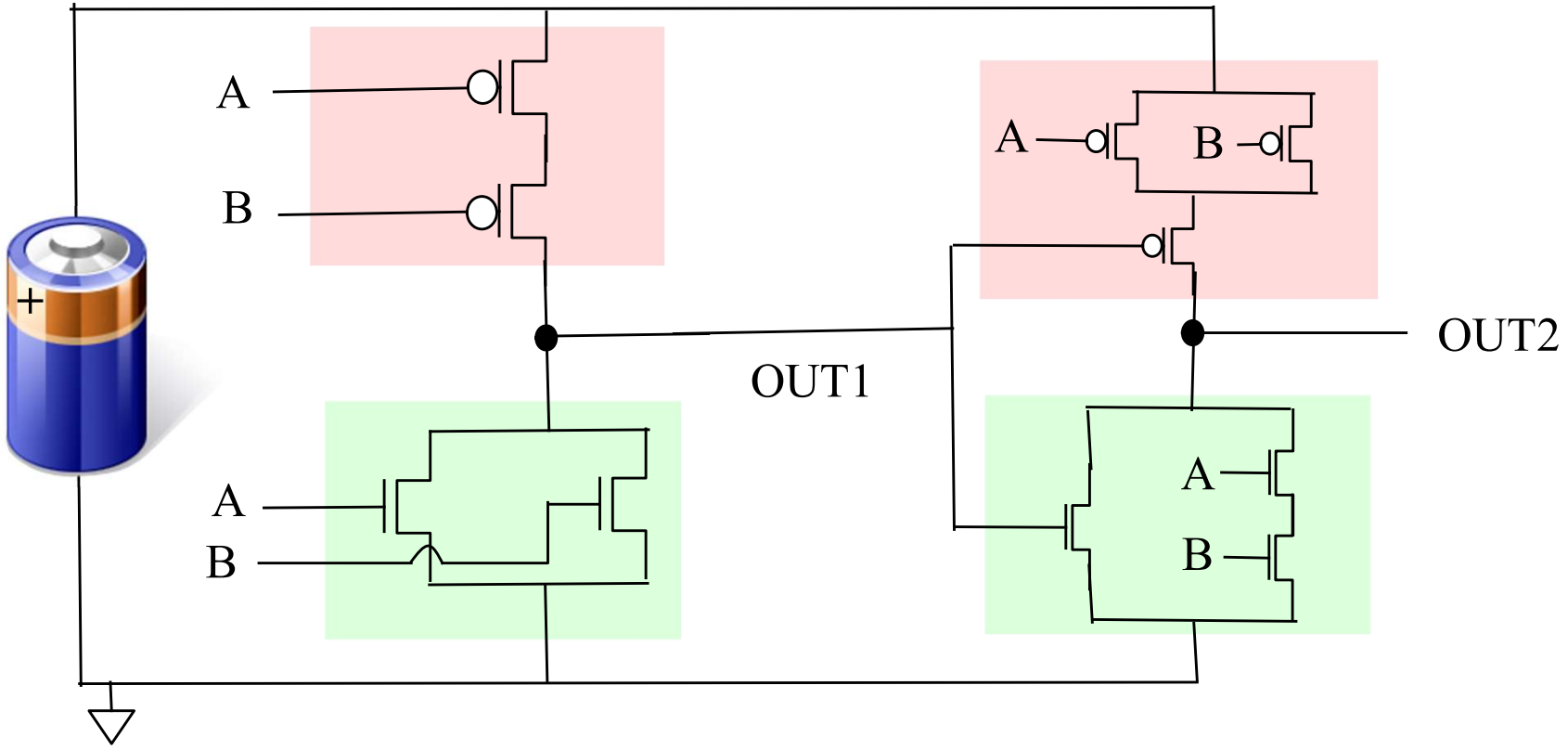
Truth Table

Problème 4

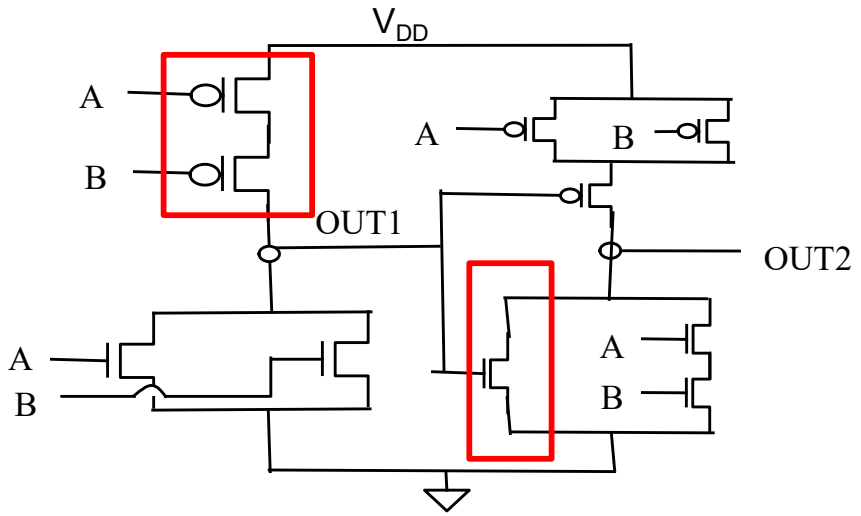
Problème 4a: XOR en CMOS

Vérifiez que la table de vérité correspond à un XOR.

10 transistors



XOR: analyse

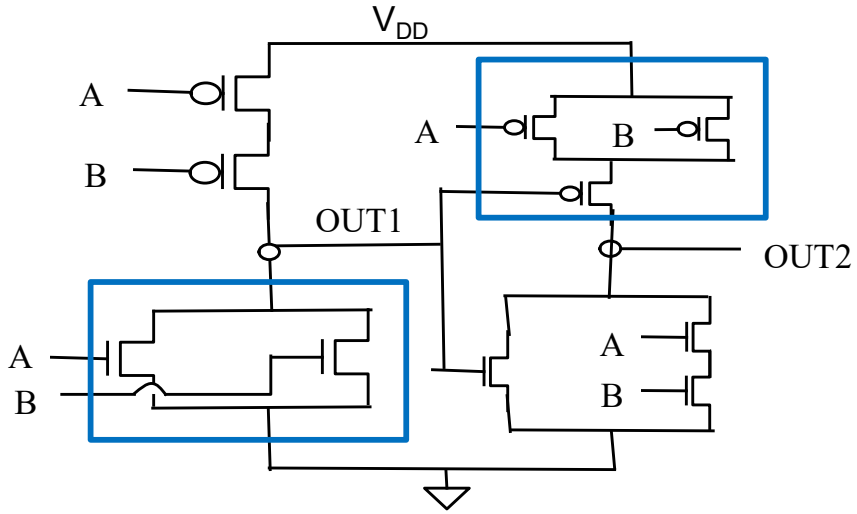


XOR

1)

A	B	OUT1	OUT2
0	0		
0	1		
1	0		
1	1		

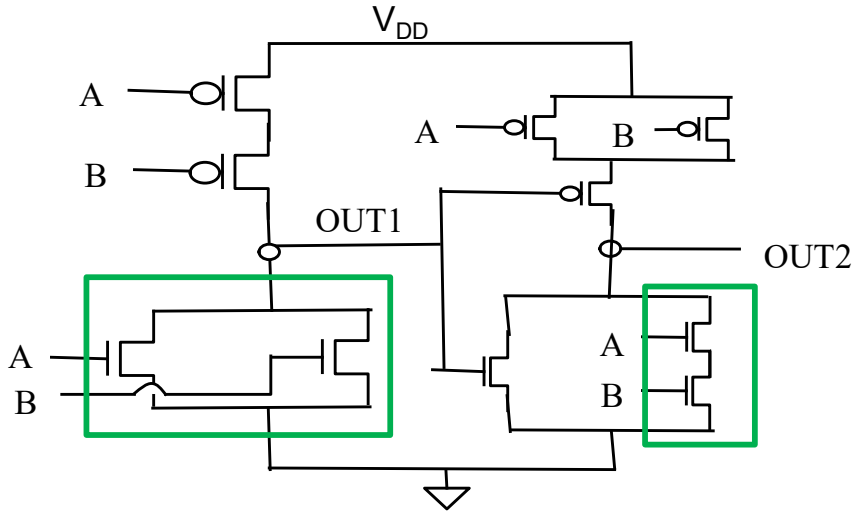
XOR: analyse



XOR

	A	B	OUT1	OUT2
1)	0	0	1	0
2)	0	1		
	1	0		
	1	1		

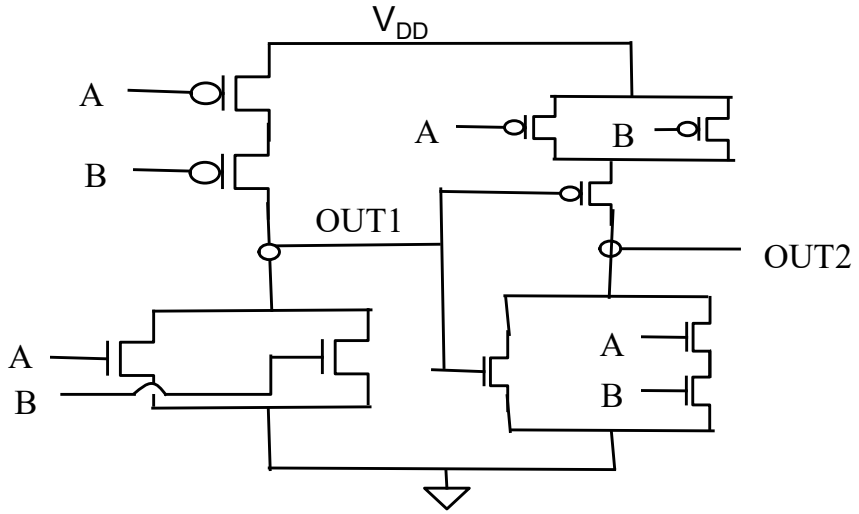
XOR: analyse



XOR

	A	B	OUT1	OUT2
1)	0	0	1	0
2)	0	1	0	1
2)	1	0	0	1
3)	1	1		

XOR: analyse



XOR

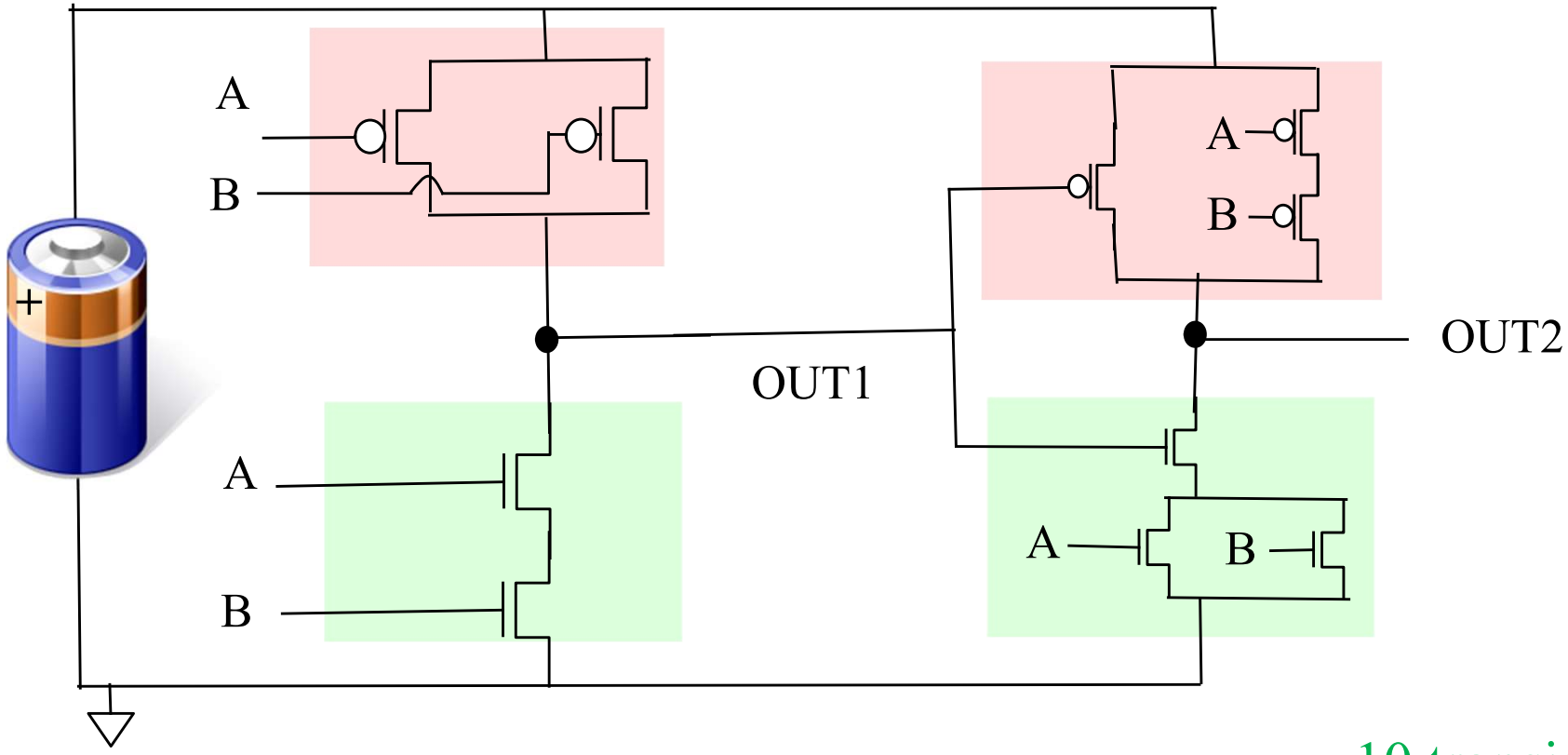
	A	B	OUT1	OUT2
1)	0	0	1	0
2)	0	1	0	1
2)	1	0	0	1
3)	1	1	0	0

NOR

Problème 4b: XNOR en CMOS

A faire par vous-même:

Vérifiez que la table de vérité correspond à un XNOR.

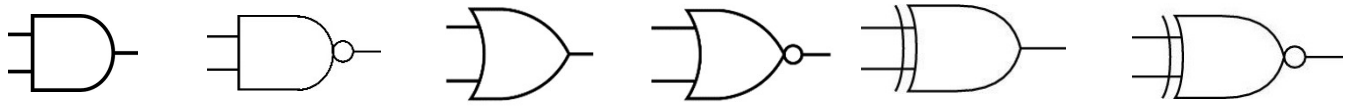


10 transistors

Table de résumé des circuits 2x1 en logique CMOS

Summary for all 2-input gates							
Inputs		Output of each gate					
A	B	AND	NAND	OR	NOR	EX-OR	EX-NOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

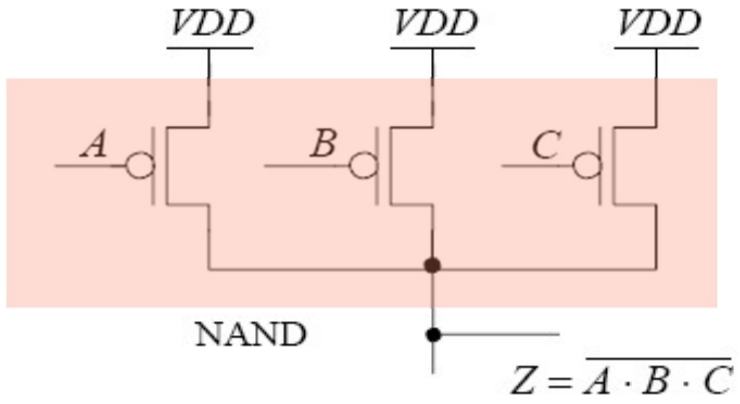
Nb. transistors: **6T** **4T** **6T** **4T** **10T** **10T**

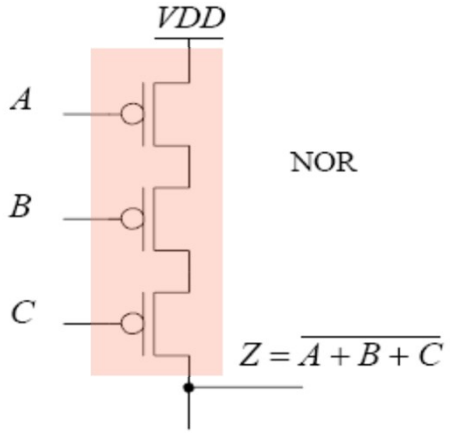


http://www.kpsec.freeuk.com/gates.htm

Circuits logiques généralisés: principes

A) Partie « supérieure » construite sur PMOS:

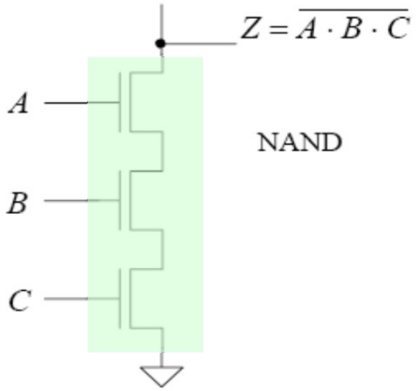


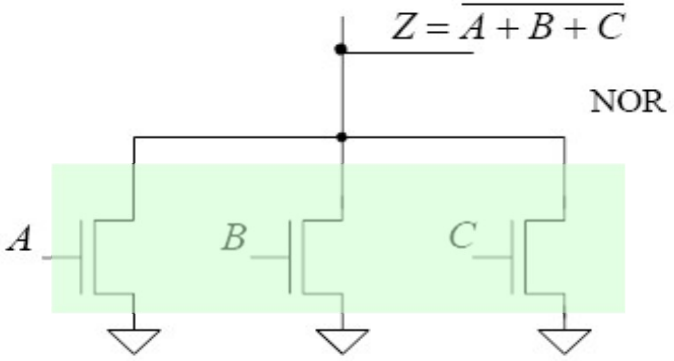


B) Partie « inférieure » construite sur NMOS:

"." = AND
"+"=OR

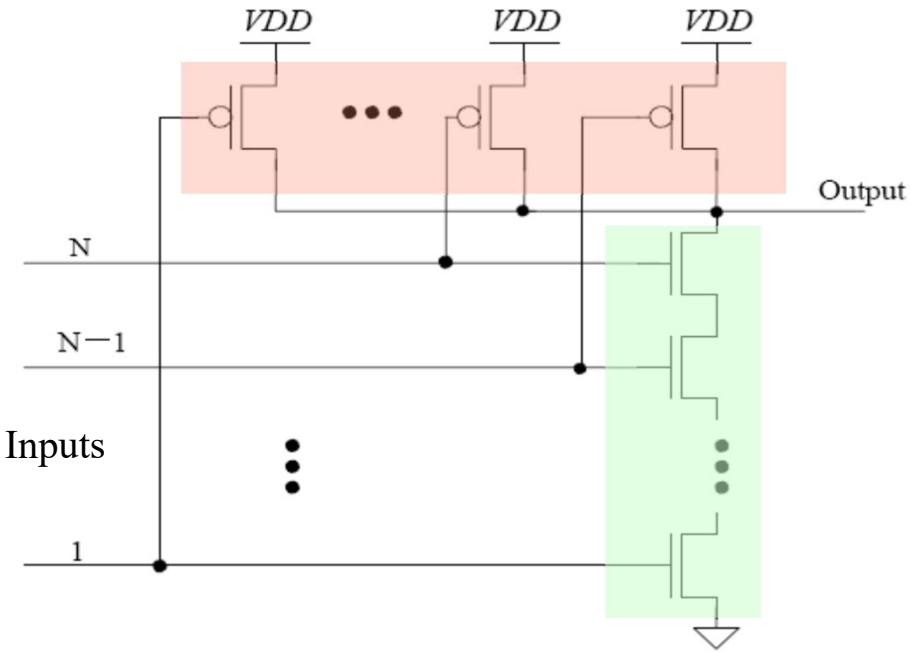
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press





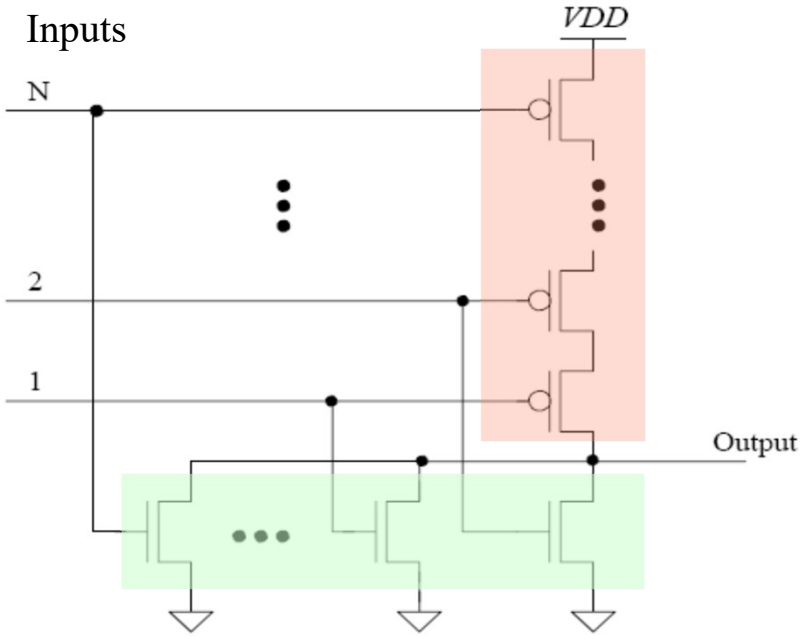
Circuits logiques à plusieurs entrées: exemples (1)

Generalized NAND



$$Out = \overline{A \cdot B \cdot C}$$

Generalized NOR



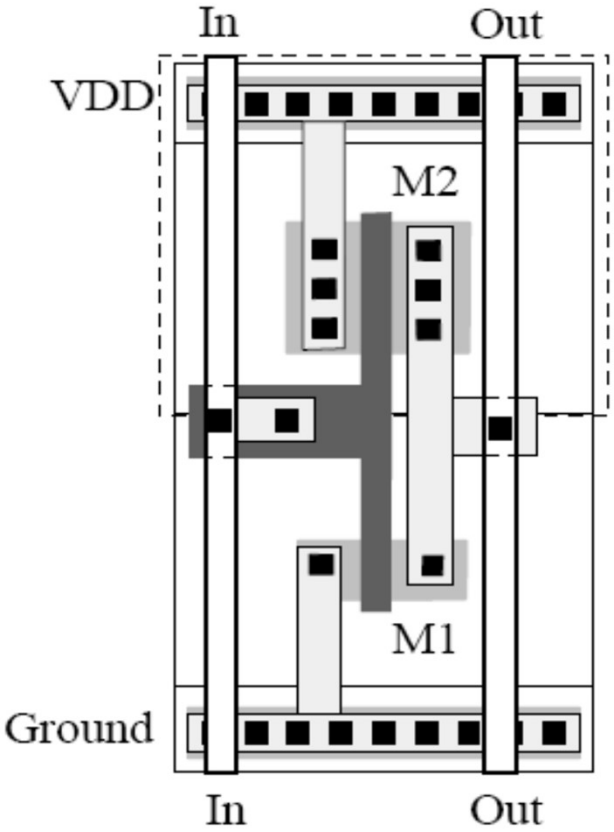
$$Out = \overline{A + B + C}$$

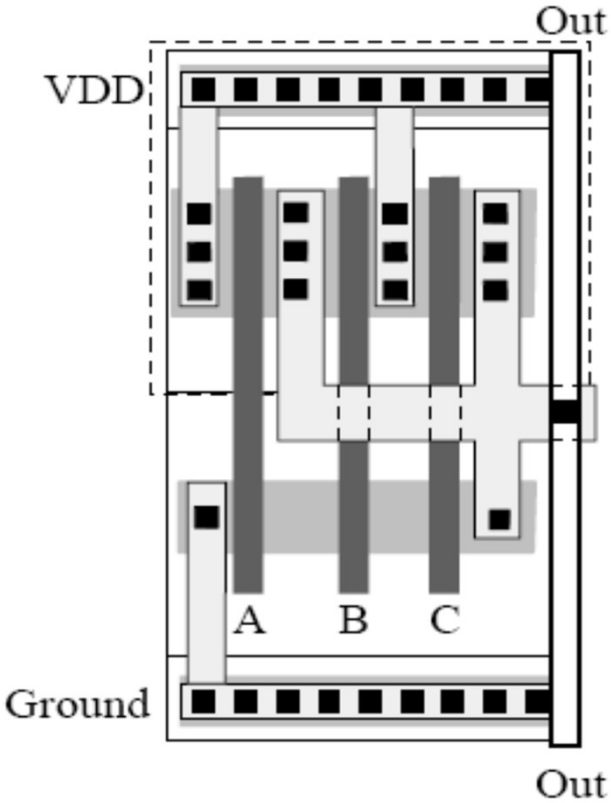
R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

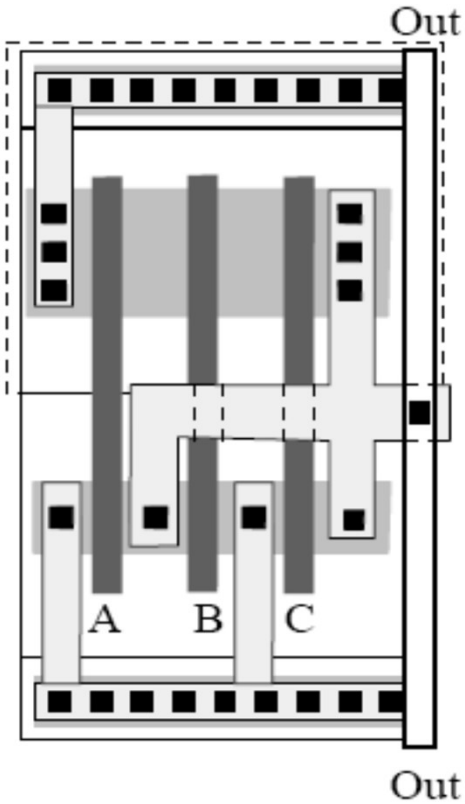
Problème 5

Problème 5

- **Quels sont ces trois circuits logiques ?**
- **Où sont les NMOS et les PMOS ?**

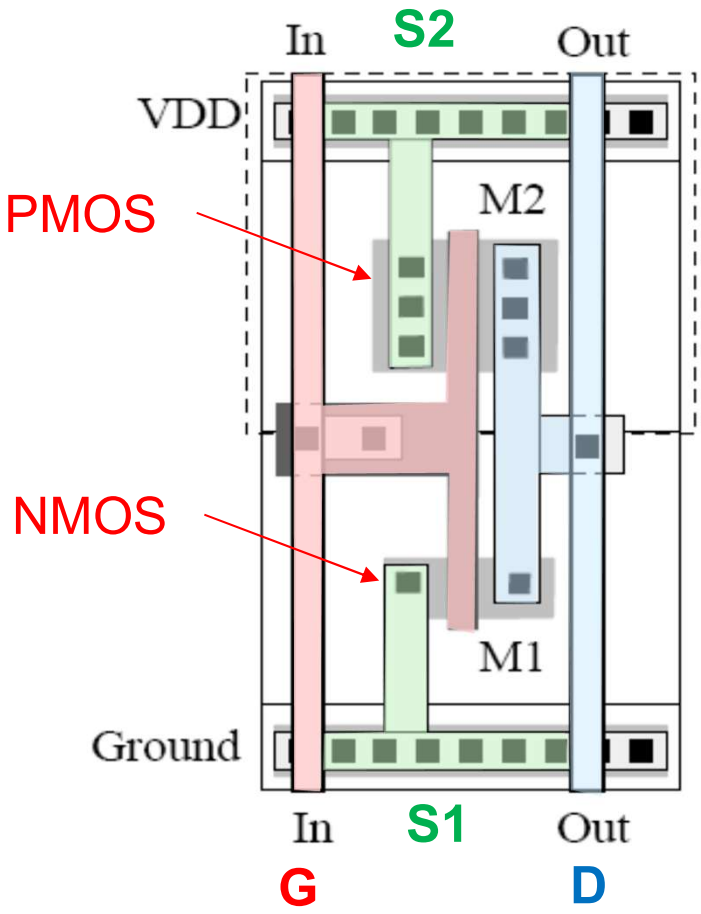


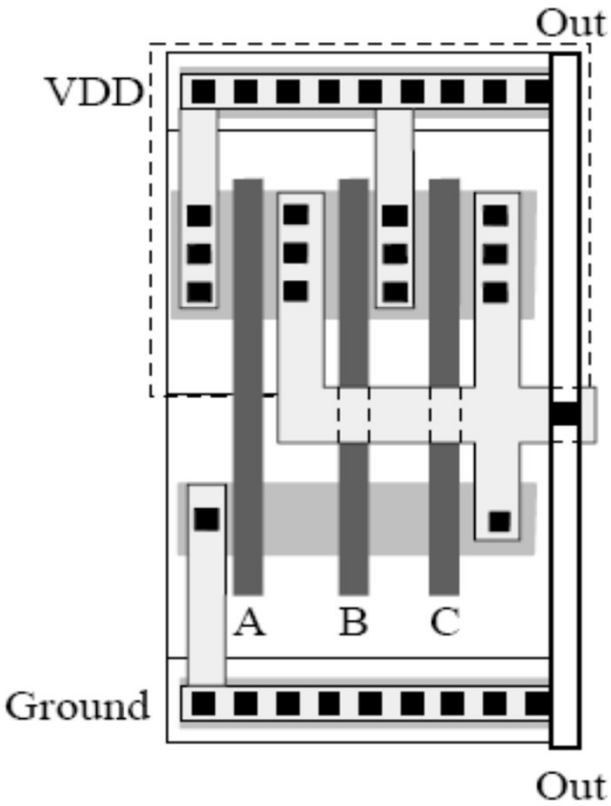


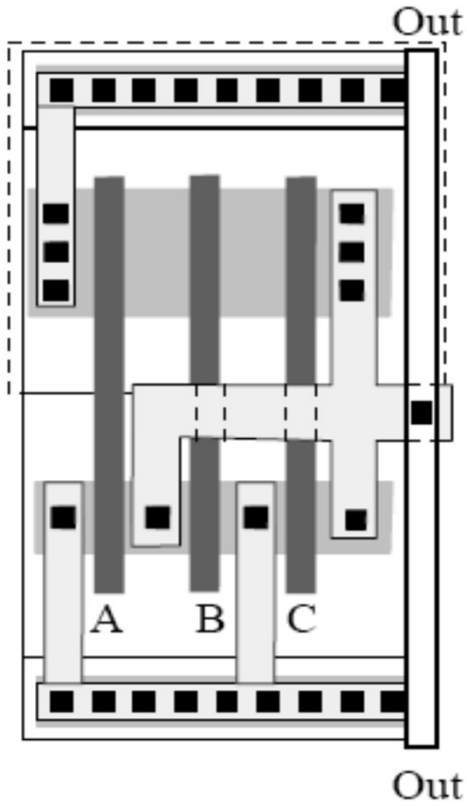


Problème 5

Inverseur

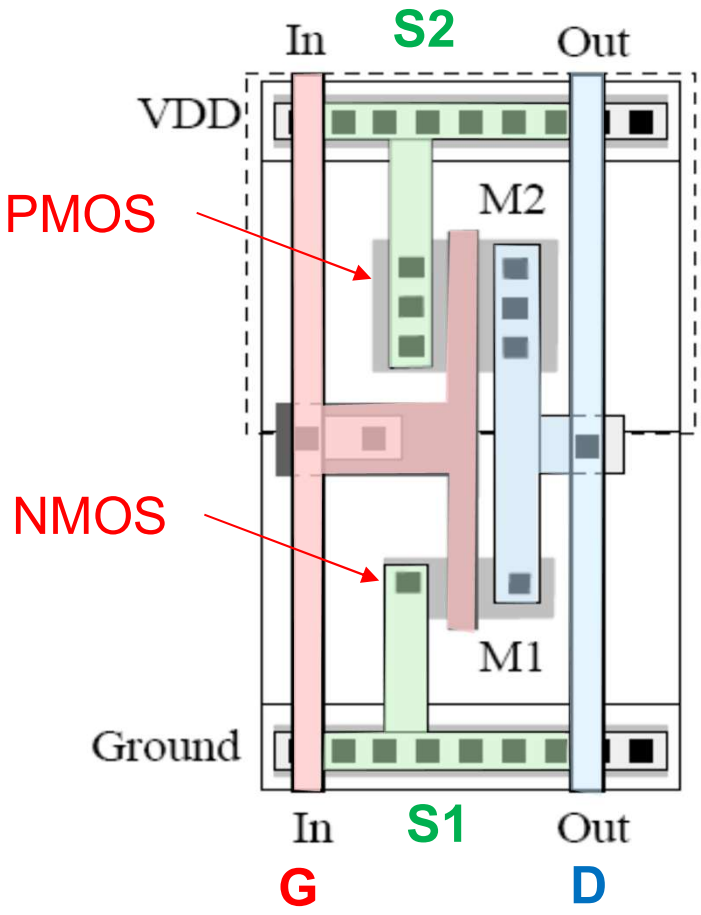




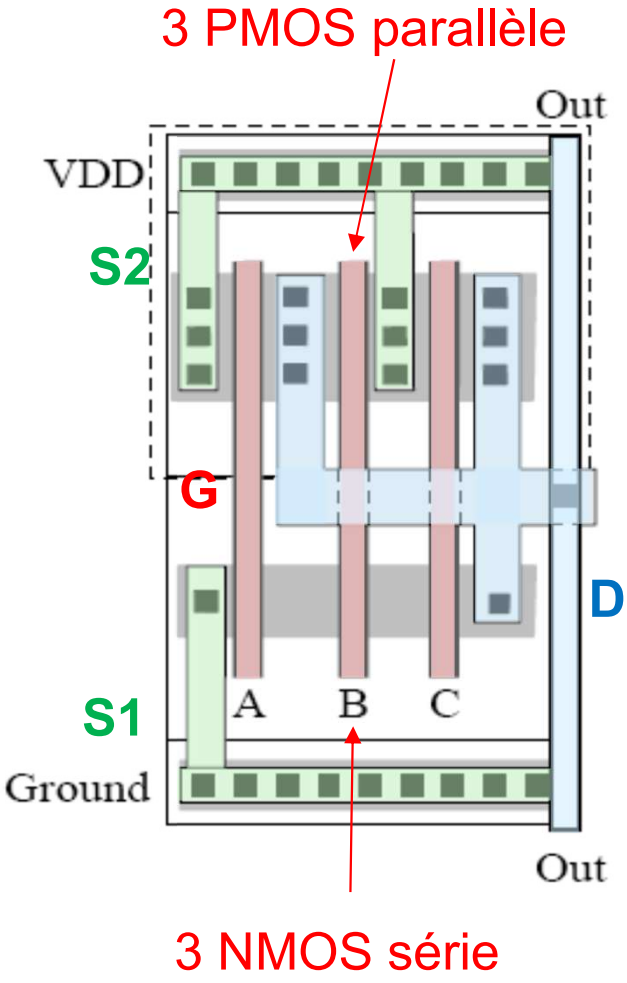


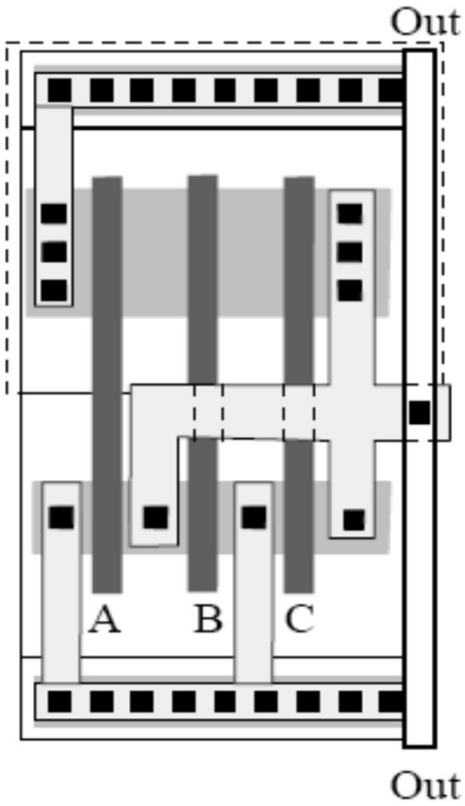
Problème 5

Inverseur



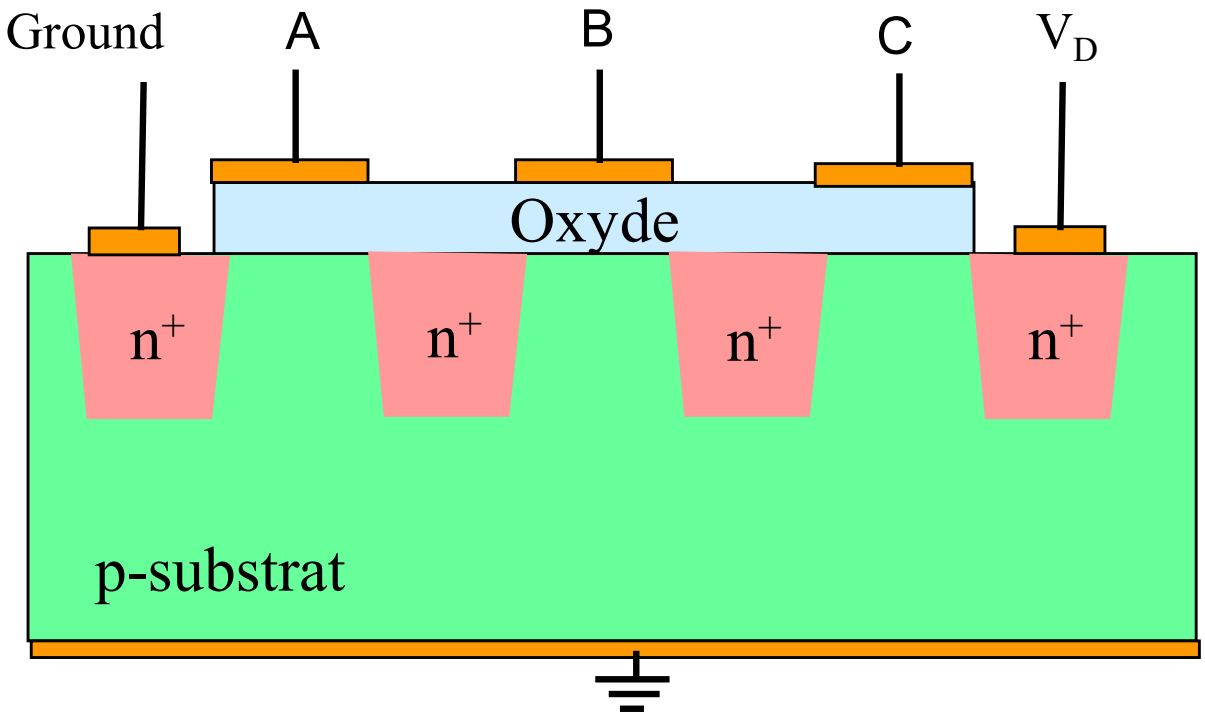
NAND

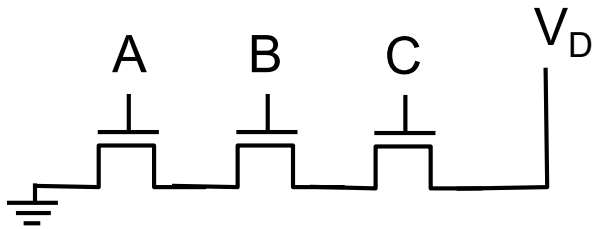


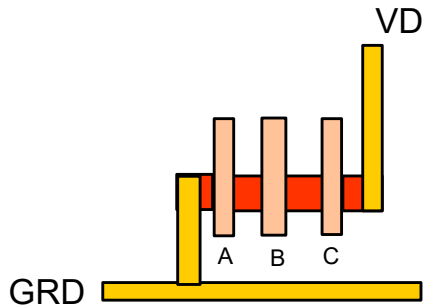


FET multi-gates

NMOS multi-gates

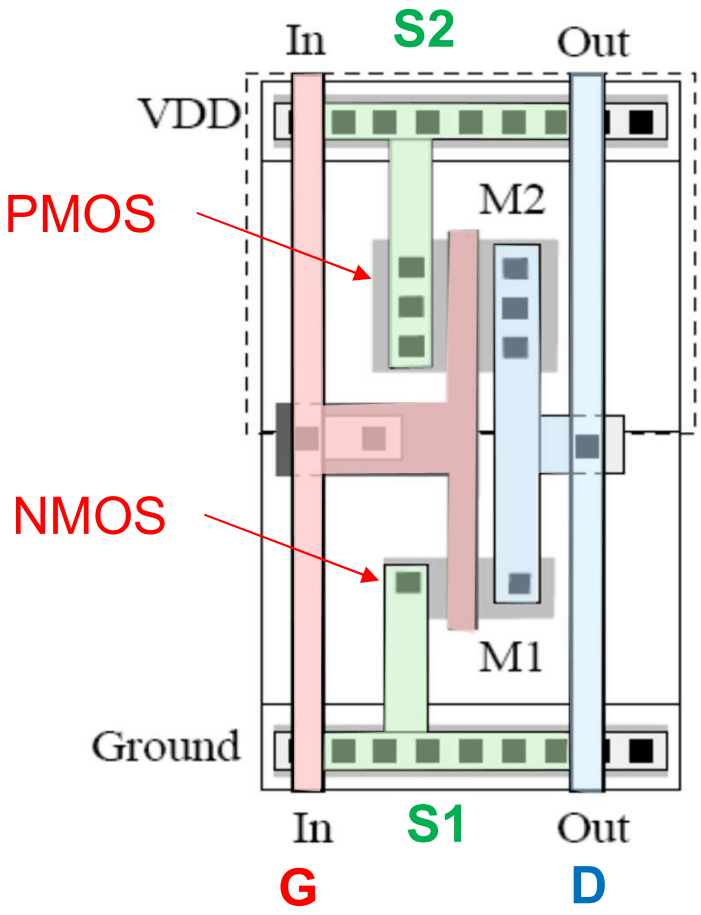




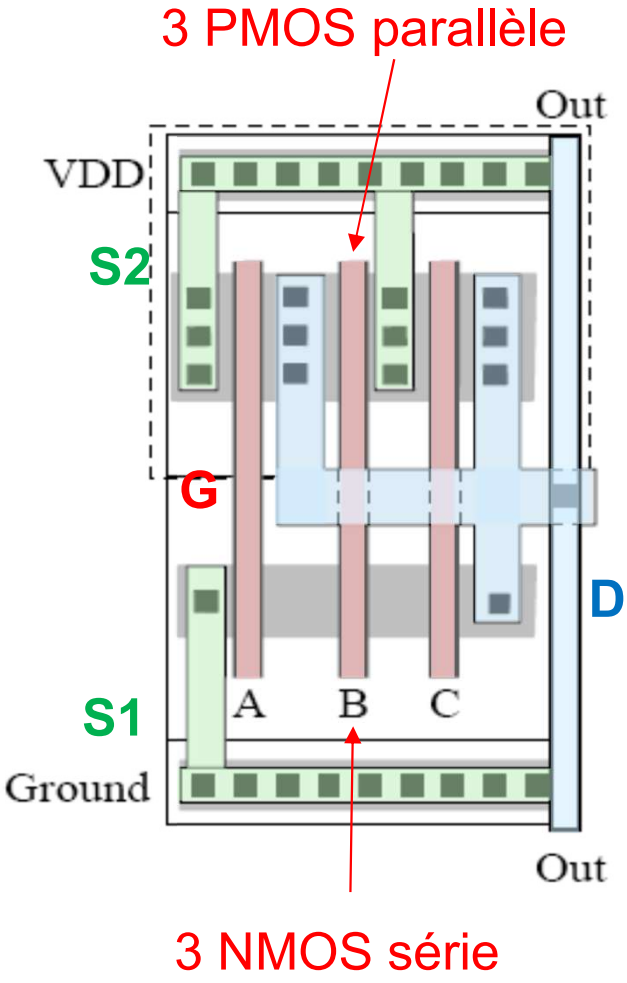


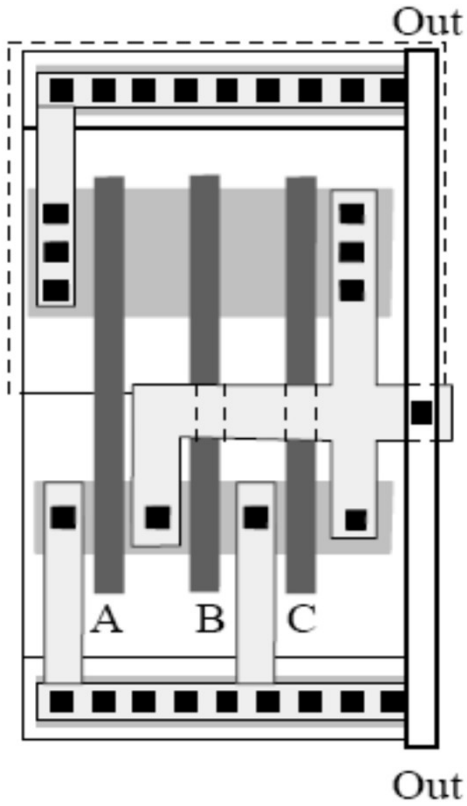
Problème 5

Inverseur



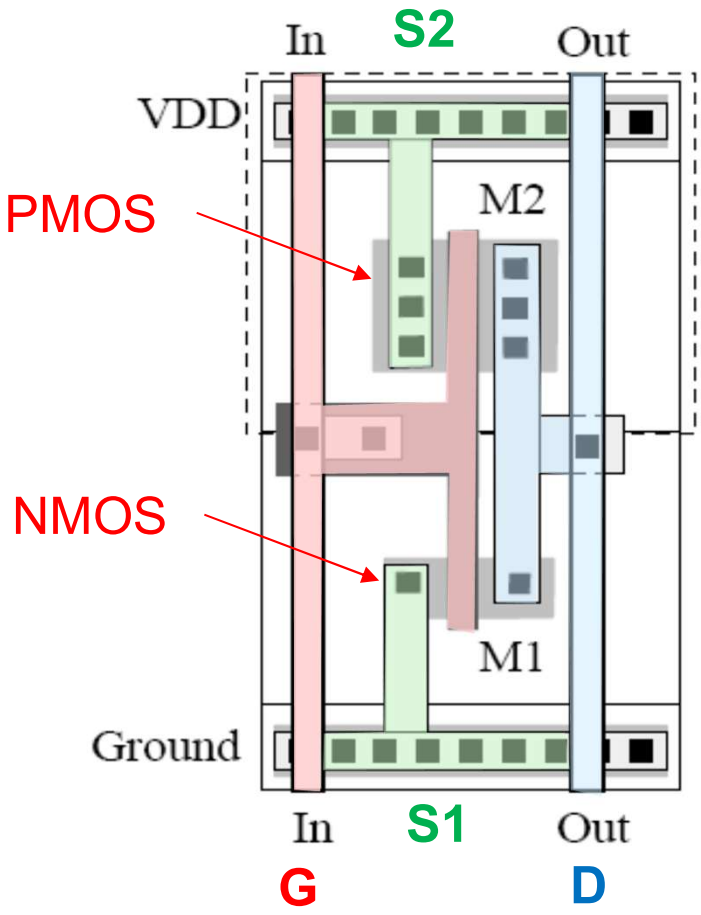
NAND



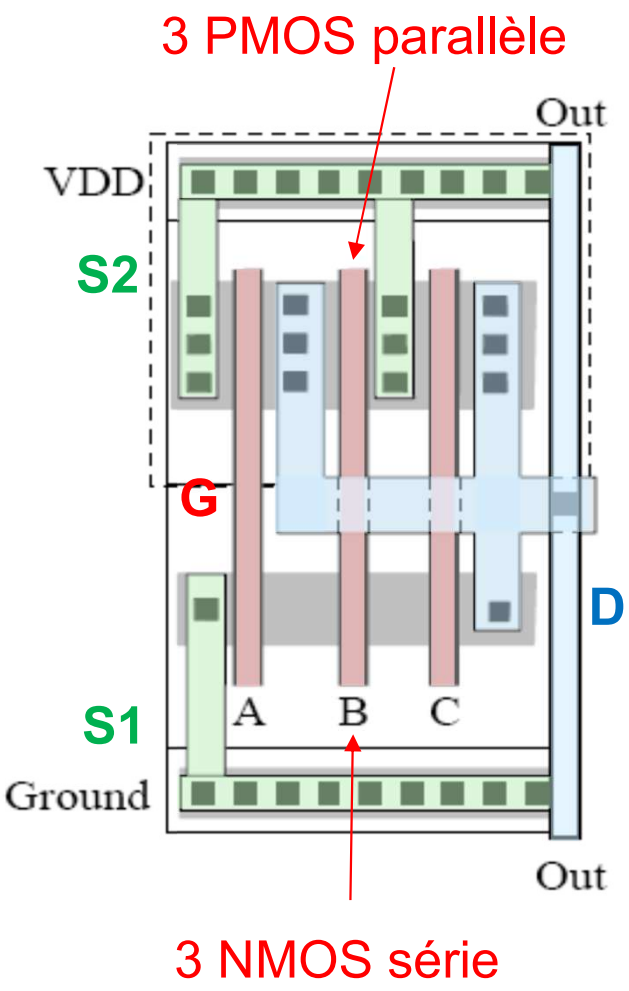


Problème 5

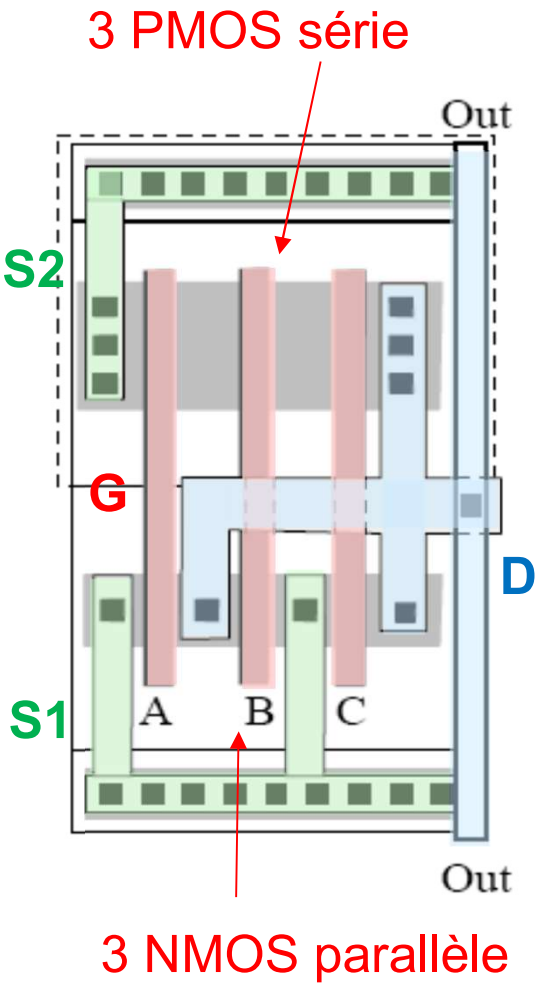
Inverseur



NAND

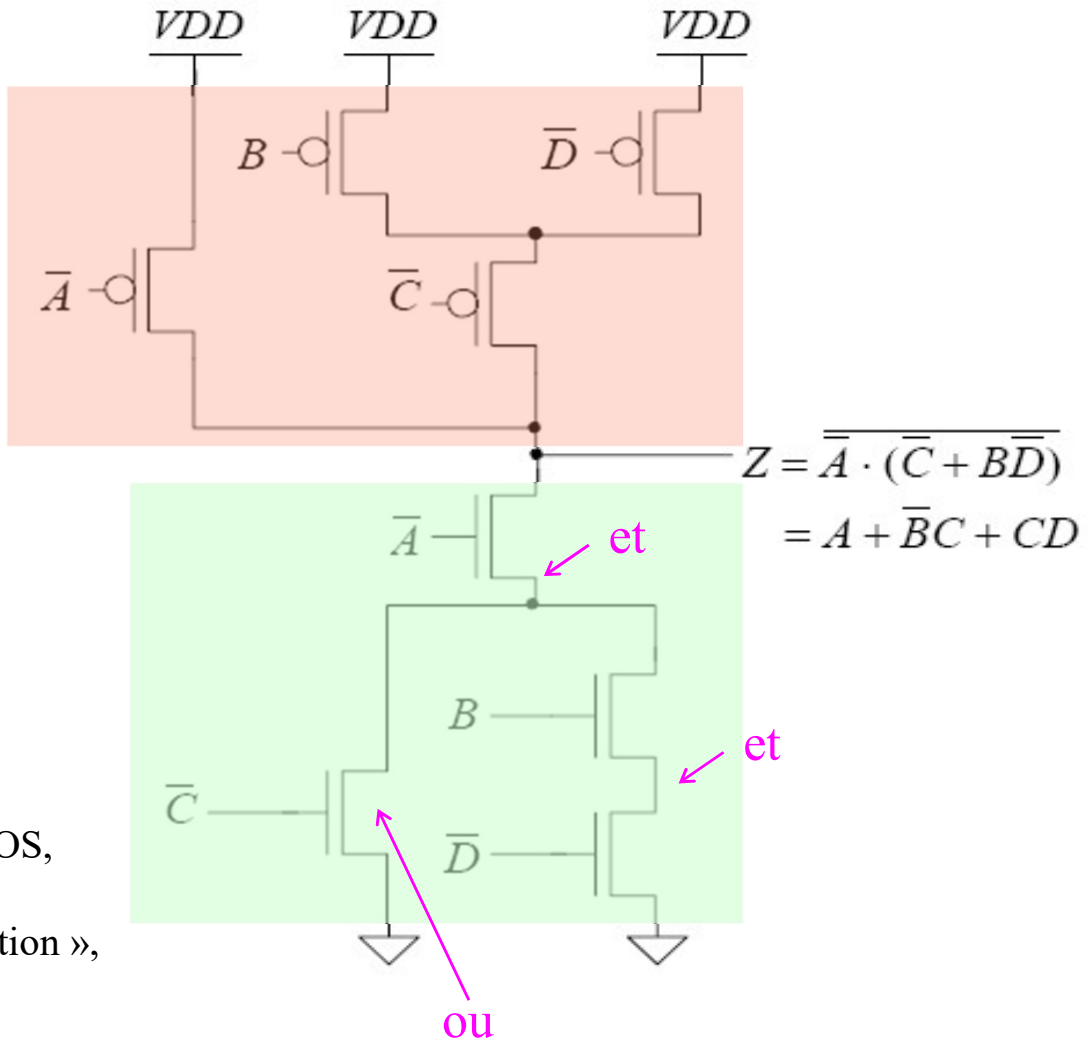


NOR



Circuits logiques à plusieurs entrées: exemples (2)

Obtenir un «0» si:



Partie PMOS

Partie NMOS

NMOS passant →

$\overline{A}$ et [$\overline{C}$ ou (B et $\overline{D}$)]

R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

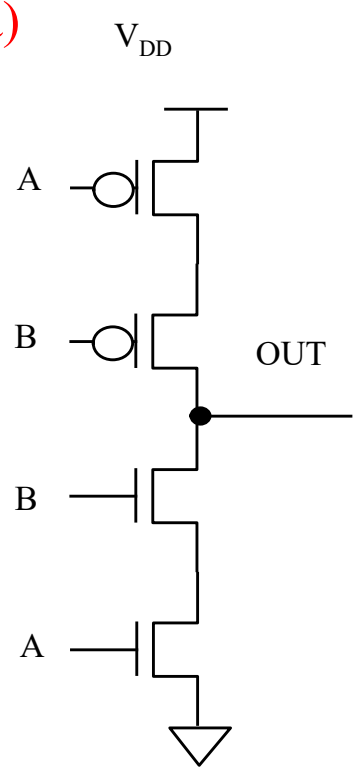
"." = AND
"+"=OR

Problème 6a

Problème 6a

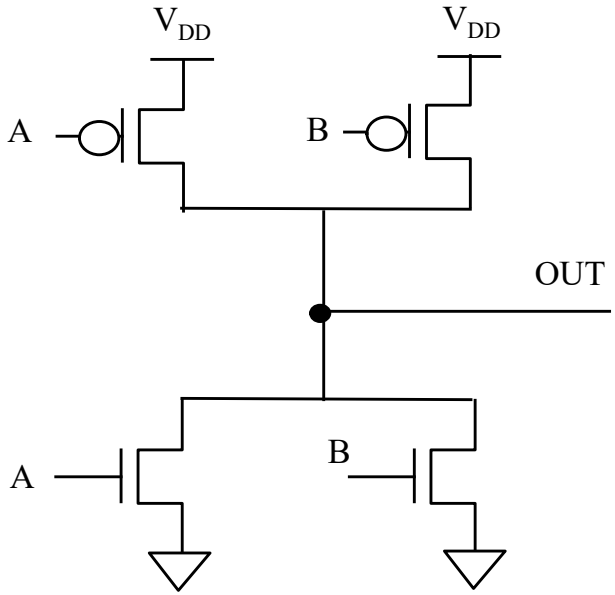
Ces structures sont-elles complémentaires ?

a)



A	B	Out
0	0	
0	1	
1	0	
1	1	

b)



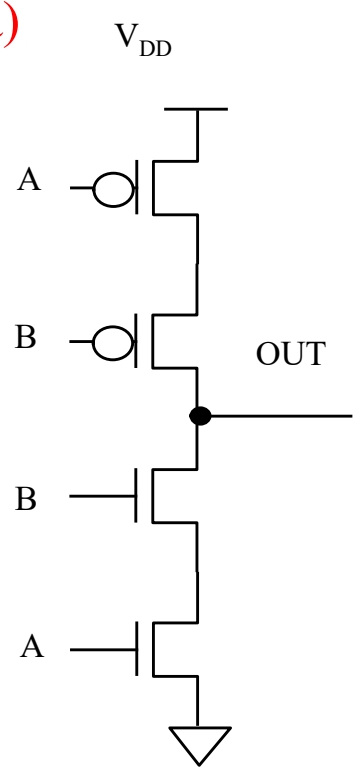
A	B	Out
0	0	
0	1	
1	0	
1	1	

Si nécessaire, déterminez leurs tables de vérité !

Problème 6a

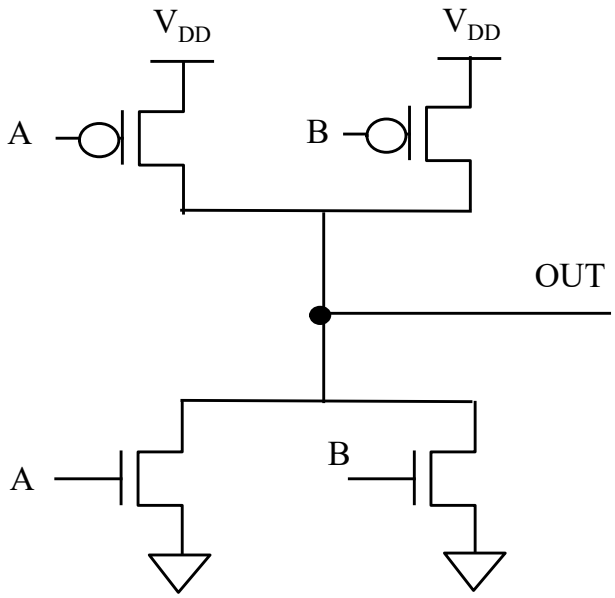
Ces structures sont-elles complémentaires ?

a)



A	B	Out
0	0	1
0	1	**floating**
1	0	**floating**
1	1	0

b)



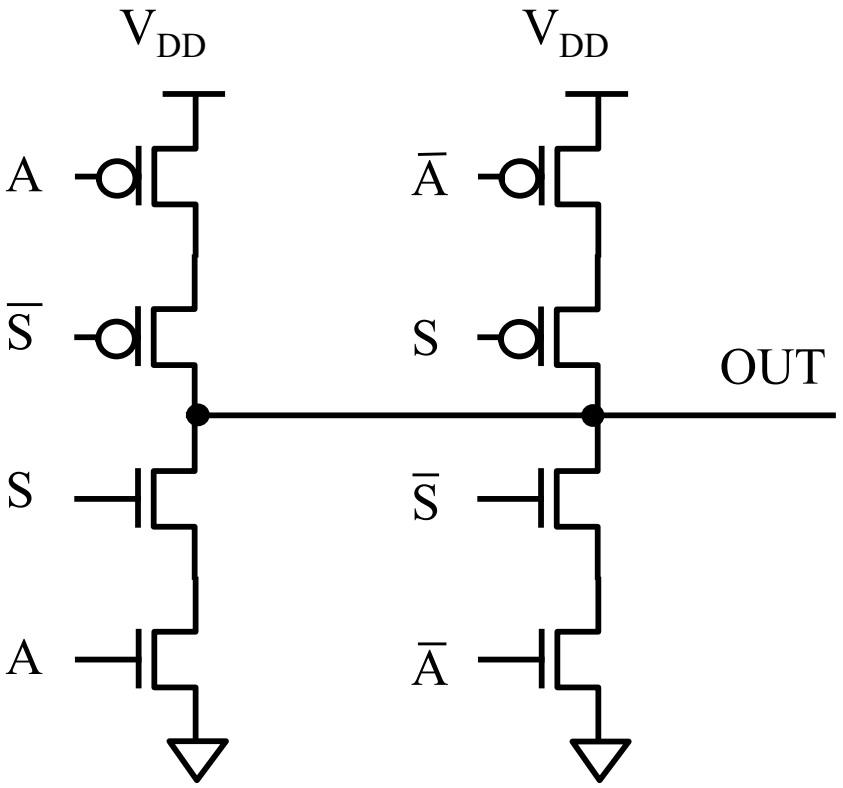
A	B	Out
0	0	1
0	1	**shortcut**
1	0	**shortcut**
1	1	0

Si nécessaire, déterminez leurs tables de vérité !

Problème 6b

Problème 6b

Combien d'étages a cette structure ?
Cette structure pose-t-elle problème ?

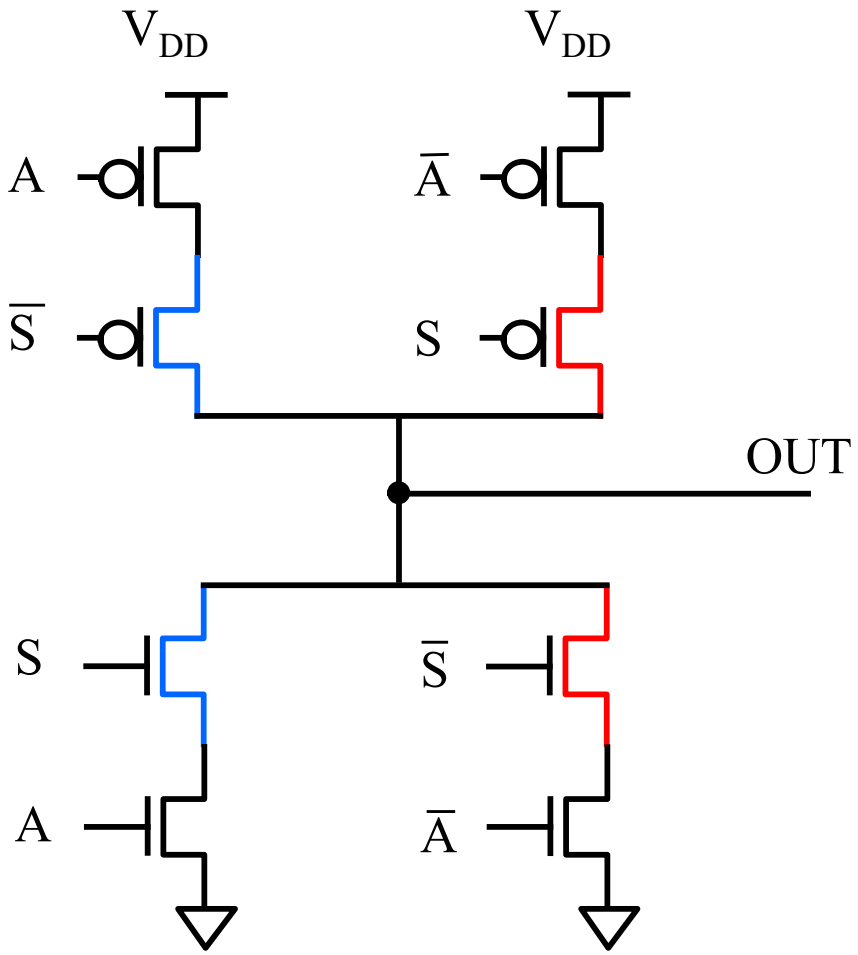


1)
2)

S	A	Out
0	0	
0	1	
1	0	
1	1	

Si nécessaire, déterminez la table de vérité !

Problème 6b

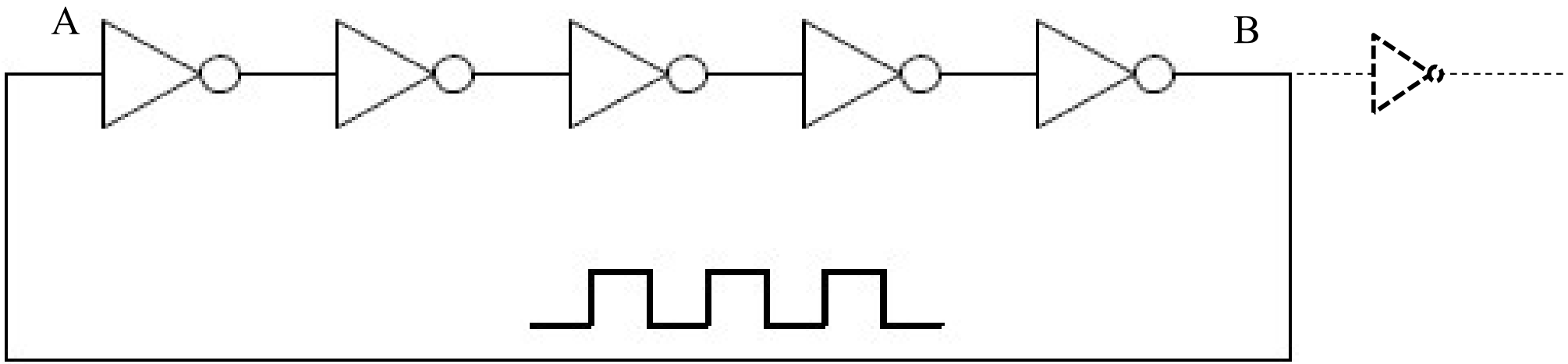


	S	A	Out
1)	0	0	A=0
	0	1	A=1
2)	1	0	$\overline{A}$=1
	1	1	$\overline{A}$=0

1 seul étage

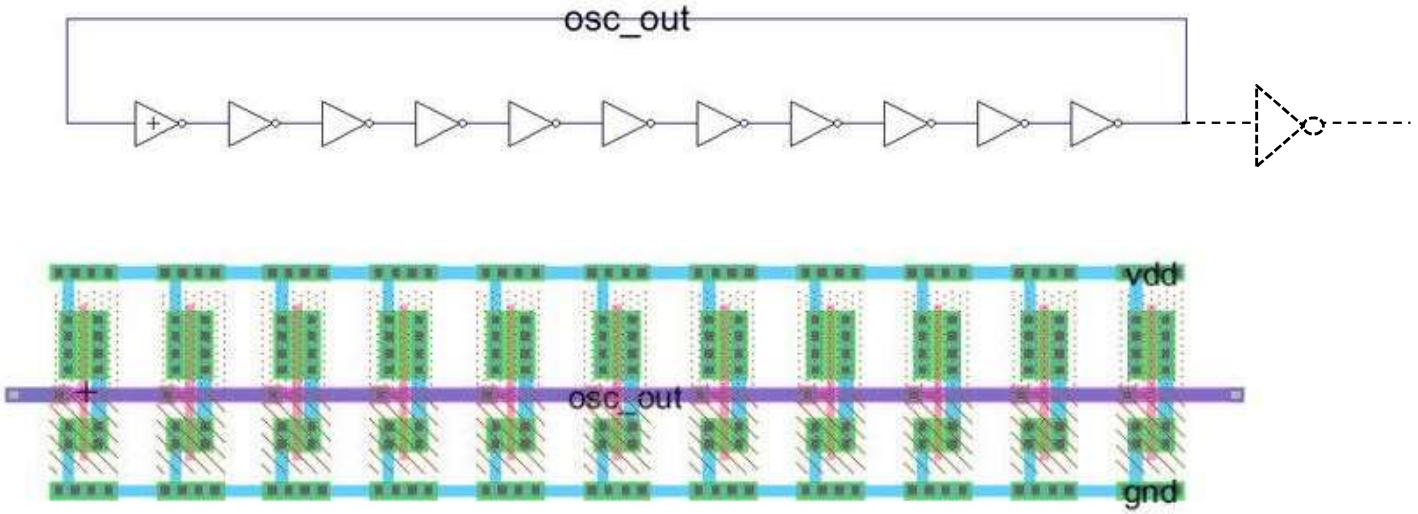
XOR (12 transistors)

Ring oscillator

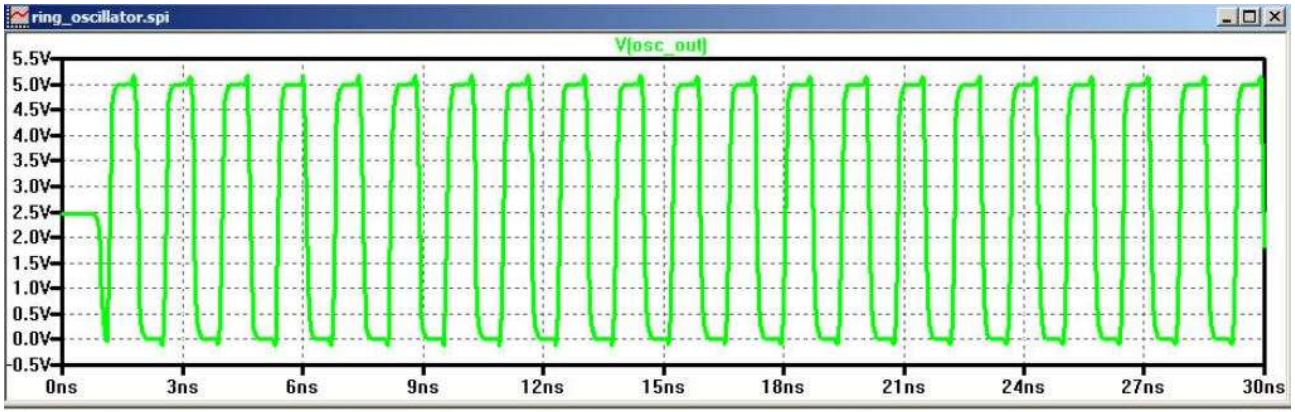


R.J. Baker, « CMOS, circuit design, layout and simulation », IEEE Press

Ring Oscillator



11 inverseurs



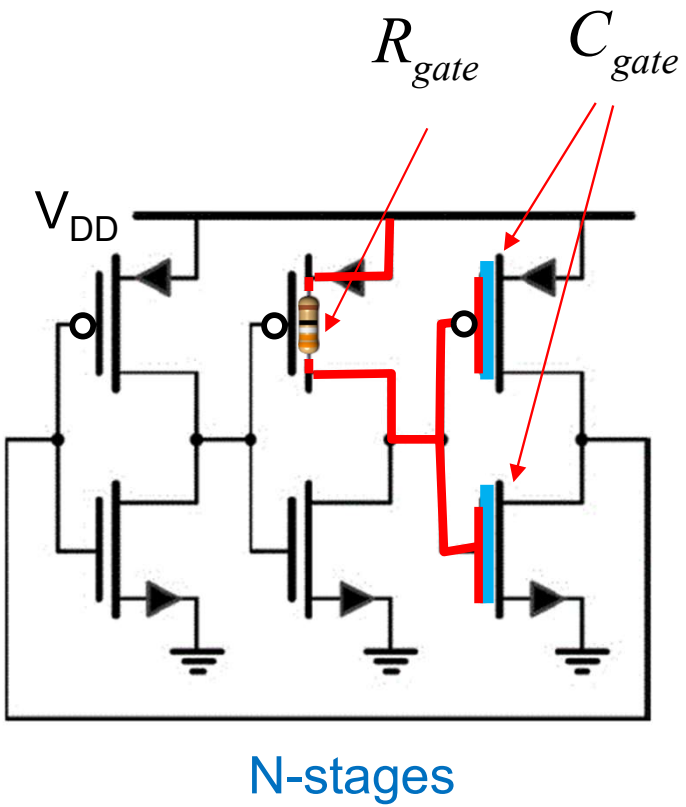
1.5 ns

670 MHz

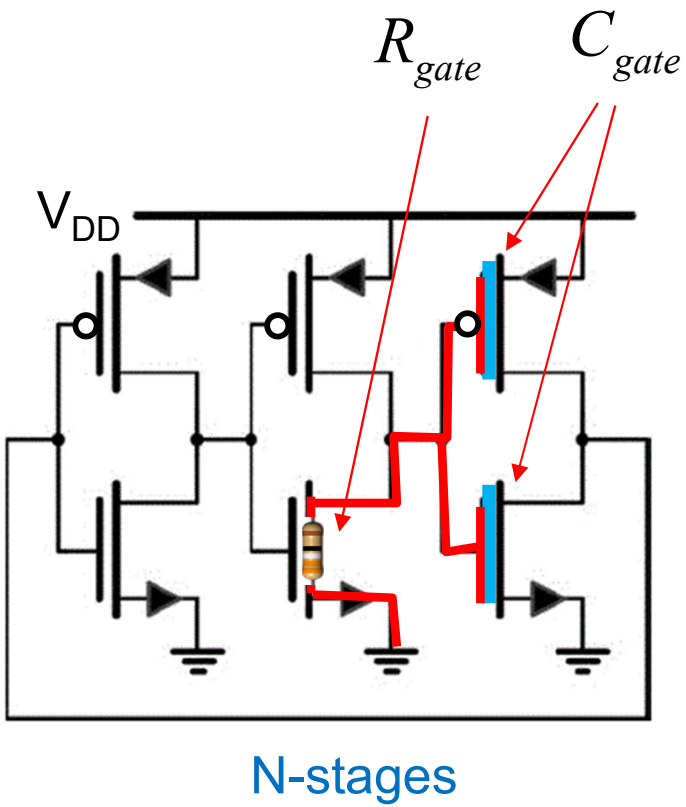
http://cmosedu.com/videos/electric/tutorial5/electric_tutorial_5.htm

Adaptation de la fréquence

Charge



Décharge

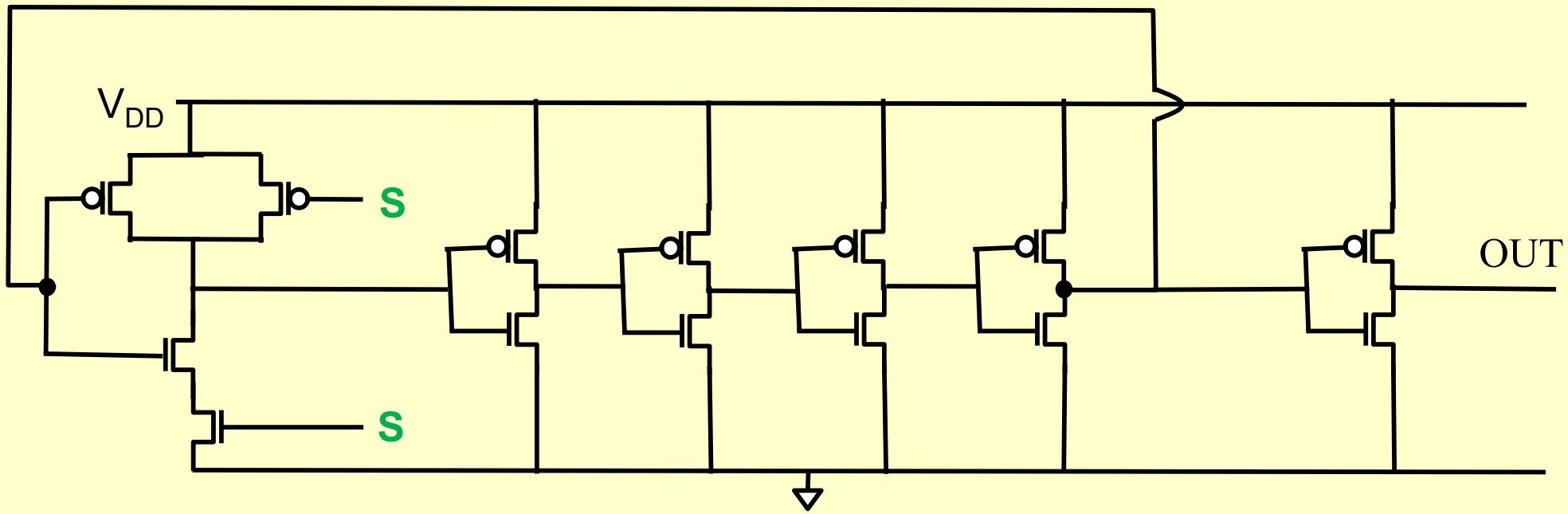


Problème 7a

Problème 7a

Analysez ce schéma

NAND INV INV INV INV INV



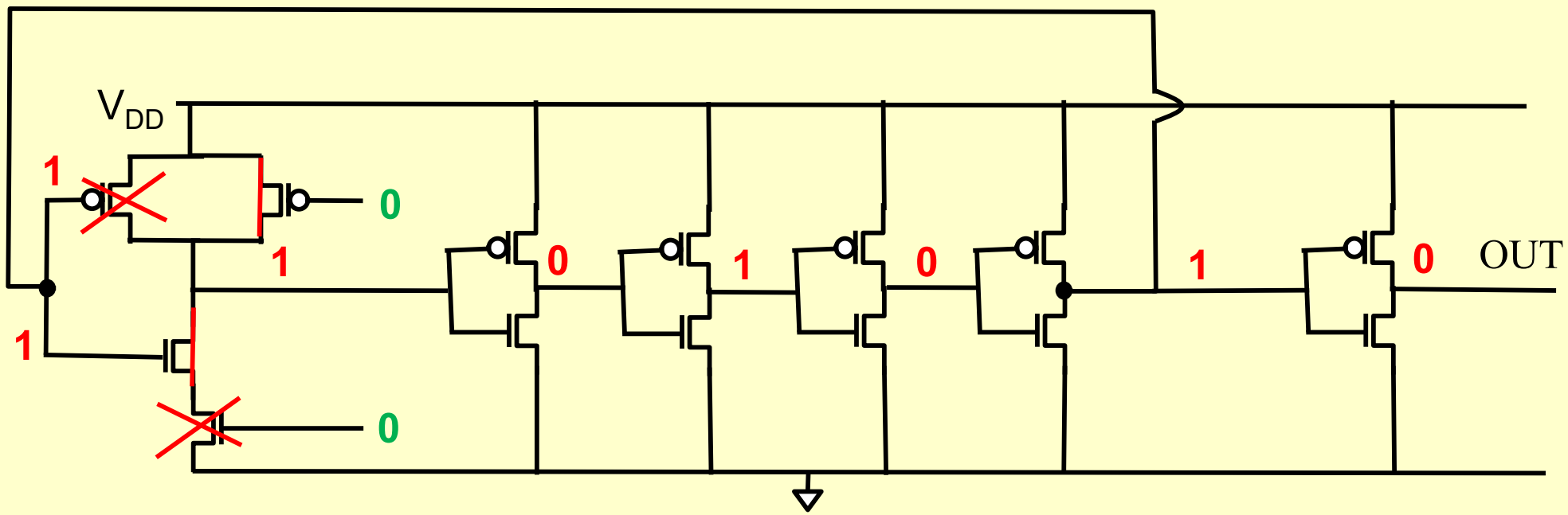
S=«0» → ?

S=«1» → ?

Problème 7a

S=0

NAND INV INV INV INV INV

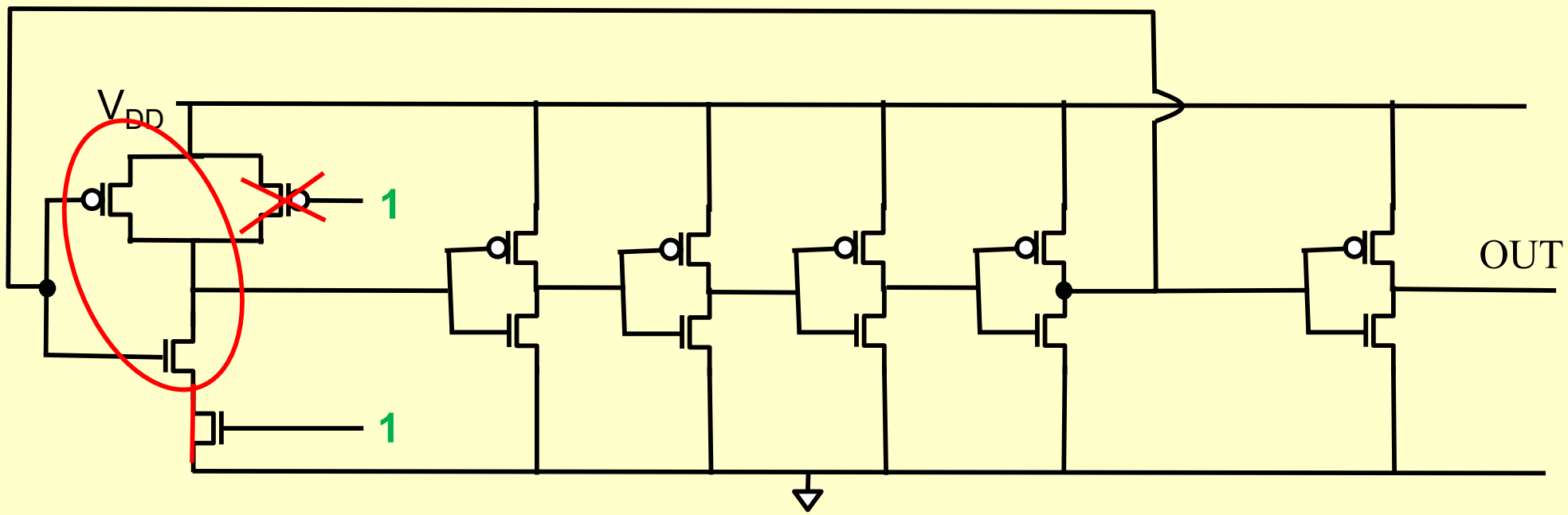


Pas d'oscillation

Problème 7a

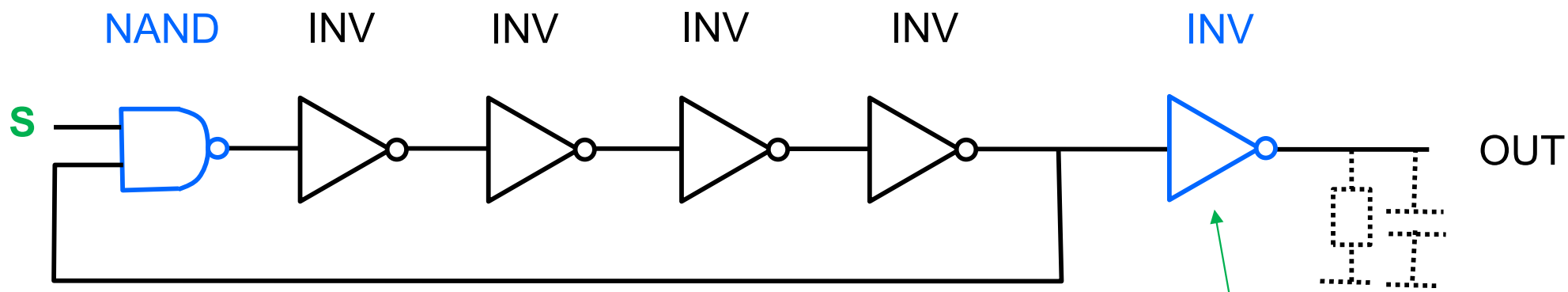
S=1

INV INV INV INV INV INV



5 inverseurs dans le ring → oscillations

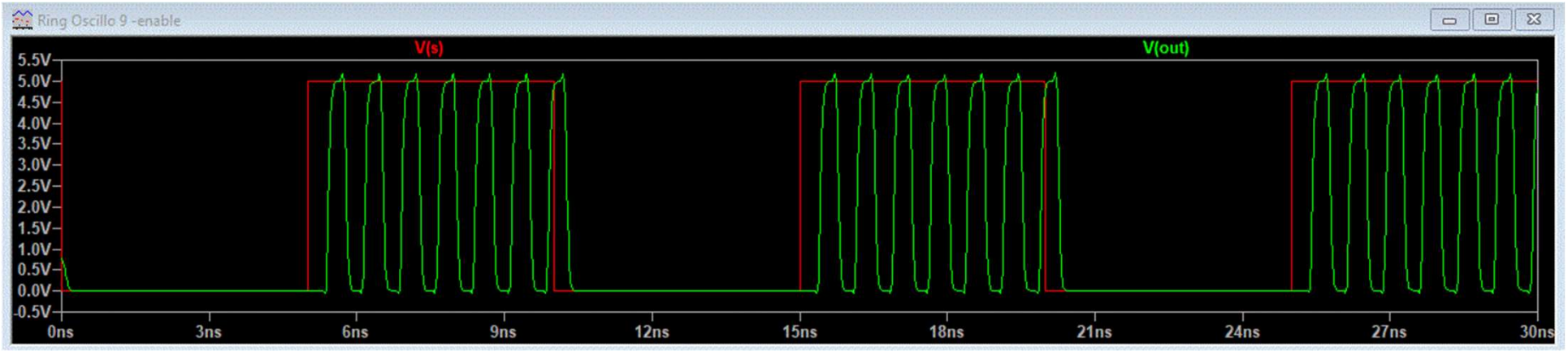
Entrée et sortie du ring oscillateur



«S» = 0 pas d'oscillations

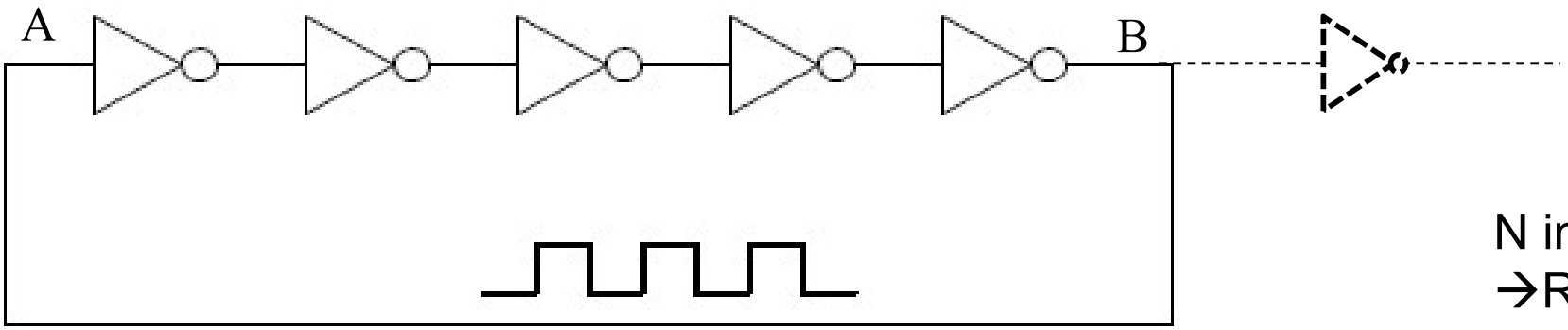
«S» = 1 oscillations

Isolation



Problème 7b

Problème 7b

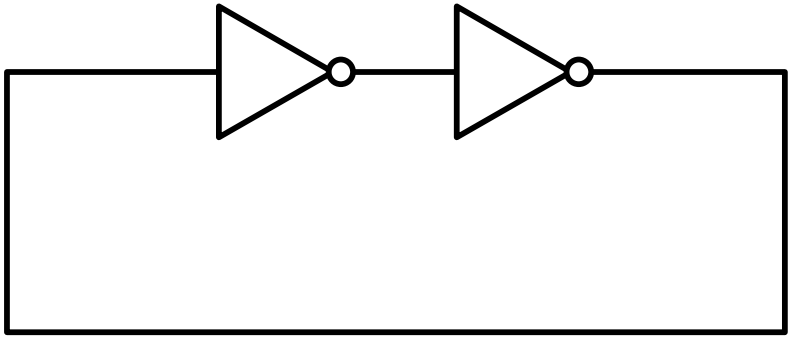


N impair
→Ring oscillator

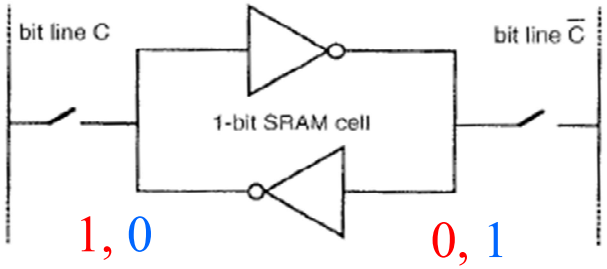
Etudiez le même système mais avec N=2 :

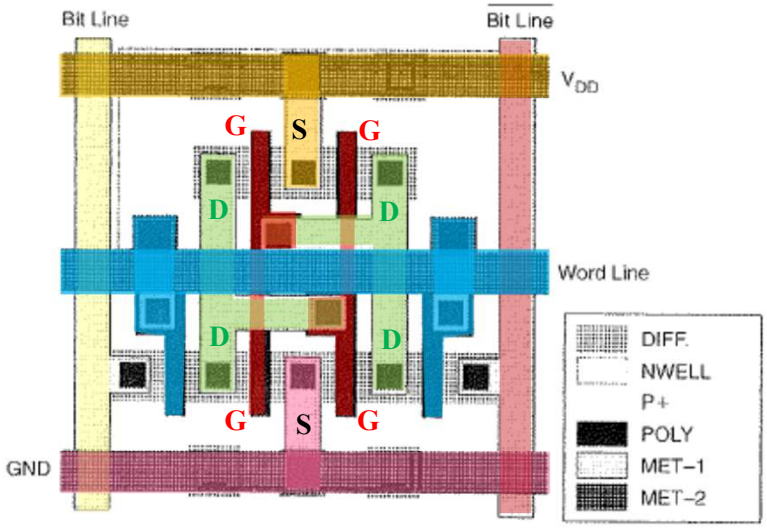
- quels états stables sont possibles ?

- ce design est-il utilisable et comment ?

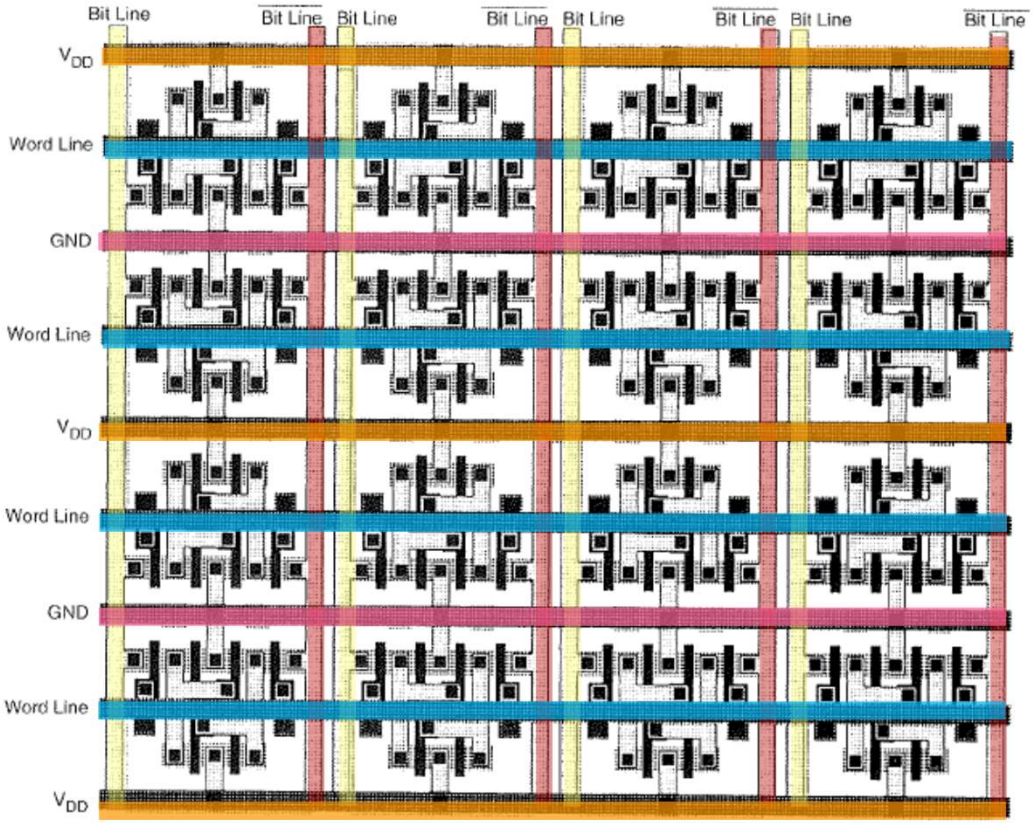


Volatile memories: SRAM





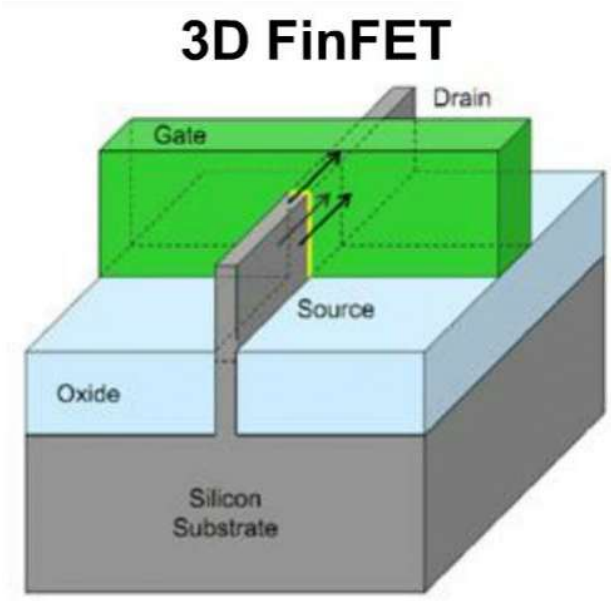
CMOS SRAM cell: layout



4x4 CMOS SRAM

S.M. Kang, Y. Leblebici, “CMOS digital integrated circuits: analysis and design”, McGraw-Hill

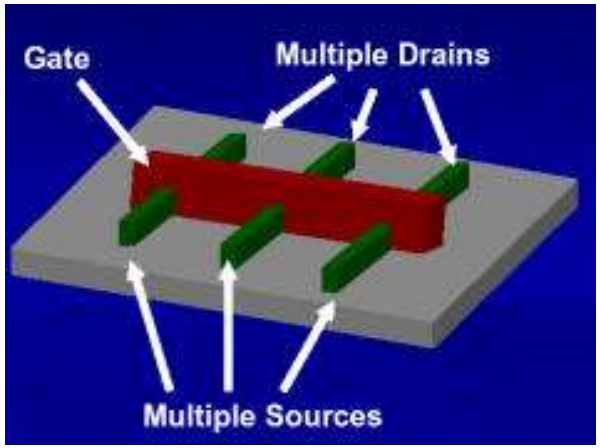
Intel Tri-gate «FinFET»: 14nm gate (2014)



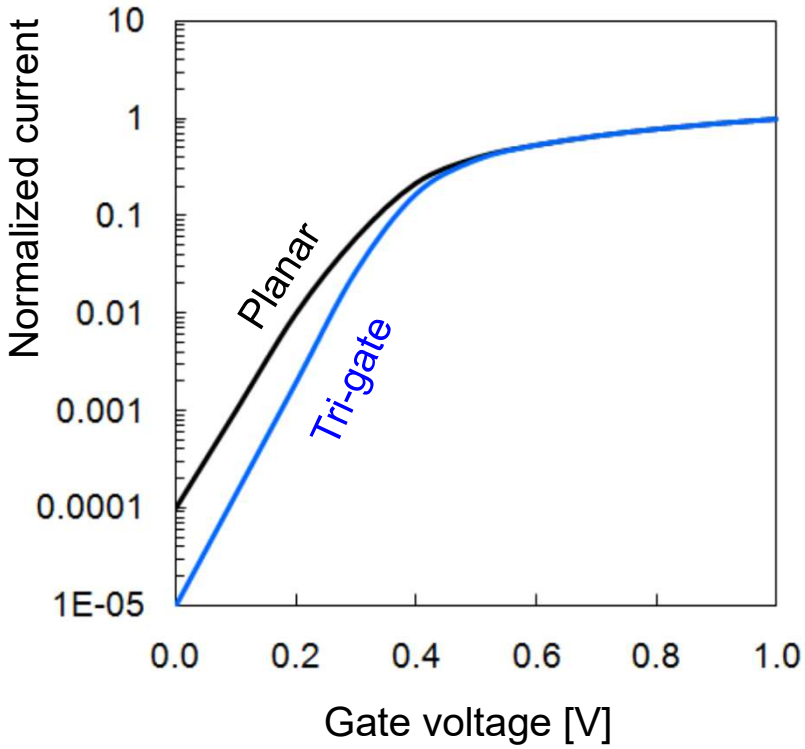
3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

https://www.semiwiki.com/forum/content/1908-finfet-process-modeling-extraction-16-nm-below.html

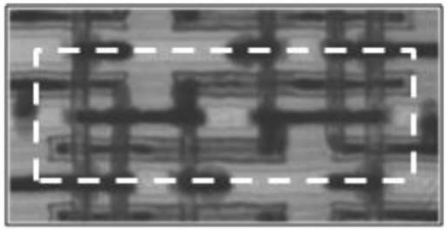
http://en.wikipedia.org/wiki/Multigate_device



M. Bohr «Intel's Revolutionary 22 nm Transistor Technology», INTEL May 2011



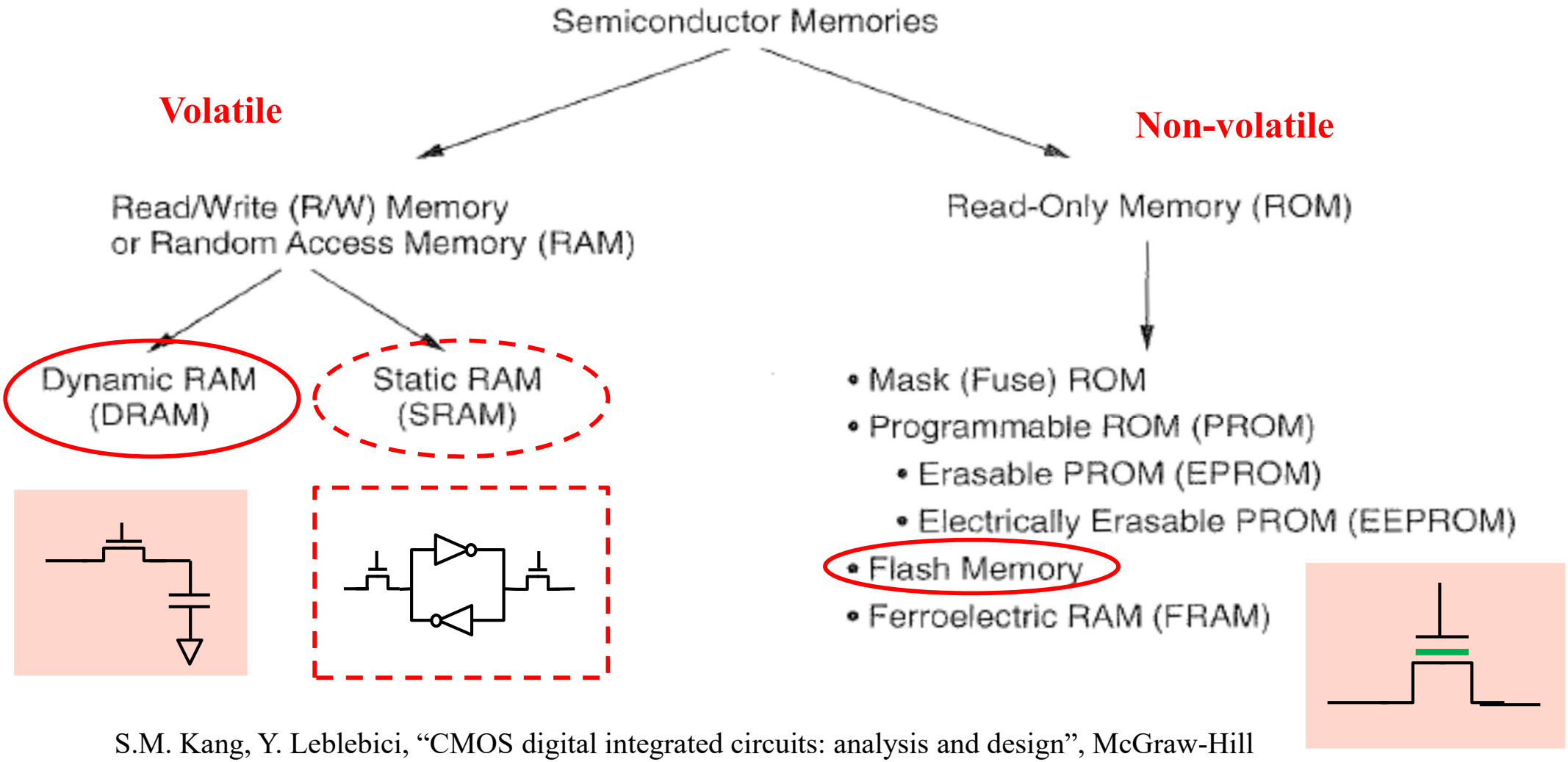
SRAM memory



http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf

.0588 um^2 = 430 nm x 135 nm

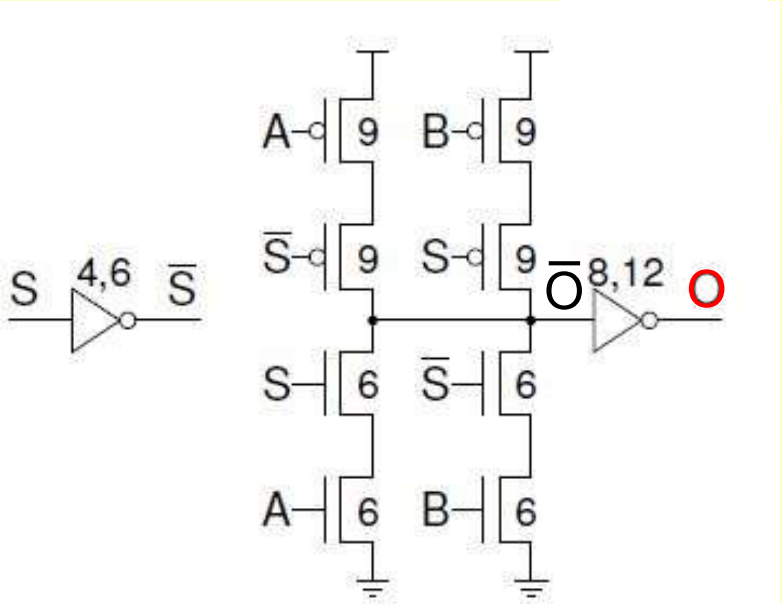
Mémoires électroniques: vue d'ensemble



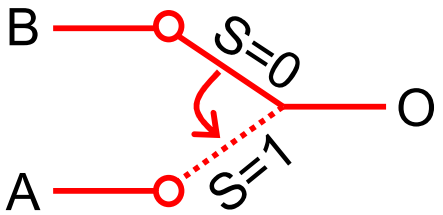
S.M. Kang, Y. Leblebici, "CMOS digital integrated circuits: analysis and design", McGraw-Hill

Exercice 12.1a: 2-1 multiplexer

Déterminez la table de vérité de ce schéma et montrez que
la sortie «O» correspond à un 2-1 MUX («O»=A si S=1 et «O»=B si S=0)



S	A	B	$\overline{O}$	O	O
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			



Zimmermann, Fichtner, IEEE journal of
solid-state circuits, Vol. 32, No. 7, pp. 1-12.

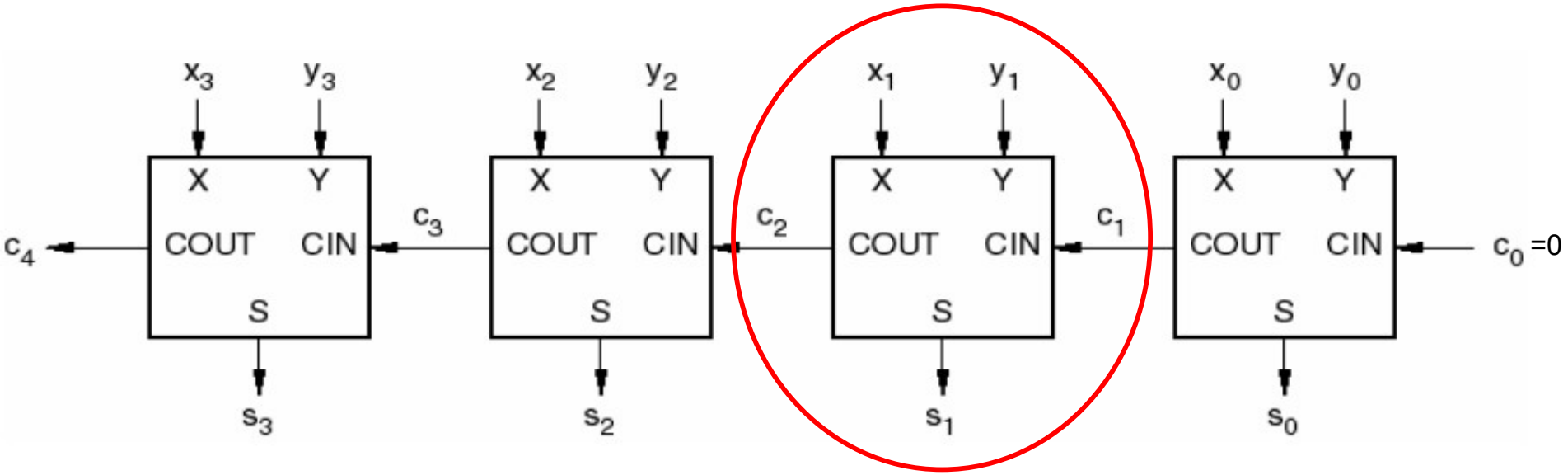
Exercice E12.2: Addition binaire

Principe

$$
\begin{array}{rl}
 & c_4\ c_3\ c_2\ c_1\ 0 \\
 & x_3\ x_2\ x_1\ x_0 \\
+ & y_3\ y_2\ y_1\ y_0 \\
\hline
= & c_4\ s_3\ s_2\ s_1\ s_0
\end{array}
$$

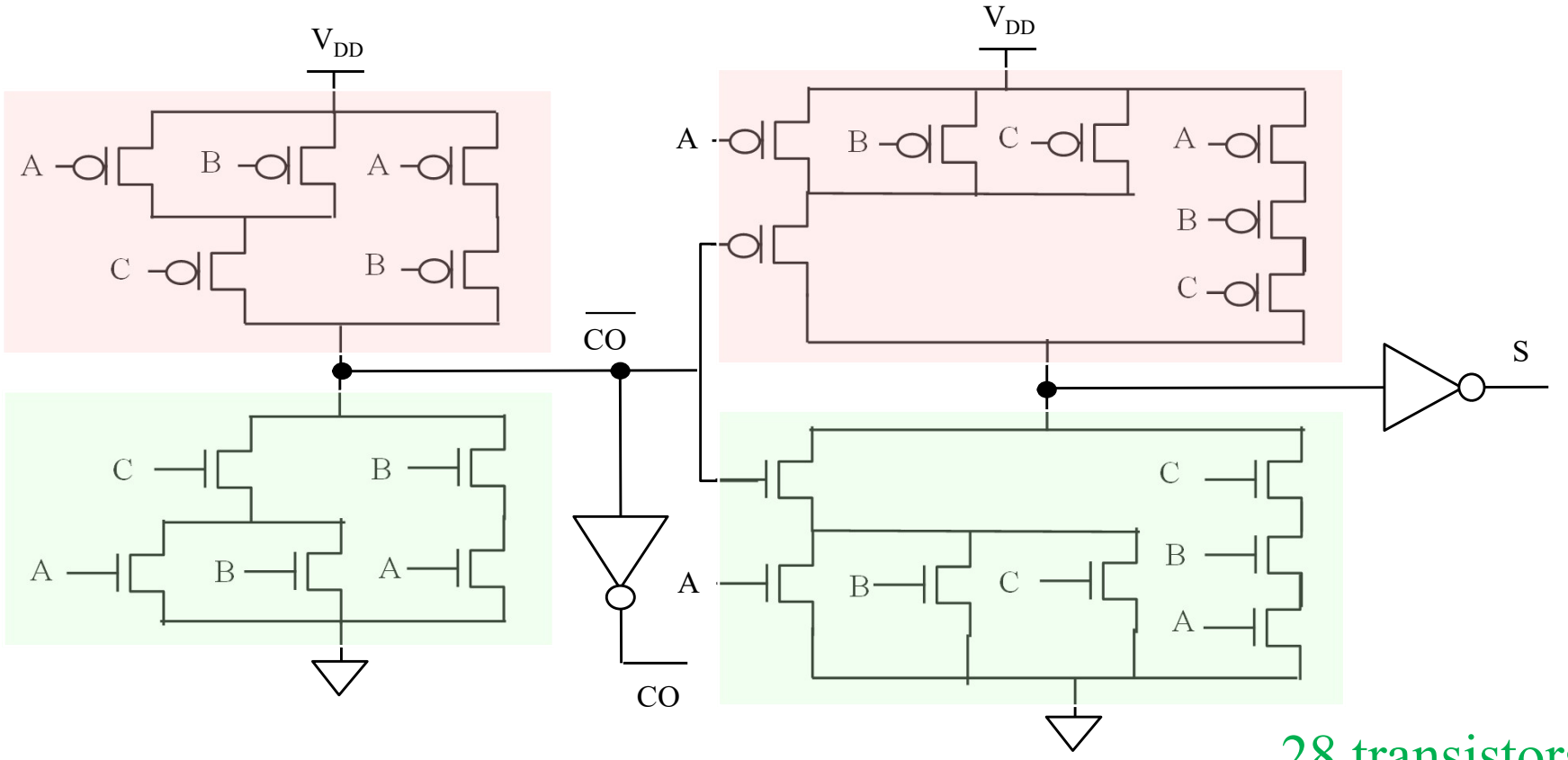
Exemple d'addition binaire:
1101 + 1001 = 10110

	1 0 0 1 0	C
	1 1 0 1	A
+	1 0 0 1	B
=	1 0 1 1 0	S



Exercice E12.2: « Full adder »

Calculez la table de vérité et montrez qu'elle correspond à une addition binaire

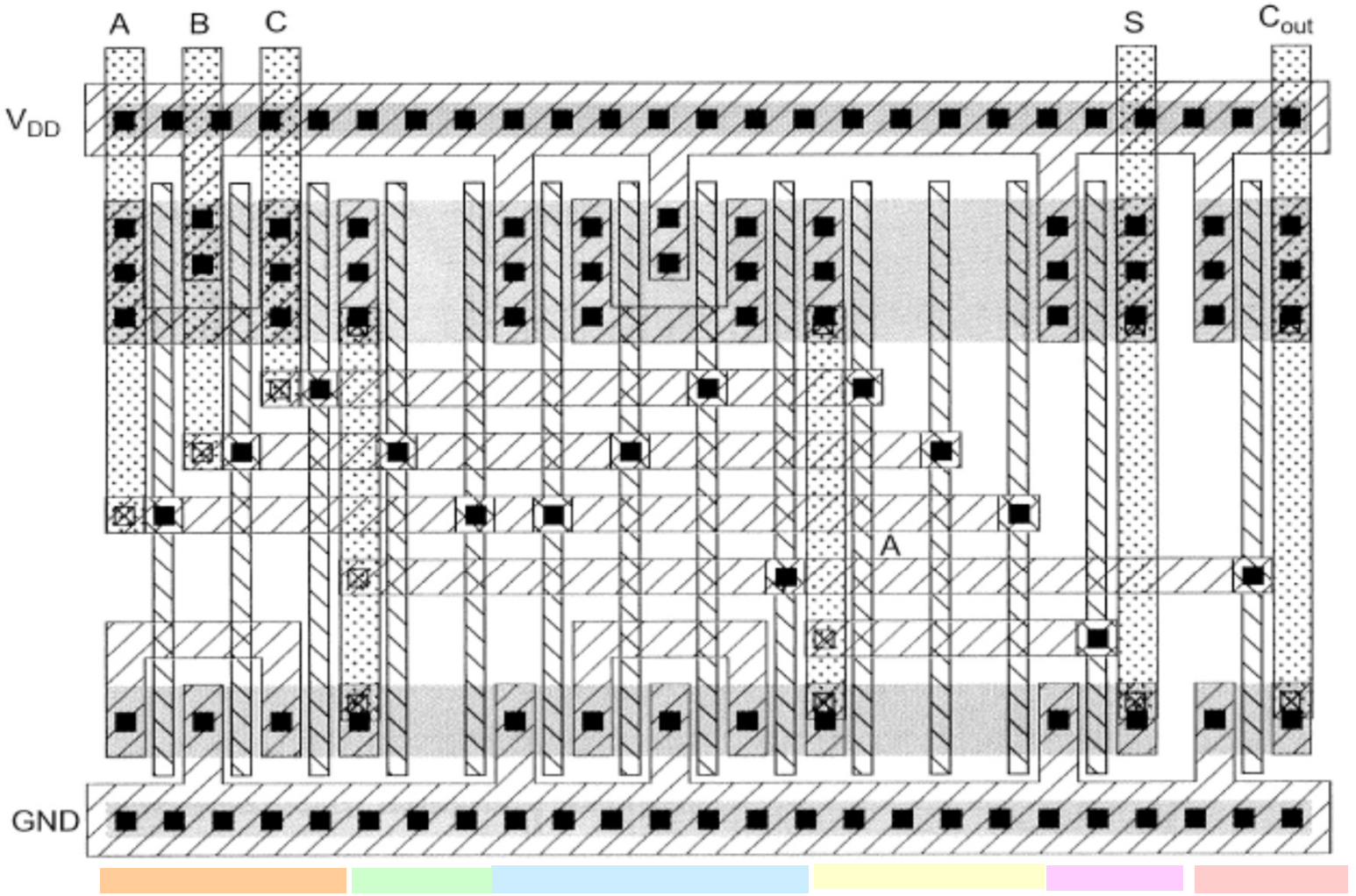


28 transistors

Zimmermann, Fichtner, IEEE journal of solid-state circuits, Vol. 32, No. 7, pp. 1-12.

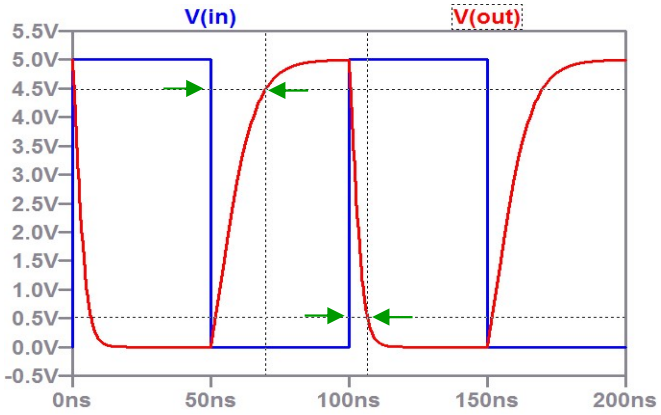
Layout du « full adder » de l'exercice E12.2

Weste/Harris, « CMOS VLSI design », Addison-Wesley

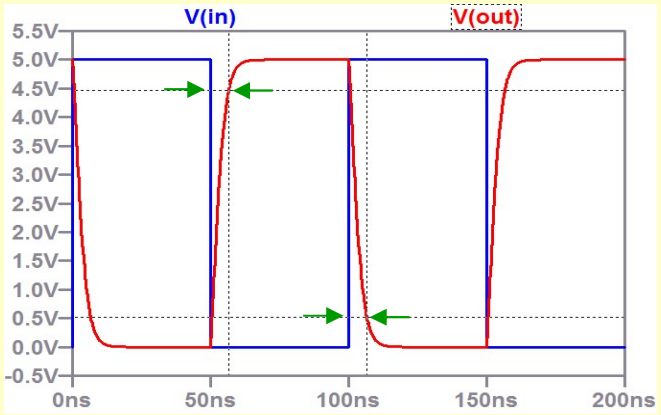


Exercice 12.3: dimensionnement (1)

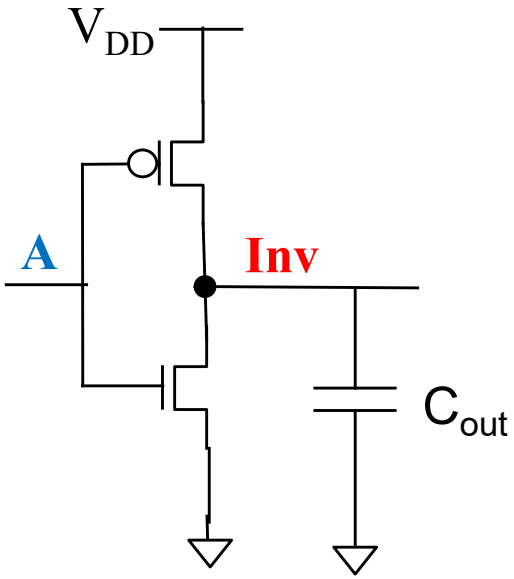
Wp=Wn

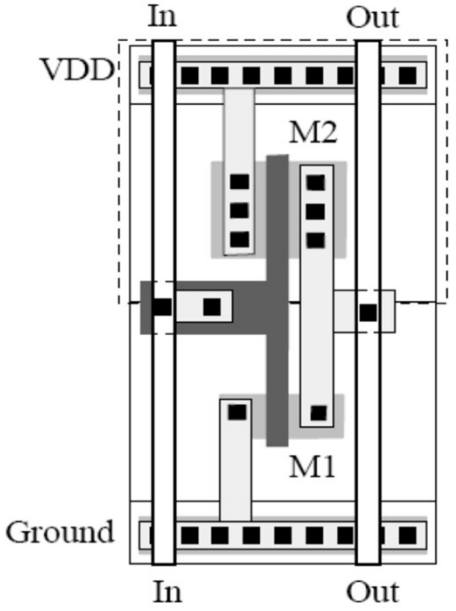


Wp= 3 Wn



Inverseur

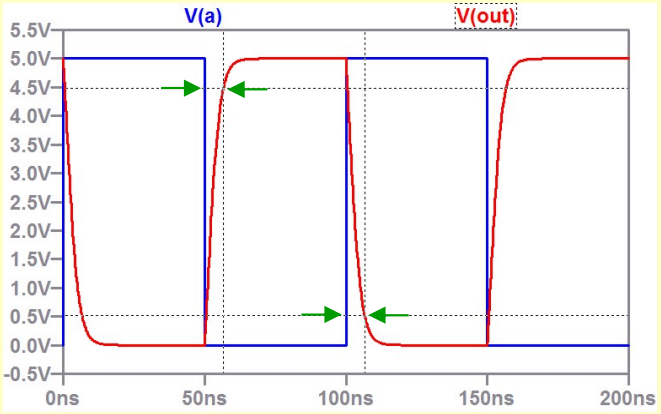




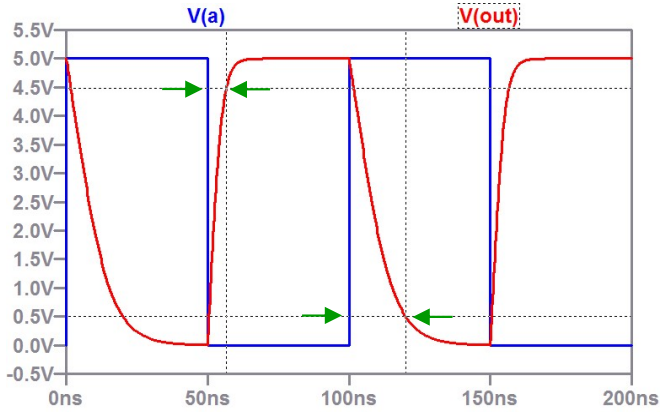
Wp= 3 Wn

Exercice 12.3: dimensionnement (2)

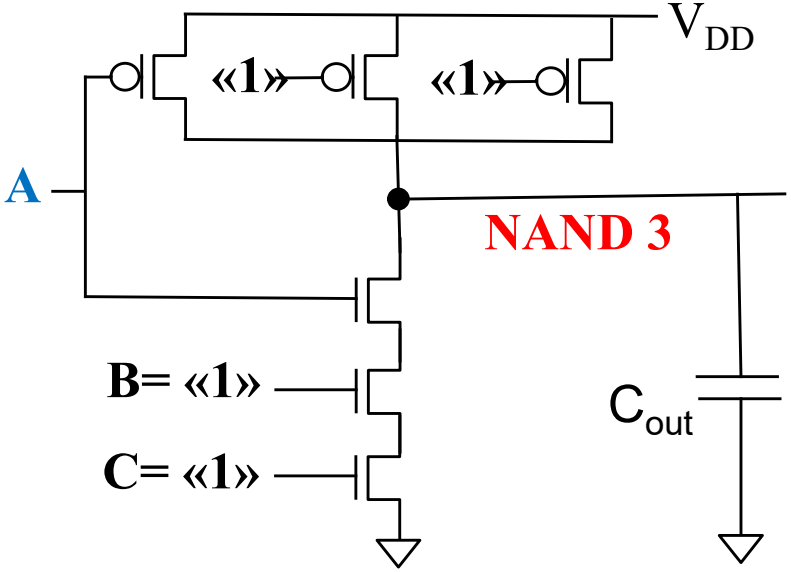
Wp= Wn

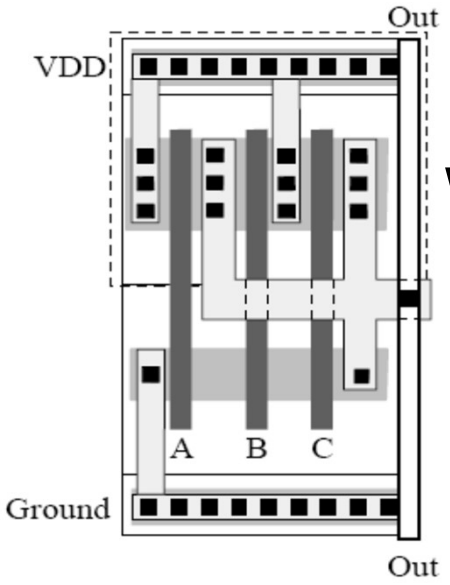


Wp= 3 Wn



NAND 3





Wp= 3 Wn

Littérature

[1] R.J. Baker, « CMOS, circuit design, layout and simulation »,
IEEE Press, 1998 and second edition 2005.

[2] Weste, Harris,« CMOS VLSI design, third edition », Addison-Wesley, 2005

[3] J.P. Uyemura, « introduction to VLSI circuits and systems »,
Wiley, 2002.

Autre:

[4] R. Zimmermann, W. Fichtner,« Low-power logic styles: CMOS versus pass-transistor logic » IEEE Journal of solid-state circuits, Vol. 32, No. 7, 1997, p. 1- 12.