EE-517: Bio-Nano-Chip Design

Solutions 11: Current-to-frequency converters, Amperometric detection, Temperature measurement

November 24, 2020

Problem 1

In amperometric detection, *Current-to-Frequency Converters* (I-to-F converters) are current-mode circuits used to transduce the faradaic current into a frequency-modulated signal that could be directly fed to processing circuits or relayed to transceivers. They present several advantages over voltage-mode circuits. They are more power and area-efficient, thanks to the elimination of amplifying circuitry and analog-to-digital converter, that are used in typical transimpedance current readout circuits. I-to-F converters are also less sensitive to matching and noise issues.

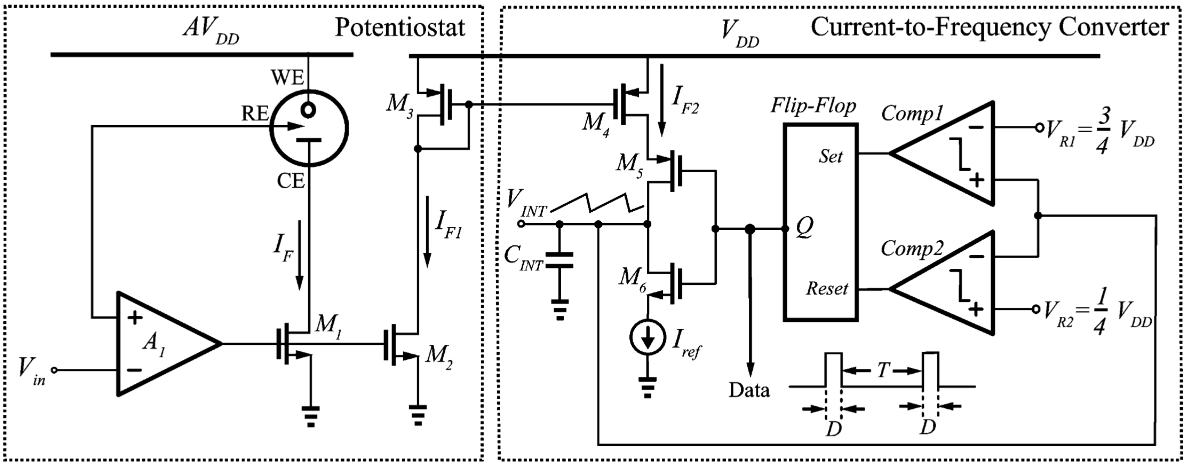

Figure 1: Simplified schematic of potentiostat and current-to-frequency conversion of oxidation currents.

(a) Fig. 1 is a simplified schematic of the circuit implemented at transistor level. Nevertheless, it highlights the main blocks constituting the potentiostat and the I-to-F converter.

- **Potentiostat:** A_1 is a single-stage amplifier. Together with transistor M_1, they constitute the control amplifier of the potentiostat, fixing the electrochemical cell potential to $AV_{dd}-V_{in}$ through the feedback loop, while measuring the faradaic current drawn by the cell. A current conveyor structure is adopted, where the faradaic current is conveyed from WE to a high impedance node (drain of M_1). The current I_F is mirrored at M_2, and is injected to the I-to-F converter. The current mirror formed by M_3 and M_4 is added to minimize the injection of the switching noise from the converter to the potentiostat.

- **I-to-F converter:** it comprises a sampling capacitor C_{INT}, two comparators and a flip-flop. I_F is encoded as a pulse signal as the following:

  during the sensing phase (Data=0): M_5 is on and M_6 is off. The mirrored faradaic current I_{f2} is integrated in C_{INT} until the voltage across the capacitor, V_{INT}, exceeds $V_{R1} = \frac{3}{4} \cdot V_{dd}$. Then, the comparator Comp1 sets the flip-flop.

  during the reset phase (Data=1): M_5 is off and M_6 is on. I_{ref} starts discharging C_{INT} until V_{INT} reaches $V_{R2} = \frac{1}{4} \cdot V_{dd}$. Then, the comparator Comp2 resets the flip-flop.

  V_{INT} is a sawtooth waveform, whereas Data is a low-duty-cycle pulse waveform of fixed pulsewidth D, and the time between two consecutive pulses, T, is inversely proportional to I_F,

$$D = \frac{V_{dd}C_{INT}}{2I_{ref}} \qquad T = \frac{V_{dd}C_{INT}}{2I_F}$$

Ivan Ny Hanitra: ivan.nyhanitra@epfl.ch

(b) The maximum resolvable frequency of the pulsed signal Data allows sizing the capacitor C_{INT}.

$$f = \frac{1}{D+T} = \frac{2}{V_{dd}C_{INT}} \cdot \frac{I_{ref}I_f}{I_{ref}+I_f} \leq f_{max}$$

Thus, $C_{INT} \geq 5.55\,pF$. $\mathbf{C_{INT} = 6\,pF}$ is taken.

(c) The circuit of Fig. 1 allows to measure oxidation currents only. In order to measure reduction currents, the potentiostat should be updated as in Fig. 2.

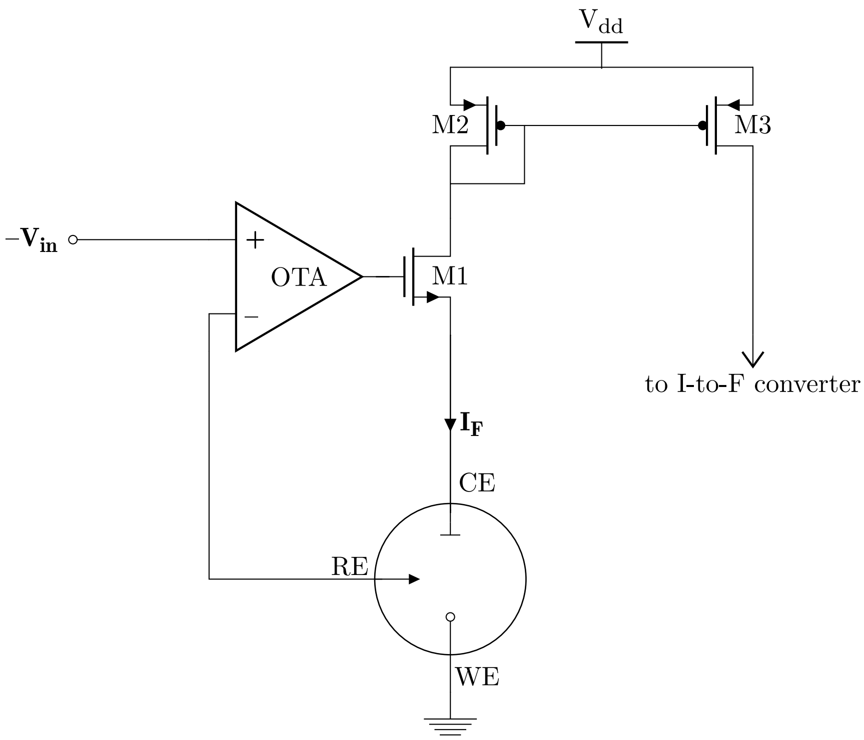

Figure 2: Potentiostat for reduction current readout.

Problem 2

A differential current measurement is performed between two electrodes, one functionalized with *Carbone Nanotube* (CNT) and cytochrome P450 3A4, and one with just CNT. A grounded-WE electrochemical cell with two *Transimpedance Amplifiers* (TIAs) is implemented. The TIA measuring the enzymatic reaction is multiplexed between the two sensing electrodes, for Cyclophosphamide and Dextromethorphan detection. The circuit is shown in Fig. 3. An unity-gain differential amplifier is added downstream to resolve the difference between V_2 and V_1, so that

$$\mathbf{V_{out} = R_{12} I_{1,2} - R_3 I_3}$$

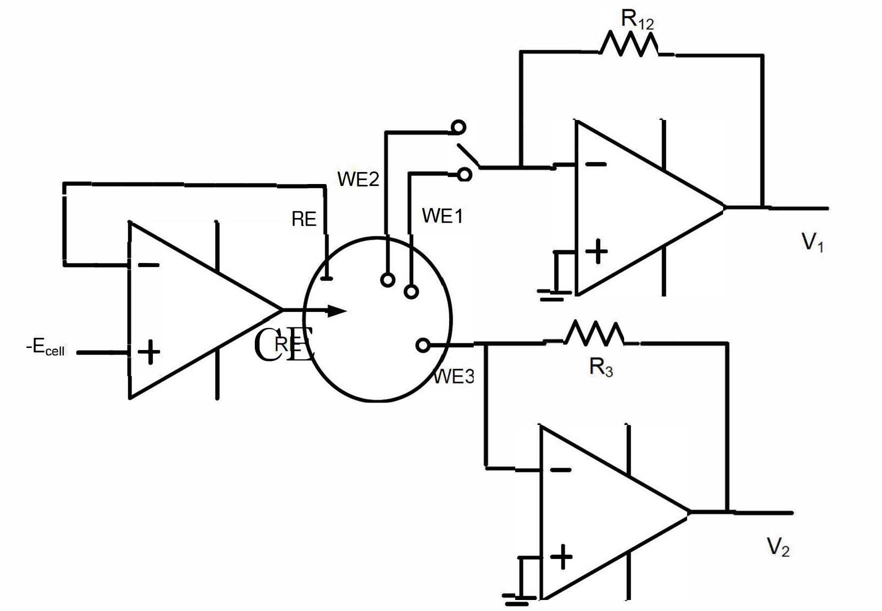

Figure 3: Multiplexed differential detection of Cyclophosphamide and Dextromethorphan.

To detect Cyclophosphamide with Cytochrome P450 3A4, we need to apply $E_{cell} = -296\,\text{mV}$ (book p.210). Likewise, Dextromethorphan detection is carried out by applyin $E_{cell} = -392\,\text{mV}$ (book p.210)

Problem 3

Temperature measurement is implemented with a *Proportional-to-Absolute Temperature* (PTAT) circuit. A beta-multiplier architecture is adopted. The circuit is displayed in Fig. 4.

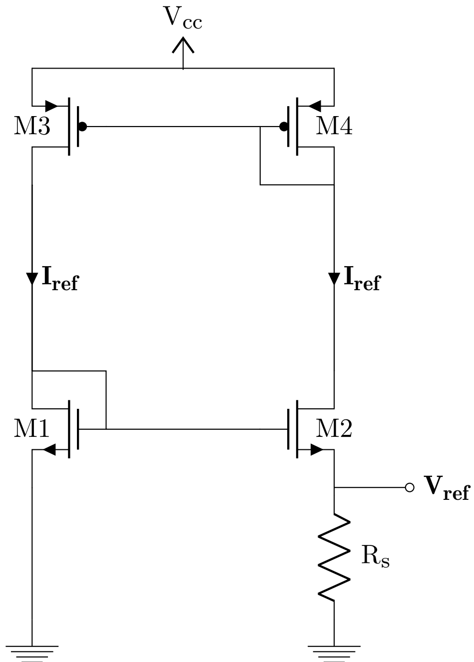

Figure 4: Beta-multiplier implemented for temperature measurement.

The MOS transistors are operating in weak inversion. The currents in the branches are

$$\begin{aligned} \text{M1}: \quad & I_{D1} = I_{S1} \exp\left(\frac{V_{g1} - V_t}{nU_t}\right) \\ \text{M2}: \quad & I_{D2} = I_{S2} \exp\left(\frac{V_{g2} - nV_{ref} - V_t}{nU_t}\right) \end{aligned}$$

where

- MOS transistor specific current: $I_S = 2\frac{W}{L}\mu C_{ox} n U_t^2$
- MOS threshold voltage: V_t
- MOS slope factor: n
- Thermal voltage: $U_t = \frac{k_B T}{q} = 26\,\text{mV}$ at 25 °C

Defining the ratio factor k between M1 and M2 as $\mathbf{I_{S2} = kI_{S1}}$, and considering that $I_{D1} = I_{ref}$ is mirrored in the second branch, $I_{D1} = I_{D2} = \frac{V_{ref}}{R_s}$, the final expression is

$$k = \exp\left(\frac{I_{ref} R_s}{U_t}\right) = 47$$

Eventually, $\mathbf{\frac{W}{L}\Big|_{M2} = 47\frac{W}{L}\Big|_{M1}}$, and $\mathbf{\frac{W}{L}\Big|_{M3} = \frac{W}{L}\Big|_{M4} = 2\frac{W}{L}\Big|_{M1}}$ is chosen, where the factor 2 accounts for charge carriers mobility compensation between nMOS and pMOS transistors.

Reference books

- **P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer**, *Analysis and Design of Analog Integrated Circuits (*5th *edition)*, Wiley, 2009
- **D. Stefanovic and M. Kayal**, *Structured Analog CMOS Design*, Springer, 2008