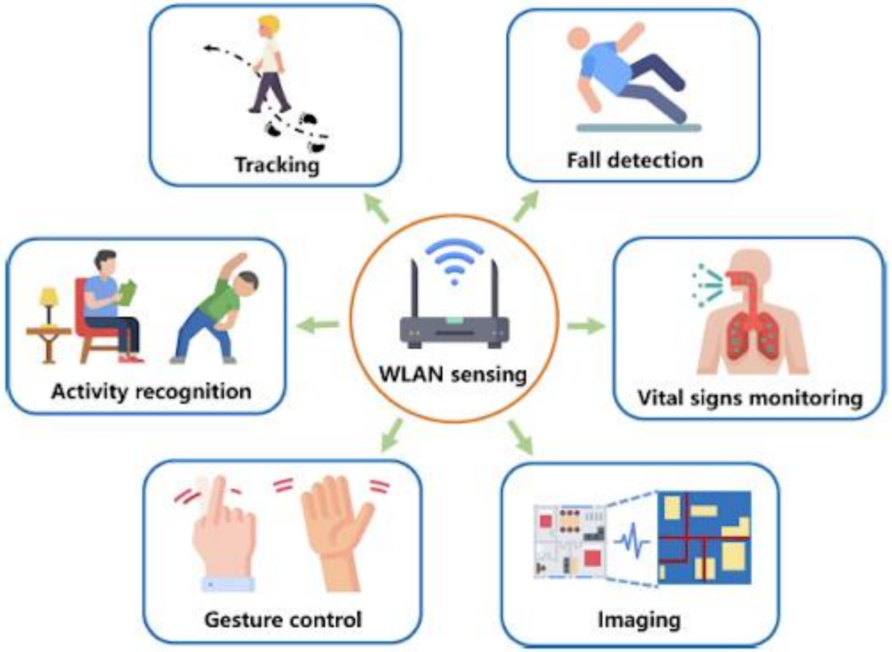
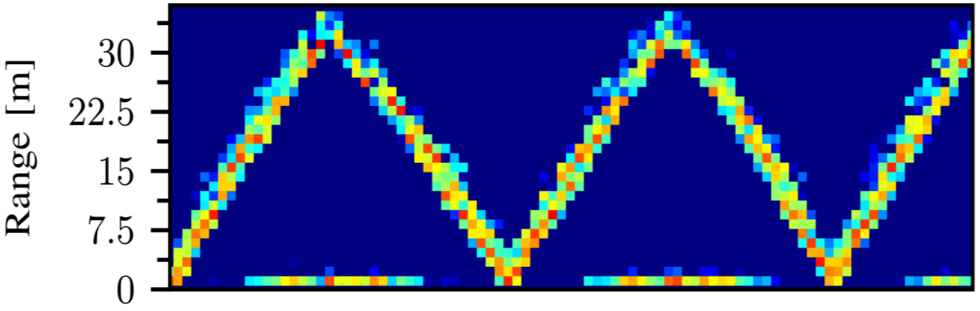
TCL Student Projects Spring 2025

VLSI / Digital Design Related Projects

Chip for Wi-Fi sensing

- **Motivation**
  - Current methods for activity detection, localization, and vital-sign estimation (breathing) require the use of cameras (intrusive) or wearables (restrictive)
  - Wireless-sensing systems can provide contactless, 24/7 detection supporting applications like home intrusion detection, tracking, activity recognition, vital-signs monitoring etc.
- **Objective**
  - Transition our current Wi-Fi sensing system (FPGA) to an ASIC (semi-custom)
  - Optimize for area, power and speed
- **Type of work:**
  - Circuit design and optimization using Cadence tools and a standard-cell based flow
  - Additional exploration with VHDL/Verilog





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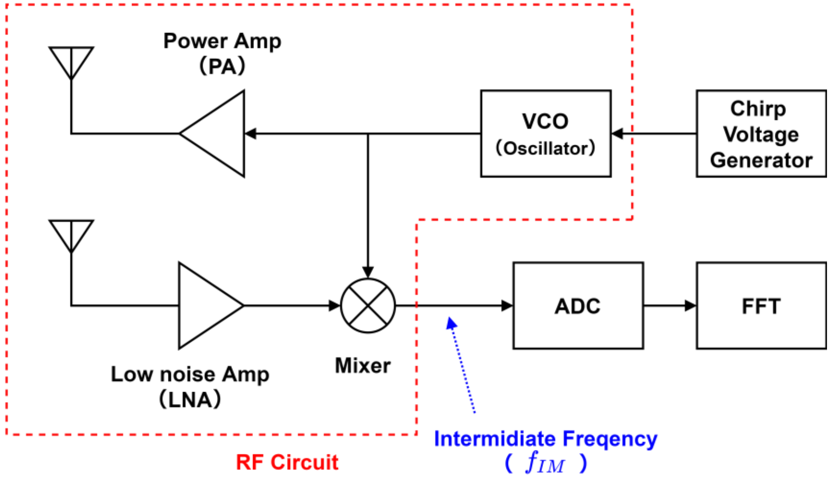
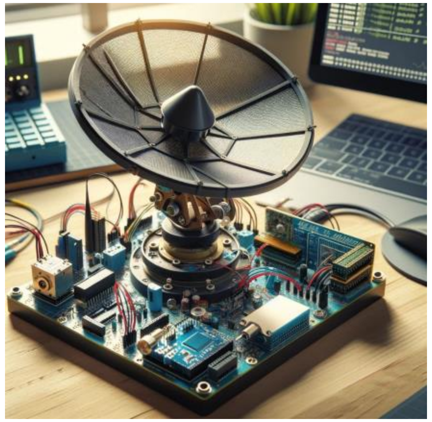
Drone Detection Radar Design

- **Motivation**
  - With the increasing use of drones in various sectors (e.g., delivery, surveillance), there is a growing need to detect unauthorized drones entering restricted airspaces
  - A radar system can provide early detection and tracking capabilities, allowing security teams to respond quickly to potential threats such as drone intrusions into airports, government buildings, or other sensitive locations
- **Objective**
  - Design an RF circuit on PCB to detect the speed and position of a drone
  - Model the behavior of the RF system for simulation and analysis
  - Digital processing will be performed on a Software Defined Radio (SDR) for real-time data acquisition and signal processing
- **Type of work:**
  - RF Circuit Design: PCB design (KiCad) and tests.
  - Signal Processing: Work with Python for system modeling and SDR for digital processing





AI Generated radar PCB

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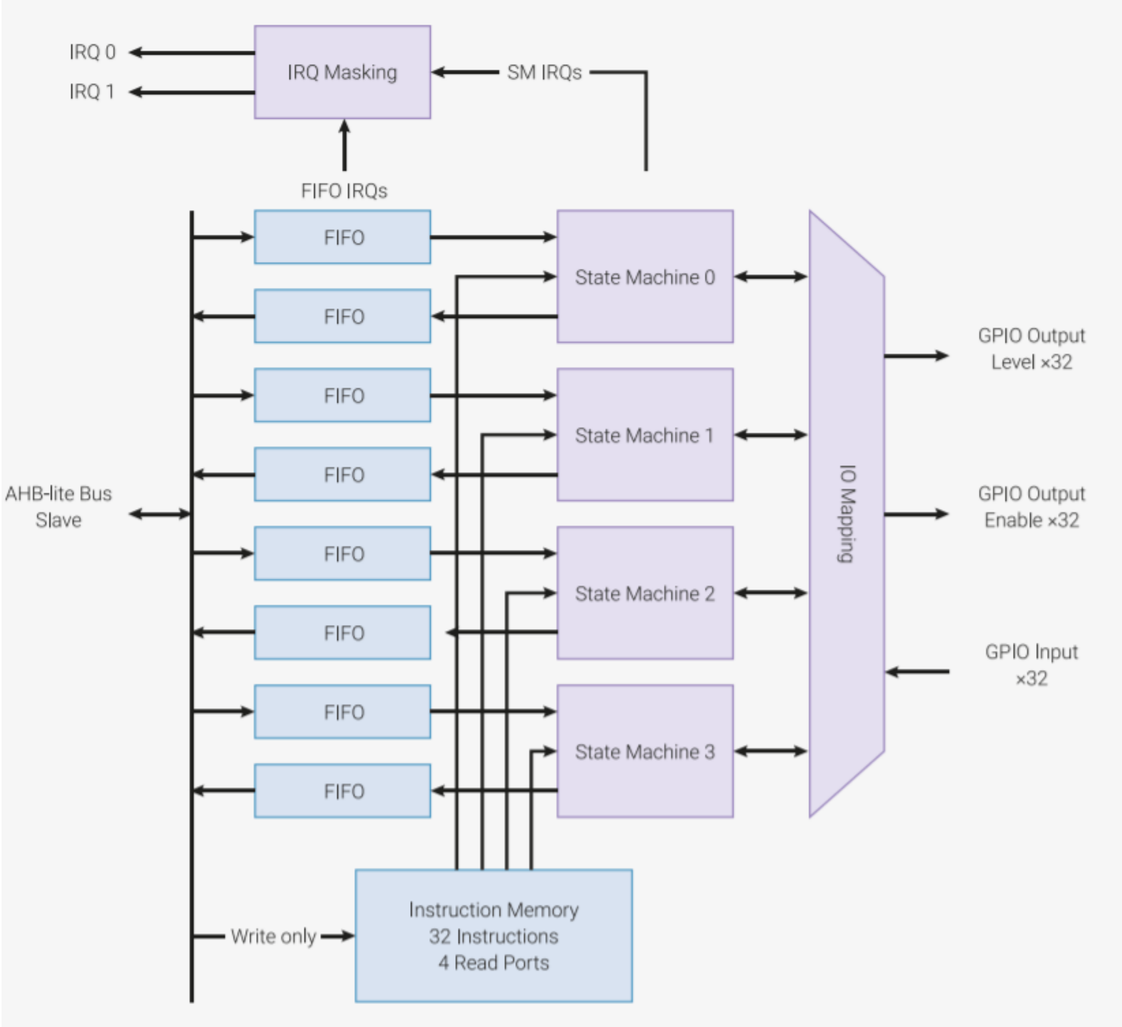
Open Reimplementation of the RP2040 PIO (Master Thesis)

- IO interface of Raspberry Pi RP2040
  - Simple state machines with 9 16-bit instructions
  - Highly Specialized for real time IO implementation of protocol like I2C, SPI, CAN, etc.
- Expected Outcome
  - RTL code reimplementing the functionality
- Tasks / Objectives:
  - Read the specifications, implement in RTL, and integrate into the HEEP System
- Type of work:
  - RTL implementation, FPGA prototyping
- Pre-requisites
  - Knowledge in an HDL (VHDL/Verilog)



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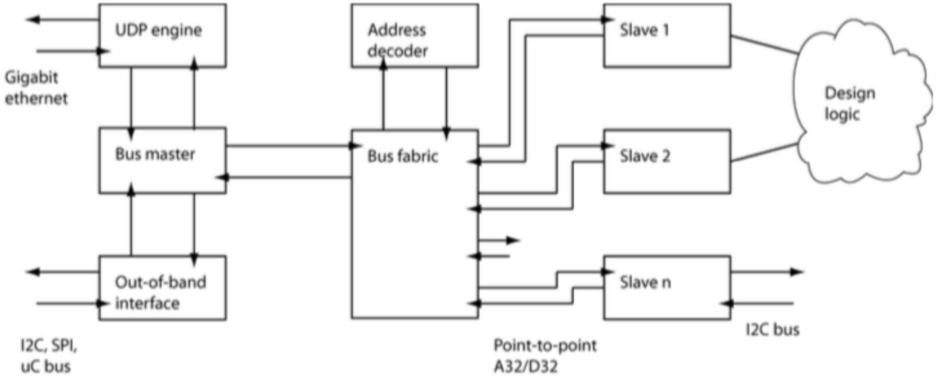
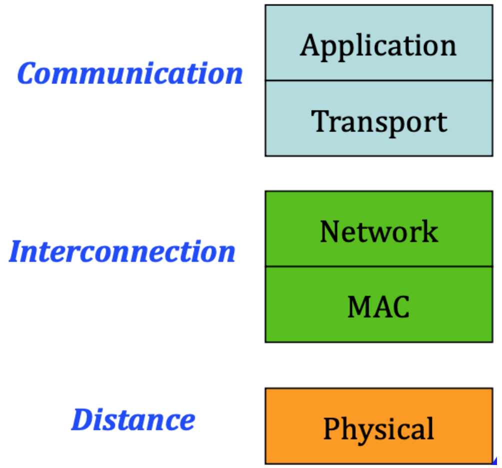
Integrating High-Speed Test Infrastructure into XHeep (Semester Project)

- Motivation
  - Methods to interact with custom ASICs (with no onboard CPU) relies on custom slow interfaces:
    - Reliable but outdated, with low bandwidth and poor compatibility with modern protocols
  - An Ethernet-based solution, combining IPbus and Verilog-Ethernet, has been implemented at TCL for high-speed testing of custom ASICs
- What is IPbus?
  - An open-source protocol developed by CERN for managing memory-mapped resources in hardware
  - Provides a packet-based communication system with built-in reliability features
  - High-speed operation: Optimized for efficient memory access
  - Complete support for the OSI stack from physical to application layer (with no CPU)
  - Comprehensive software tools: C firmware and Python wrappers for testing and control
  - Example Use: **Python → Ethernet → AXIbus** for direct communication with ASICs
- Objective
  - Integrate the IPbus-based high-speed test infrastructure into the XHeep project
- Prerequisits:
  - Knowledge in VHDL and in SV/Verilog
  - Basics in python





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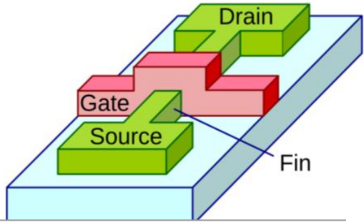
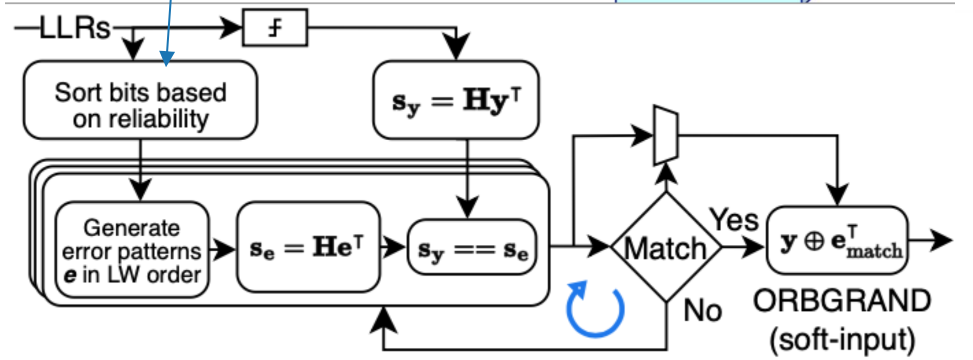
Analog High-Performance Sorters for Telecommunications

- Motivation
  - In telecommunications (5G/6G/800Gbps Fiber), algorithms must operate at unprecedented speeds.
  - A critical challenge: sorting large sets of elements to find the U smallest elements, crucial for communication systems
  - Current approaches rely on semi-custom designs (HDL, EDA tools), which often fail to achieve peak performance and minimum power consumption.
- Tasks/Objectives:
  - Evaluate architectural alternatives in a mixed-signal way
  - Optimize for area, power, and speed
  - Compare against purely digital implementations
- Type of work:
  - Circuit design and optimization using **Cadence tools in 16nm FinFet**
  - Additional exploration with **HDL** and **Python** for modeling and validation



Huge sorter network



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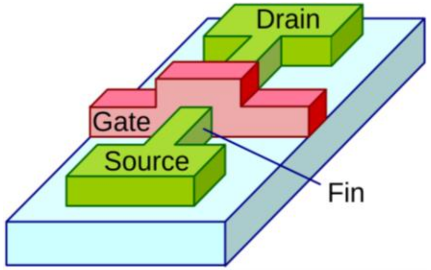
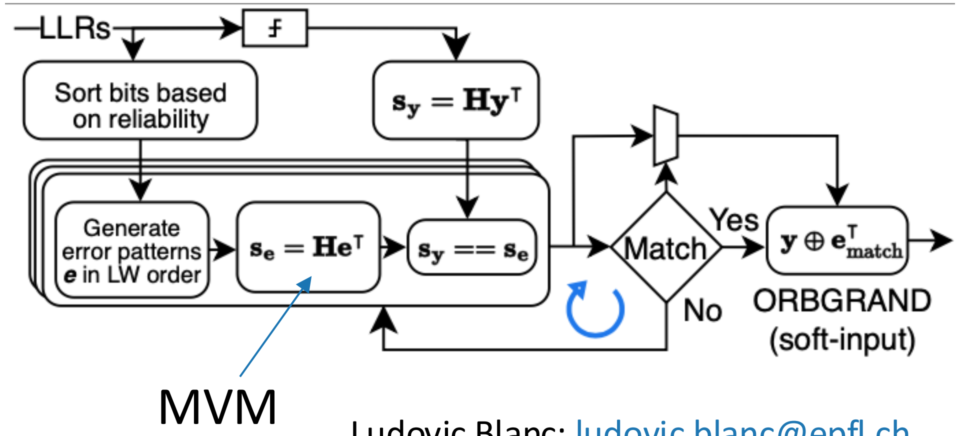
Efficient MVM for Syndrome Computation in Decoders

- **Motivation**
  - Matrix-vector multiplication (MVM) is emerging as a bottleneck in decoder implementations for modern communication systems
  - Current implementations use **standard-cell designs**, but a **full-custom approach** could bring significant improvements
  - Inspiration comes from **AI accelerators**, particularly **binary neural networks**, which use custom arrays for efficient computation
  - Unlike AI accelerators, our application:
    - Requires only **GF(2) (=modulo 2) summation** (no multi-bit analog outputs or reprogrammable weights)
    - Hardcoded weights, enabling a simpler, more efficient design



- **Tasks/Objective**
  - Design a Full-Custom MVM accelerator in 16nm FinFet
  - Compare the proposed design with standard-cell implementations in terms of efficiency and performance
- **Type of work**
  - Use Cadence tools for transistor-level circuit design
  - Python scripts to automatize the layout generation
  - HDL model of the MVM



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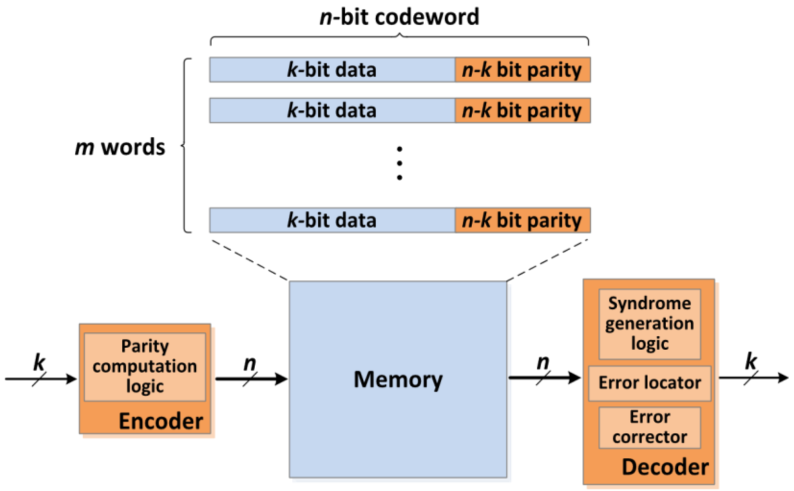
Multi-Bit Error Correction Code (ECC) for Gain-Cell eDRAM

- Background
  - Embedded DRAMs are much denser than SRAMs, but also easy to be affected by the retention time variation

  => Error correction codes for mitigating refresh-related failures
- Tasks/Objectives:
  - Explore how to achieve better tradeoff between parity bits storage overhead, latency, and system power
  - Design, verify and implement the chosen multi-bit ECC
- Type of work: Digital circuit design & ASIC implementation
- Prerequisites:
  - VHDL/Verilog
  - Python/C
  - Basic knowledge/interest of ECC and linear algebra is preferred



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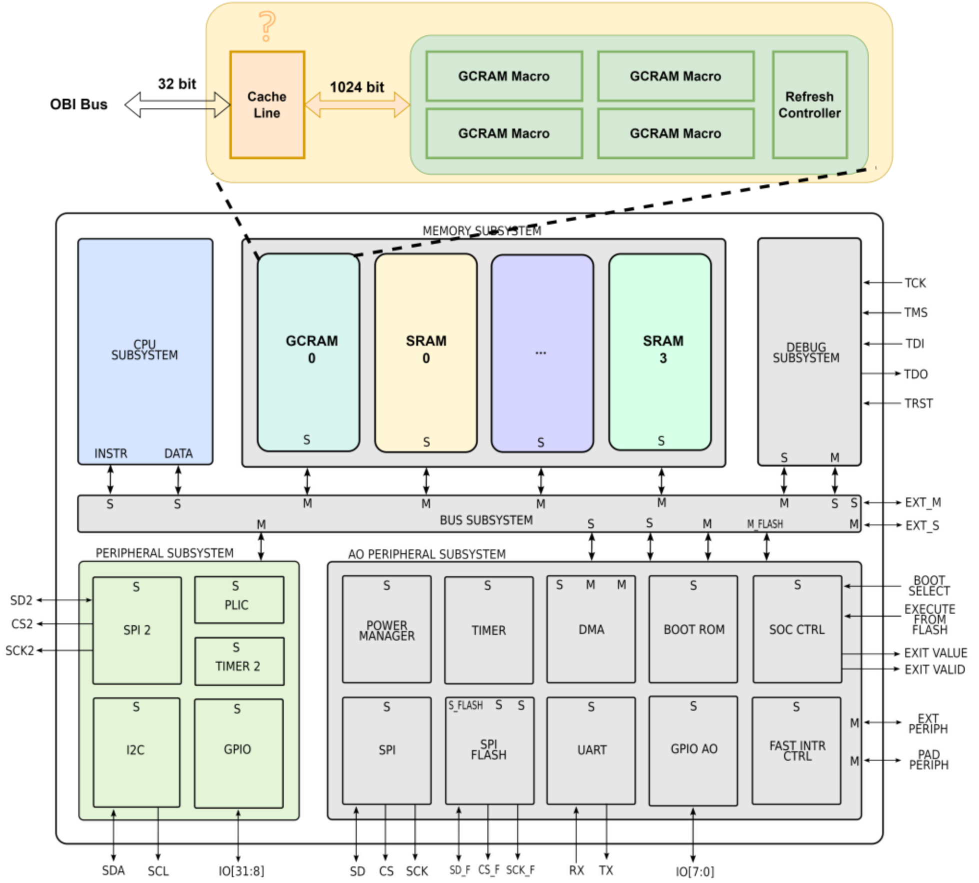
Optimize Gain-Cell eDRAM Performance on X-Heep Platform

- Background
  - GC-eDRAM has a larger line size (1024-bit) compared to data bus width (32-bit), read-modify-write and refresh operation increases memory access time

  => Add one or more cache lines as a buffer zone
- Tasks/Objectives:
  - Familiar with SoC architecture and be able to run benchmarks
  - Optimize the cache line structure to improve the performance
- Type of work: Software & hardware co-optimization
- Prerequisites:
  - VHDL/Verilog
  - C/Python
  - Basic knowledge of System on Chip (SoC) is preferred, like cache, system bus



X-HEEP

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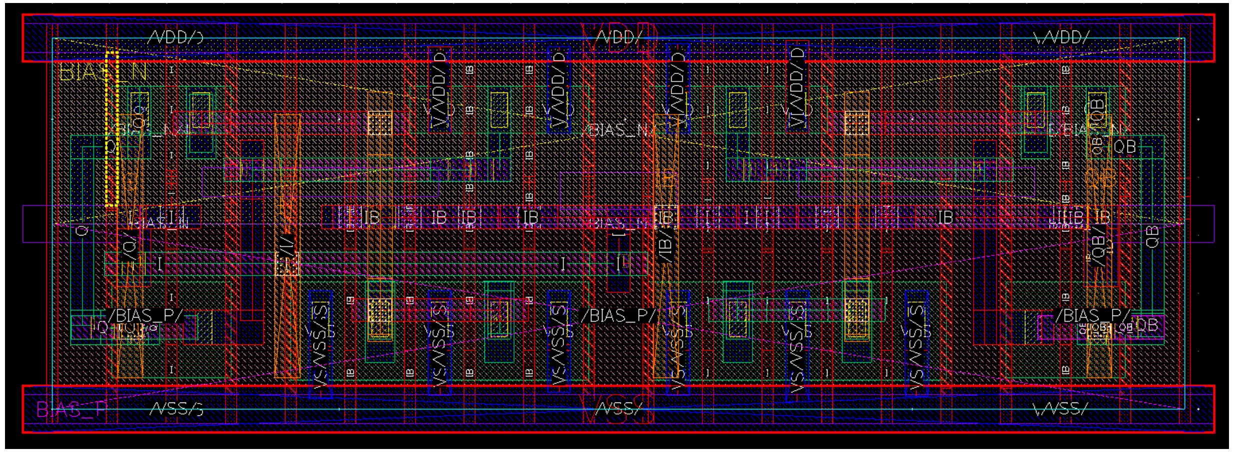
Ultra-low power standard-cells library optimization for AO systems

- Background
  - Always-on systems operate at reduced frequency (kHz range) and are dominated by leakage power consumption
  - Conventional CMOS are highly power hungry + require high design effort to lower their consumption (voltage scaling, clock-gating, reversed body biasing)
- Tasks/Objectives:
  - Optimize, Design and characterize a full-custom differential standard-cell library (DPTLSL) based on preliminary works for improved performance (robustness/leakage)
  - Comparison with a standard CMOS library
- Prerequisites:
  - Cadence Virtuoso (schematic/layout)
  - Monte Carlo/spice simulations
  - Python
  - Teamwork and git



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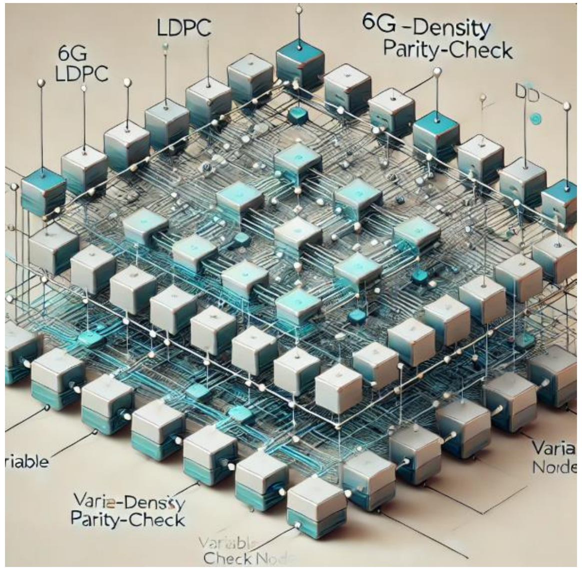
Design of A Matrix with Multiple Sizes and Its Decoder Implementation

- **Motivation**
  - Low-density parity-check (LDPC) are a standard in 5G-NR and hold significant promise for 6G applications
  - Length flexibility is necessary to match the varying wireless channel
  - An efficient decoder is expected to support multiple sizes flexibly
- **Tasks/Objective**
  - Given a base matrix, design a matrix with different lifting sizes (a small size should be nested in a large one)
  - Verify the designed matrix in a given configurable LDPC ASIC decoder
- **Type of work**
  - Matlab or C++ to analyze the matrix performance
  - VHDL/Verilog to test the designed matrix
  - Basic knowledge of layout design



GPT Generated 6G LDPC Decoder

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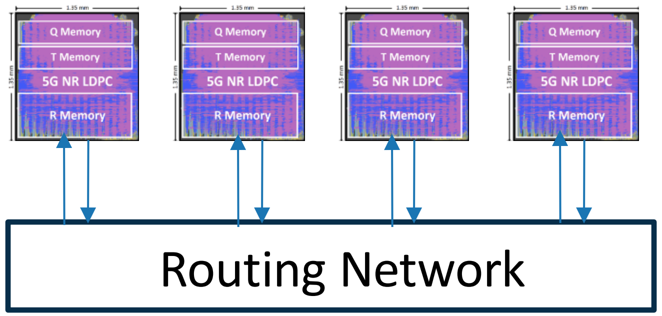
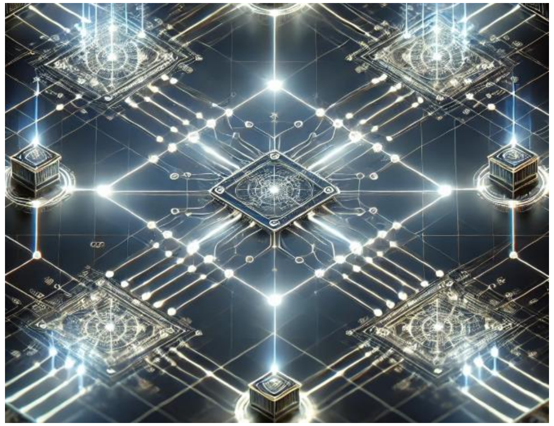
Routing Design for Data Coupling in Decoders

- **Motivation**
  - Multi-core is an efficient architecture to improve T/P in wireless
  - It also provides a chance to design a global coupling (GC) among each core to enhance the LDPC error-rate performance
  - A flexible routing that supports coupling in such a design is important
- **Tasks/Objective**
  - Simplify the routing design in the perspective of coding theory
  - Implement the designed flexible routing in ASIC
- **Type of work**
  - Matlab or C++ to analyze the routing performance
  - VHDL/Verilog to test the designed matrix
  - Basic knowledge of layout design





GPT Generated Routing Network in a multi-core design

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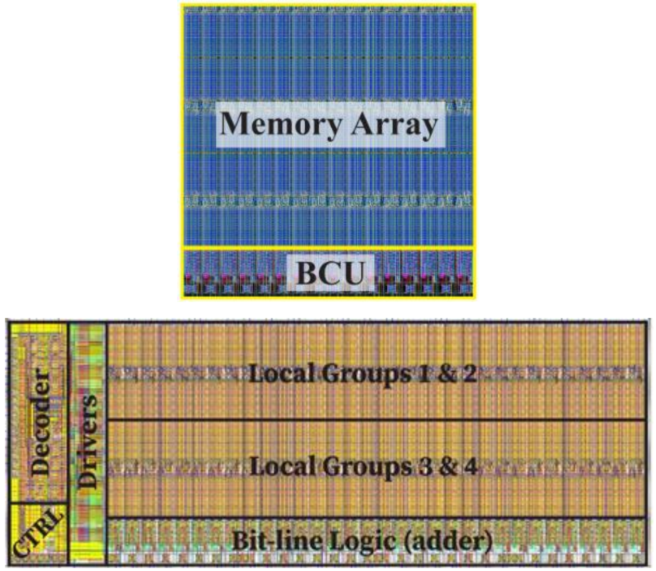
Elaboration of an In-Memory Computing Memory Compiler (Master Thesis)

- **Motivation**
  - In-memory computing shows promising gains for edge AI architectures
  - Designing memories is a complex task
  - Automating the generation of arbitrary memory sizes can enable huge gains
- **Tasks/Objective**
  - Design a IMC memory compiler in 65nm technology using open-source tools
    - port the flow for high density SRAM bitcells
  - End goal : from memory size and config, generate gds, lef, lib, spice files
  - Bonus : porting the flow for an open-source technology node and publication
- **Type of work**
  - Physical design, simulation, characterization, verification
  - Automation with scripts
- **Requirements**
  - Excellent understanding of Digital and full custom flows
  - Programming skills : Python, TCL, Spice, HDL
  - Comfortable with scripting and versioning tools (git)



Example of IMC memory macros manually designed

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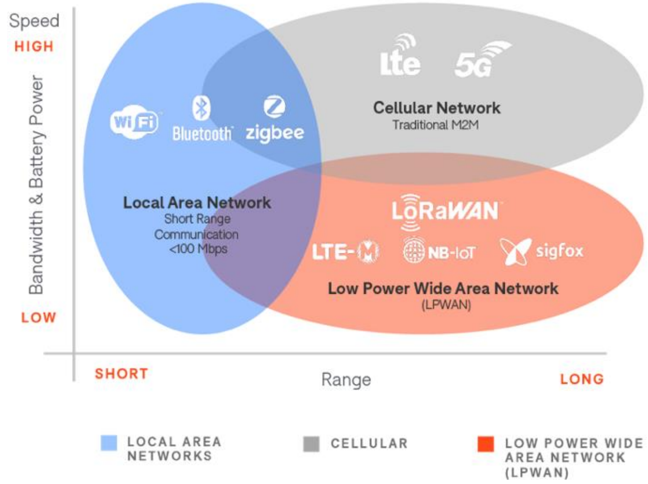
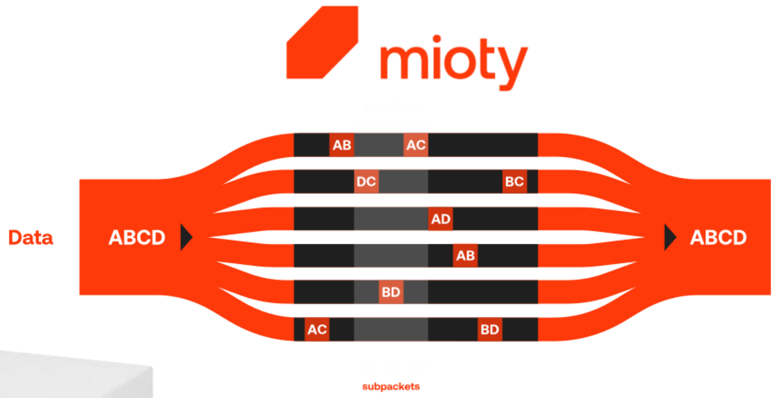
Telecommunications Related Projects

Mioty Implementation

- Topic
  - Mioty is a recent standard for low-power wide-area networks (LPWAN)
  - Although the specification is open-source, there currently is no implementation for software defined radio available
  - Previous student projects led to a first basic implementation
- Tasks/Objectives:
  - Improve synchronization of current implementation to achieve real-world communications
  - Build a transceiver compatible with commercial devices
- Type of work:
  - Coding (C++ and python)
  - Measurement of real transmissions
- Prerequisits: C++, basics of wireless communications





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Cellular Sensing: Traffic Safety Alert

- Background
  - Pedestrians distracted by phones are at risk on roads.
  - Use cellular sensing to alert pedestrians of fast-approaching vehicles.
- Tasks/Objectives:
  - Collect, extract and process real-time CSI data from cellular signals
  - Identify patterns indicating vehicle speed
  - Classify traffic as safe or dangerous using CSI data
- Type of work:
  - Data collection, Signal processing, Algorithm design
- Prerequisits: Python/C++, basics of wireless communications

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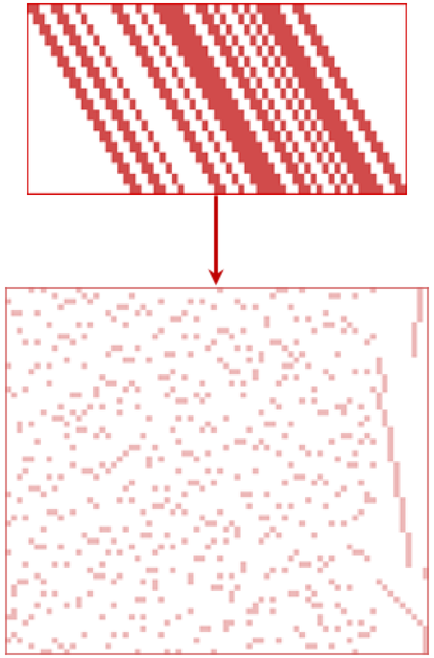
Improved Belief Propagation Decoding for Short Codes

- Topic
  - Belief propagation (BP) algorithm is widely used in channel coding, signal processing, and artificial intelligence
  - Though BP decoding is successful for long codes, direct BP decoding has very poor performance for short codes
  - Recently, we found that BP decoding for short codes can be significantly improved by sparsifying the parity-check matrix, which will be a promising decoding solution to 6G uRLLC scenarios
- Tasks/Objectives:
  - Improve the quality of the transformed sparse matrix for a specific code with the help of machine learning
  - Construct good short linear codes tailored to the sparse BP decoding
- Type of work (Recommended in a group >= 2 students)
  - Algorithm design
  - Coding (Matlab, C++ and Python)
- Prerequisites: Linear Algebra, machine learning, basics of coding theory



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Passive Orbit Determination based on Satellite Emitted Signals

- **Context:**
  - Orbit determination is a complex process that often requires observations from many sensors for a long period of time.
  - It is possible to leverage the Doppler shift in the link from satellite to ground station to perform orbit determination.

- **Objectives:**
  - Implement, and test an algorithm to perform early orbit determination on real satellites.
  - Build one or several ground stations.
  - Exploit signal strength and Doppler shift.
  - Suggested study case: Iridium satellites.

- **Ressources:**
  - SDR, USRP, RF components, antennae.
  - Accurate US Space Command satellite ephemeris.

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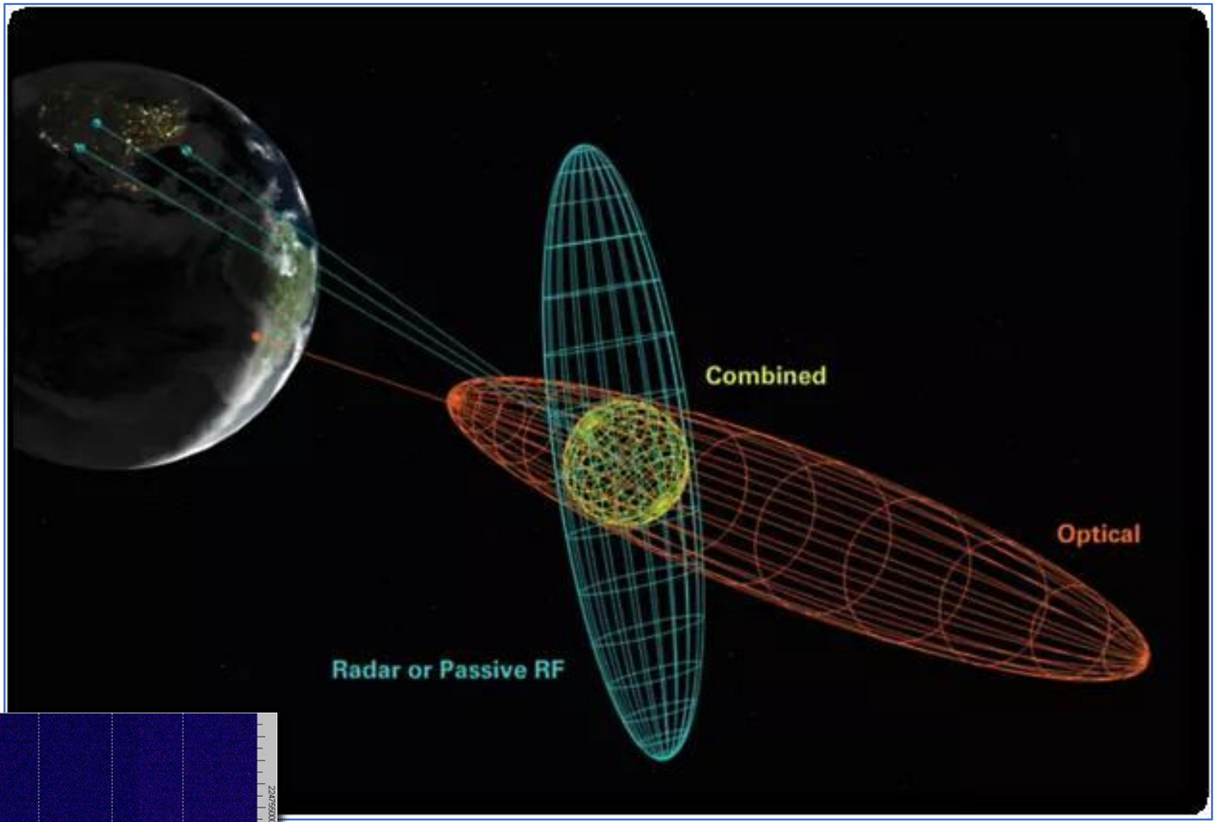
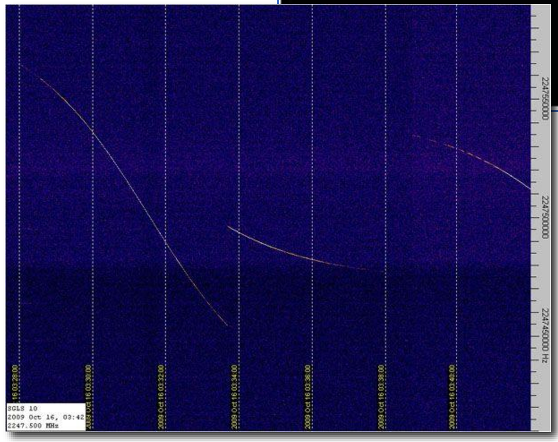
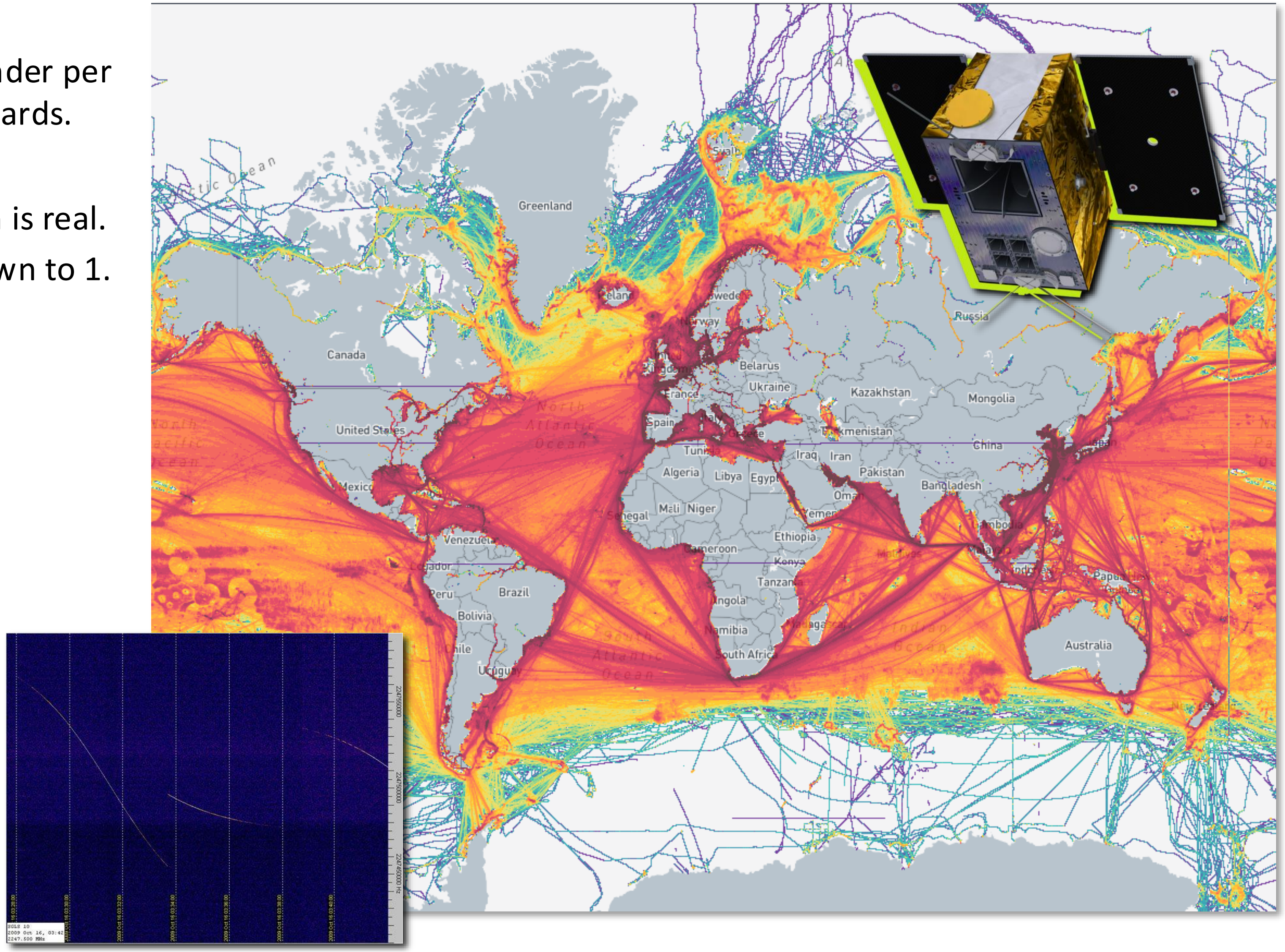




Localization of ships from space using a single satellite

- **Context:**
  - AIS (Automatic Identification System) = 1 transponder per ship to send location every 10 seconds to coast guards.
  - AIS can be received from space.
  - Localize signal position -> proof if claimed location is real.
  - Often made with 3 satellites -> we want to get down to 1.
- **Objectives:**
  - Implement and test Doppler based single satellite geolocation of AIS signals.
  - Enhance existing algorithm of the TCL.
  - Collaborate with satellite operator to perform acquisitions.
- **Ressources:**
  - Real satellite signal acquisitions on demand.
  - Accurate US Space Command satellite ephemeris.



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Thank you for your attention!