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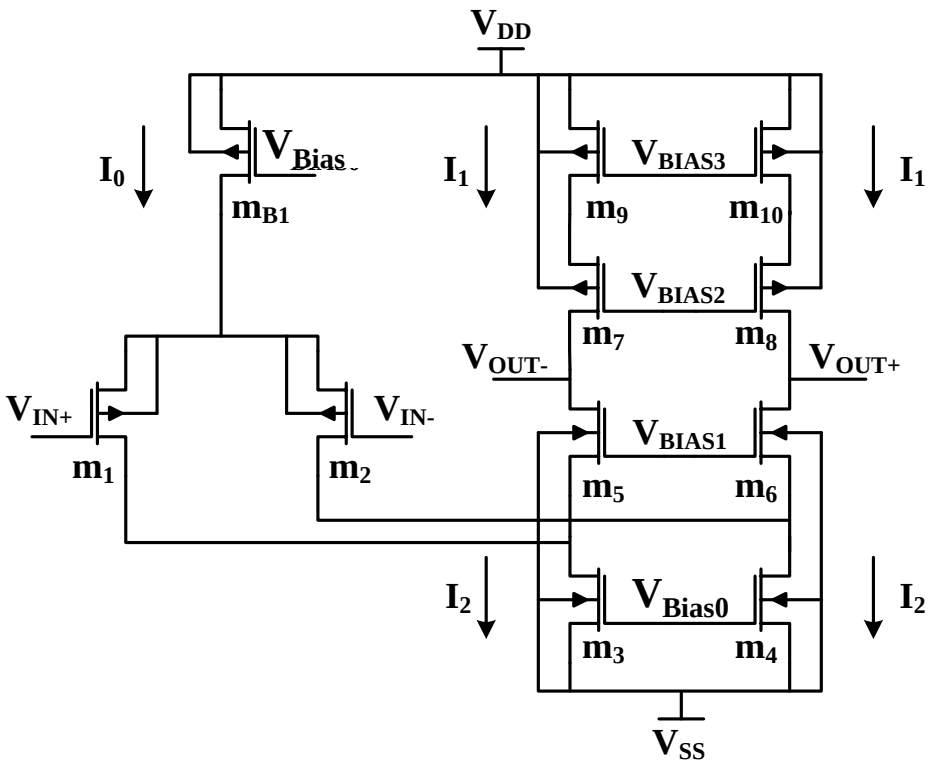
1. Fully differential folded cascode OTA: Procedural sizing

The purpose of this section is to provide the sizing procedure of the following OTA step-by-step. Starting by choosing circuit-level parameters (specifications) and propagating them to transistor level.



The technology used is CMOS 80nm 1.8V devices and their parameters are:

Parameter		Unit Extracted	
K_p	PMOS	40	$\mu A/V^2$
	NMOS	208	
U_a	PMOS	16	V/µm
	NMOS	5	
n	PMOS	1.3	-
	NMOS	1.2	
C_{ox}		8.3	$fF/\mu m^2$

The OTA, have to meet the following specifications.

Parameter	Value Specification		Unit
Open-loop gain	> 70		dB
GBW	60		MHz
Slew rate [**SR**]	50		V/µs
Load capacitors [C_L]	100		fF

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1.1. Bias currents

	Parameter	Expression	Value	Unit	Guideline
Bias	I_0			µA	
	I_1	$\mathbf{1,2 \times \frac{I_o}{2}}$		µA	

1.2. Differential pair

Determine the transconductance, inversion factor and W/L ratio of the differential pair.

	Parameter	Expression	Value	Unit	Guideline
Differential pair	$g_{m1,2}$			μS	
	$I_{f1,2}$			-	
	$\frac{W_{1,2}}{L_{1,2}}$			-	

1.3. Folded cascade load

The 8 transistors composing the folded cascode stage will now be sized.
Determine the inversion factor and W/L ratio of these transistors to:

- Keep all saturation voltages of $m_{9,10}$, $m_{7,8}$, $m_{5,6}$ small
- Minimize the noise and offset contribution of m_3 and m_4
- For simplification, only two values will be chosen for the inversion factor: **I_F= 10 or I_F = 1**.

	Parameter	Expression	Value	Unit	Guideline
Folded	$\frac{W_5}{L_5}$				
	$\frac{W_7}{L_7}$				

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	$\frac{W_9}{L_9}$				
	$\frac{W_3}{L_3}$				

Calculate the output resistance necessary to meet the open-loop gain specification.

	Parameter	Expression	Value	Unit	Guideline
Rout	R_{out}			MΩ	

Neglecting the conductance of the differential pair (assume $g_{ds1} \approx 0.5 g_{ds3}$), determine the conductance and length of all transistors so that:

- The specified open-loop gain is achieved
- The NMOS and PMOS resistances at the output node are balanced ($R_{up} = R_{down}$)
- The total area of the folded cascade stage is minimized (in the order of 85μm^2)
  - m_7 and m_9 have the same length
  - The length of m_3 is two times the one of m_5

	Parameter	Expression	Value	Unit	Guideline
Rout	$n_{n,p} \times g_{m5,7}$			μS	
	R_{up}			MΩ	
	$L_7 \times L_9$			μm^2	
	L_9			nm	$L_7 = L_9$
	L_7			nm	$L_7 = L_9$
	R_{down}			MΩ	

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	$L_3 \times L_5$			μm^2	
	L_5			µm	$L_3 = 2L_5$
	L_3			µm	$L_3 = 2L_5$

Calculate the width of all transistors.

	Parameter	Expression	Value	Unit	Guideline
Rout	W_3	$\boldsymbol{\frac{W_3}{L_3} \times L_3}$		µm	
	W_5	$\boldsymbol{\frac{W_5}{L_5} \times L_5}$		µm	
	W_7	$\boldsymbol{\frac{W_7}{L_7} \times L_7}$		µm	
	W_9	$\boldsymbol{\frac{W_9}{L_9} \times L_9}$		µm	

1.4. Differential pair finalization & Current source

Find the length and the width of the differential pair.

Parameter	Expression	Value	Unit	Guideline
L_1			nm	$g_{ds1} \leq 0.5 g_{ds3}$
W_1			µm	

Parameter	Expression	Value	Unit	Guideline
L_{B1}			nm	
W_{B1}			µm	

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1.5 Offset Estimation:

In case of the above folded cascade, give the expression of the input referred offset that include the contribution of Differential pair: $m_{1,2}$; Folded cascode: $m_{3,4}$ and Active load: $m_{9,10}$

$\sigma_{Vos}^2 =$

$$\sigma_{I_D(\beta,V_{T0})}^2 = \sigma_\beta^2\left(\frac{\partial I_D}{\partial \beta}\right)^2 + \sigma_{V_{T0}}^2\left(\frac{\partial I_D}{\partial V_{T0}}\right)^2$$

Theoretical reminder: $\sigma_{V_G}^2 = \frac{\sigma_{I_D}^2}{g_m^2}$

$$= \sigma_\beta^2\left(\frac{I_D}{\beta}\right)^2 + \sigma_{V_{T0}}^2 (g_m)^2$$

1.6 Common-mode feedback CMFB

Propose a CMFB circuit that use two differential pairs to tune the gate voltage of MB1 and set the common-mode output voltage to $V_{DD}/2$. Show how this CMFB circuit is connected to the fully differential cascode OTA (i.e. give the name of its input and output nodes):

CMFB schematic:

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1.7 Propose and size an optimal biasing circuit for $V_{Bias0-3}$