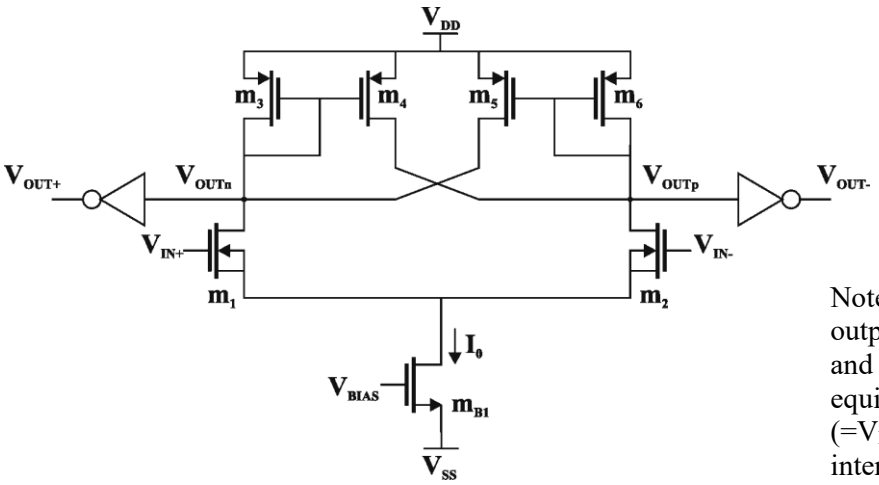
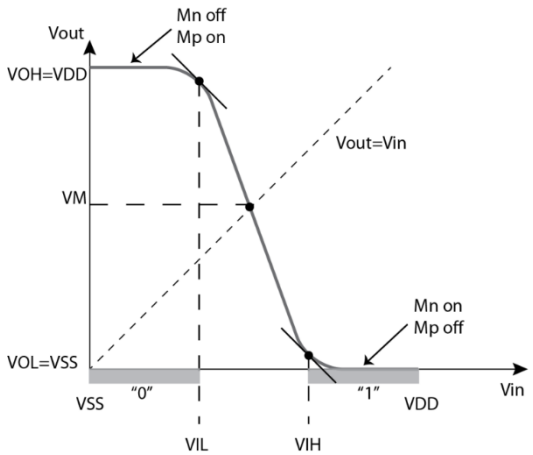
Parameter		Value Extracted	Unit	
K_p	PMOS	90	$\mu A/V^2$	V_{DD}= 1.2 V V_{ss} = 0V
	NMOS	220		
U_a	PMOS	10	V/µm	
	NMOS	14		
	V_{T0}	0.4	V	
n	PMOS	1.25	-	
	NMOS	1.2		
C_{ox}		13	$fF/\mu m^2$	
C_{ov}		0.2	fF/µm	

1. Analyse the functionality of a comparator

Comparator with the internal positive feedback



Note the inverters are added at the output in order to ensure positive and negative saturation voltages equivalent to the logical one (=V_{DD}) and the logical zero (=V_{SS}) interpretable by digital circuits.



Describe in your own words how this comparator works taking into account the inverter transfer characteristics reported here and supposing a positive feedback factor k=1.

VOH	1.2 V
VOL	0 V
VM	0.6 V
VIH	~ 0.7 V
VIL	~ 0.5 V

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2. Size the comparator

- Creat the schematic of the comparator and name it **COMP_FD**
- Set the initial transistor sizes in order to minimize the parasitic capacitances by following the points listed below and explain briefly your calculations.
- The bias transistor m_{B1} has to be sized to provide the differential pair tail current $I_0 = 4\ \mu A$.
- Choose the positive feedback factor k = 1;

Set the size positive feedback transistors with minimum size W=L= L_{min} = 65nm;

- Size the differential pair transistors to operate in strong inversion ($I_F = 10$) and $L = 2L_{min}$.
- Size the inverter with minimum size and to have $V_M = V_{DD}/2$

Check and save the schematic.

Transistor	W [µm]	L [µm]
$M_{1,2}$		
$M_{3,6}$		
$M_{4,7}$		
M_{B1}		

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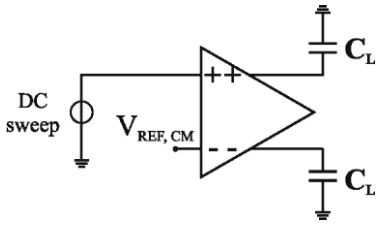
3. Perform the DC analysis

Testbench_COMP_DC



The reference voltage connected to the negative input is equal to 0.6V.
The load capacitances correspond to the input parasitic capacitances of a D flip-flop, C_L = 2fF.

- Create the **Testbench_COMP_DC** cell.
- Choose **DC Analysis** and set the simulation parameters to sweep Vin+ from 0 to V_{DD}.
- In order to plot the transfer curves, use the **vs** button and then choose in the schematic the corresponding node.

Note: The schematic has hierarchy, to visualize the transistors of the comparator you have to select the COMP_FD symbol in the schematic and descend into the transistor level view:

1 - First run

Perform the DC analysis for the initial transistor sizes. Descend to schematic view of the **COMP** cell and plot the following voltages: **vs (OUTn), vs (OUTp), vs (OUT+), vs (OUT-).**

If the comparator **does not switch the state**. Explain why:

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2 - Second run: Same current, different sizes

If necessary, resize the positive feedback transistors, keeping I_0 = 4 µA and k=1, in order to correctly switch the states.

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(W/L) = _____ $W_3 = W_4 = W_5 = W_6$ = _____ µm, $L_3 = L_4 = L_5 = L_6$ = _____ µm

Enter new sizes and repeat the simulation.
Choose the positive (OUTp) or negative (OUTn) output to measure the positive and negative saturation voltage at the input of the inverter:

V_{SAT+} = _____ V, V_{SAT-} = _____ V

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3 - Third run: Same sizes, different current

If necessary, resize the bias transistor m_{B1}, keeping the minimal dimensions of feedback transistors, in order to correctly switch the states**.**

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$(I_0)_{min}$ = _____ µA W_{mB1} = _____ µm, L_{mB1} = _____ µm

Enter new sizes and repeat the simulation.
Choose the positive (OUTp) or negative (OUTn) output to measure the positive and negative saturation voltage at the input of the inverter:

V_{SAT+} = _____ V, V_{SAT-} = _____ V

- **Determine analytically**

Set the positive feedback transistors to minimal dimensions.

Size the bias transistor m_{B1} to provide the differential pair tail current I_0 = 10 µA. Then size the differential pair transistors to operate in strong, moderate and weak inversion. (L = L_{min})

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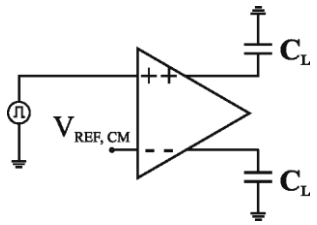
$I_{F\ diff\ pair}$	W/L diff pair	W diff pair
20		µm
10		µm
1		µm
0.1		µm

- **Perform the transient analysis**

Testbench_COMP_TRAN



- Create the **Testbench_COMP_TRAN** cell.
- Choose Transient Analysis and set the simulation parameters.
- Run the simulation.
- In order to plot the transfer curves, use the vt button and then choose in the schematic the corresponding node.

- **Determine large signal response delay:**

Set the pulse voltage source parameter **Voltage 1** to **0.2V** and **Voltage 1** to **1V**.
Perform transient analysis. Plot the following voltages: **vt (IN+)**, **vt (OUTn), vt (OUT+).**

Fill in the table:

$I_{F\ diff\ pair}$	t_d (IN+, OUT+)	t_d (IN+, OUTn)	t_d (OUTn, OUT+)
20	ns	ns	ns
10	ns	ns	ns
1	ns	ns	ns
0.1	ns	ns	ns

Comment the results:

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- **Determine small signal response delay:**

Set the pulse voltage source parameter **Voltage 1** to **0.59V** and **Voltage 2** to **0.61V**.
Perform transient analysis. Plot the following voltages: **vt (IN+), vt (OUTn), vt (OUT+).**

Fill in the table:

$I_{F\ diff\ pair}$	t_d (IN+, OUT+)	t_d (IN+, OUTn)	t_d (OUTn, OUT+)
20	ns	ns	ns
10	ns	ns	ns
1	ns	ns	ns
0.1	ns	ns	ns

Comment briefly the results:

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- **Set the differential pair dimensions as calculated for I_F = 1 and I_0 = 8 µA.**

Set the pulse voltage source parameter **Voltage 1** to **0.2V** and **Voltage 2** to **1V**.
Compare the response delay for different I_0 values.

I_0	t_d (IN+, OUT+)	t_d (IN+, OUTn)	t_d (OUTn, OUT+)
8 µA	ns	ns	ns
16 µA	ns	ns	ns
32 µA	ns	ns	ns

Comment the results:
