1. Setting up your working environment

Note: Executing commands and actions are enclosed in frames like this one.

1. Setting up your working environment

edauser0@selsrv1-edauserX> cd EE429_FULLCUSTOM

2. Extract the library of your lab.

EE429_FULLCUSTOM> gtar -xvf /softs/classroom/tutorials/2024-2025/EE435/Lab1_Techno_OTA.tar.gz

3. Run the cadence.

Run Virtuoso by typing: > virtuoso &

4. Create a link to the lab1 library:

In the Library Manager (Tools→Library Manager), click Edit → Library Path Editor, add library Lab1_Techno_OTA

Note: If you don't have the file EE429_FULLCUSTOM yet, then you have to create it and set your working environment as follows:

Start by creating a folder called EDALABS in your home directory. And go in it.

```
> cd
> mkdir EDALABS
> cd EDALABS
```

You can check your position in the hierarchy with *pwd* command. Run it and check where you are.

Each project is held in a separate directory which contains different configuration files and design data. Since many tools use configuration files that are stored in the *current* directory, the project directory actually defines a *working environment*. The file *"edabd2021_fullcust.tar.gz"*, contains the full and already configured working directory. Here we will only extract it and ***you will use the same directory throughout the laboratory sessions.*** **Please copy the directory as shown below. Please note that you can also use selsrv2 server.**

✓ Extract the directory for your project.

```
[1]edauser0@selsrv1-edauser0>
tar -xvf /softs/classroom/tutorials/2024-2025/EE429/EE429_FULLCUSTOM.tar.gz
[2] edauser0@selsrv1-edauser0> cd EE429_FULLCUSTOM ↵
```

2. Technology parameters extraction

Before designing circuits, you will extract and verify the values of the most important technology parameters. A simulation setup has been prepared for each parameter. Your task is to understand them and run the corresponding simulations to familiarize yourself with the 64nm technology.
The values of all the 64nm technology parameters are presented in the table below. Report the average values you obtain through simulations.

Parameter		Value Extracted	Value Simulation	Unit	
K_p	PMOS	90		$\mu A/V^2$	V_{DD}= 1.2 V V_{ss} = 0V
	NMOS	220			
U_a	PMOS	10		V/µm	
	NMOS	14			
V_{T0}		0.4		V	
n	PMOS	1.25		-	
	NMOS	1.2			
C_{ox}		13		$fF/\mu m^2$	
C_{ov}		0.2		fF/µm	

2.1. Normalized transconductance K_p

The K_p value will first be extracted for NMOS and PMOS transistors with W =10u and L = 400nm. Then, a large range of dimensions will be explored, and the variability of K_p will be verified.

1. Open the Kp schematic
2. Start the simulation environment: Launch → ADE Assembler
3. Open Existing View
4. Load "maestro"
5. Explore the TB to understand how it works
6. Run the simulation
7. Plot All → Explore and analyze the variability of Kpn and Kpp vs L and W

Write the equation used to simulate Kp and give its maximum value for W/L=10/0.4

Parameter	Equation	Value	Unit
k_{pn}			
k_{pp}			

2.2. g_m/I_d

The g_m/I_d curve will first be plotted for NMOS and PMOS transistors with W =10u L = 400nm. Then, a large range of dimensions will be explored.

1. Open the GmOverId schematic
2. Start the simulation environment: Launch → ADE Assembler
3. Open Existing View
4. Load "maestro"
5. Explore the TB to understand how it works
6. Run the simulation
7. Plot gm/Id → Explore and analyze the results
8. Verify the value given for the technology parameter "n".

Write the equation and values of is_n and is_p

Parameter	Equation	Value	Unit
is_n			
is_p			

2.3. Early voltage U_a

The Early voltage will first be extracted for NMOS and PMOS transistors with W =10u and L = 400nm at $I_F = 4$. Then, a large range of transistor lengths will be explored.

1. Open the U_a schematic
2. Start the simulation environment: Launch → ADE Assembler
3. Open Existing View
4. Load "maestro"
5. Explore the TB to understand how it works
6. Run the simulation
7. Extract Uan and Uap
8. Plot All → Explore and analyze the results

Observe the effect of increasing L on r_{on} and r_{op}. Does the output resistance increase when L increases, and how efficiently?

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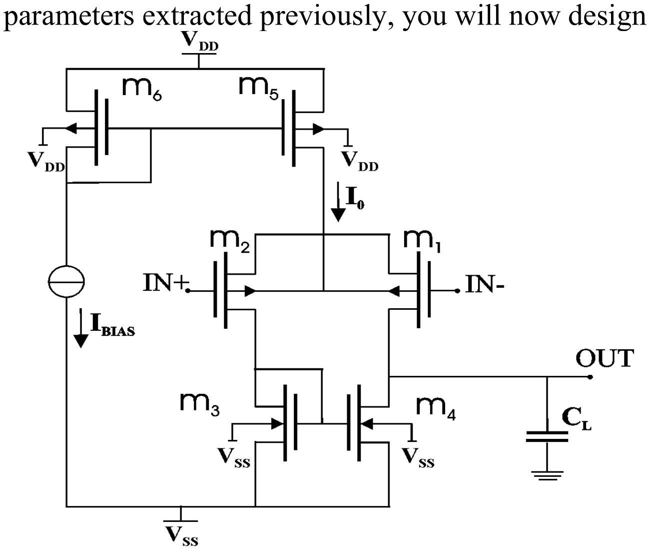
3. OTA design

Using the technology parameters extracted previously, you will now design a simple OTA.



3.1. Specifications

The circuit will be designed to meet the following specifications, which will be verified by simulation.

Parameter	Unit	
	Specification	
Open-loop: Gain: $\mathbf{A_o}$	≈ 35 dB (56)	dB
GBW: $\mathbf{f_{GBW}}$	25	MHz
Slew rate: **SR**	20	V/µs
Load Cap: $\mathbf{C_L}$	1	pF
$\mathbf{I_{F,5}}$	10	
$\mathbf{I_{BIAS}}$	10	µA

3.2. Sizing:

The OTA will now be sized. Calculate the following parameters in the proposed order.

	Parameter	Expression	Value	Unit	Guideline
Bias	I_0			µA	
	$\frac{W_5}{L_5}$			µm	$L_5 = 0.5\mu m$
Differential pair	g_{m2}			µS	*GBW*
	$\frac{g_{m2}}{I_{d2}}$			V^{-1}	
	$I_{F1,2}$			-	$I_F = I_c$ *is the inversion factor*
					Strong or weak inversion
	$\frac{W_{1,2}}{L_{1,2}}$			-	
	R_{out}			kΩ	A_o
	$L_{1,2}$			µm	R_{out}, $L_4 = L_2$
	$W_{1,2}$			µm	
	$\frac{W_4}{L_4}$			-	$I_F = 10$
	L_4			µm	$L_2 = L_4$
	W_4			µm	
	g_{m4}			µS	$\frac{g_m}{I_D} =$

3.3. Determine analytically

- **the poles (dominant and non dominant)**
- **the phase margin PM**
- **the common mode input range CMIR$^+$/ CMIR$^-$**
- **the output swing**

	Analytical expression	**Numerical value**
A [dB]		
f_{dom} [Hz]		
f_{nondom} [Hz] (neglect junction cap C_{SB}, C_{DB})		
PM [°]		
CMIR$^+$ [V]		
CMIR$^-$ [V]		
V_{OUTmax} [V]		
V_{OUTmin} [V]		
ΔV_{OUT} [V]		

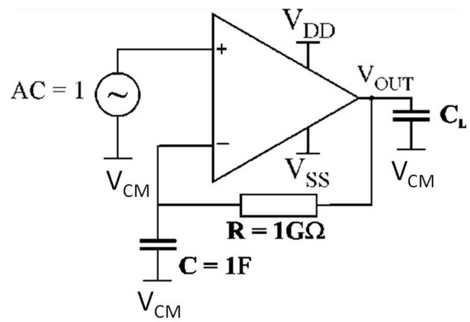
3.4. Design verification & Performance simulation

Using a prepared set of test-benches, the OTA performances will be verified by simulation.

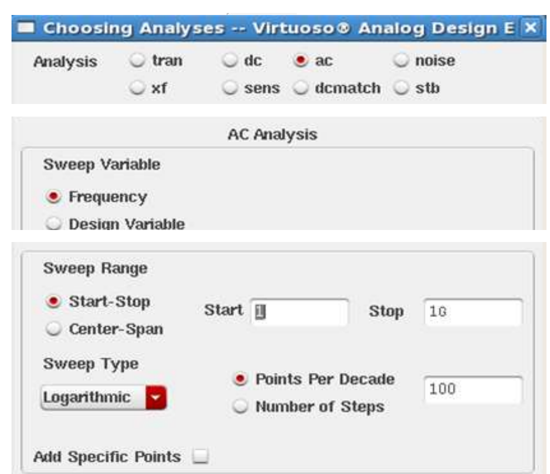
1. Open the OTA_65n schematic
2. Set all transistor sizes according to your design

3.4.1. Operating point and Open-loop gain

- The test-bench used to simulate the Dc and AC behavior of the OTA is the following:



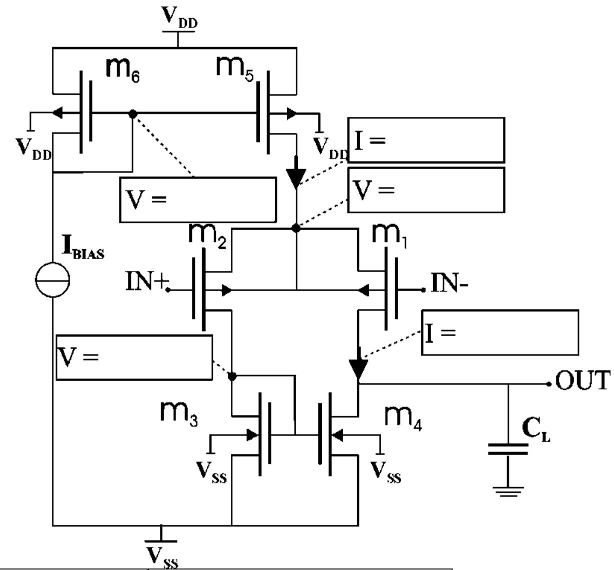
1. Open the Testbench TB_OTA_DC_AC schematic
2. Explore the TB to understand how it works
3. Start the simulation environment: Launch **ADE Assembler**
4. Create New View "maestro"
5. Set **Glogal Variables** for "DC voltage, current sources and Load capacitor"
6. Define a new test choosing **DC_Analysis** and select **Save DC operation Point.** (you can change the default test name to **DC_Test**))
7. Define a new test choosing **AC_Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to **AC_Test**).
8. Define for AC_Test the following expression to be plotted:
   open loop gain ? dB20(VF("/VOUT_OL"))
   open loop phase ? phase(VF("/VOUT_OL"))
9. Save, Run and Report the values on the following schematic, and fill-in the tables below and verify that they correspond approximately to theory (your calculations).



Note: To display the simulation results

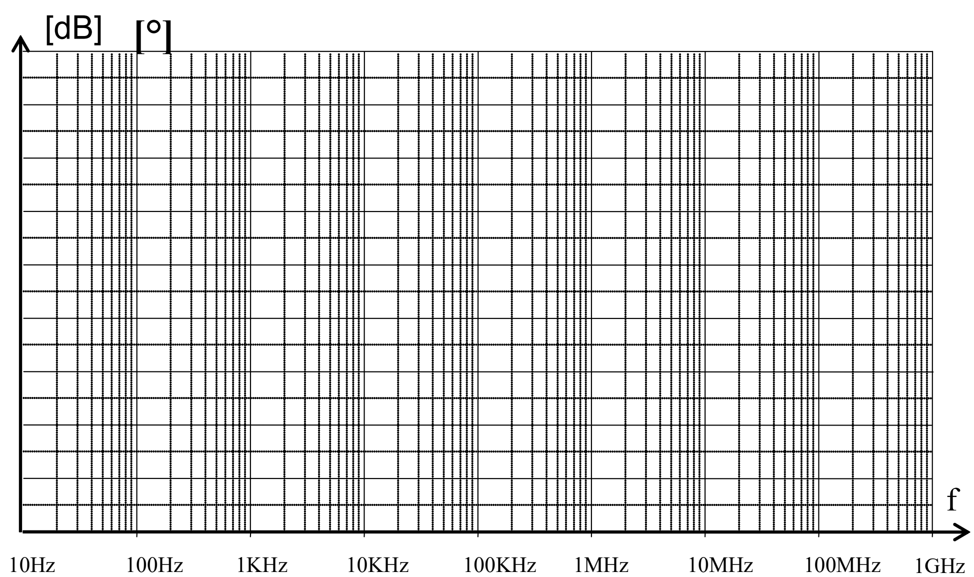
- Descend in the hierarchy to the schematic level of the OTA
- Select **maestro** tab
- Select **Results** tab
- Right click on **OP_Test** and select:

1. **Annotate→DC Node Voltages**
2. **Annotate→DC Operating Points**



	calculated	simulated
Dominant pole [kHz]		
Non-Dom pole [MHz]		
PM [°]		
$\mathbf{A_0}$ [dB]		
$\mathbf{f_{GBW}}$ [MHz]		

Provide the hand painted Bode plots for magnitude and phase:



Comment on stability:

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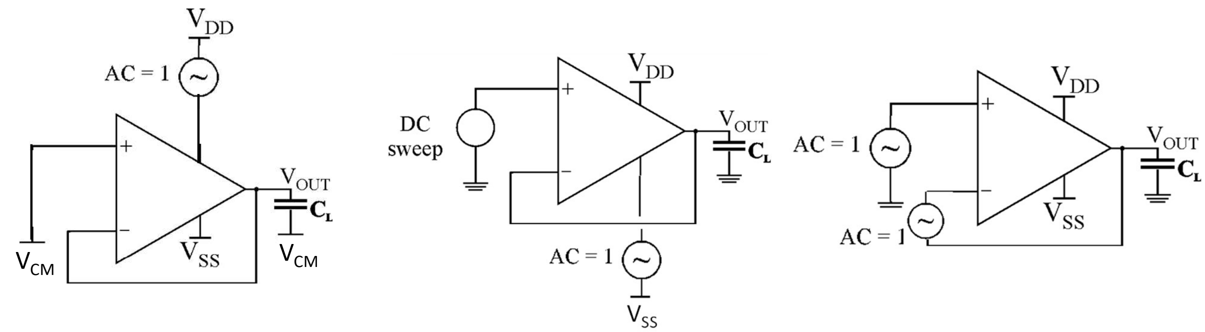
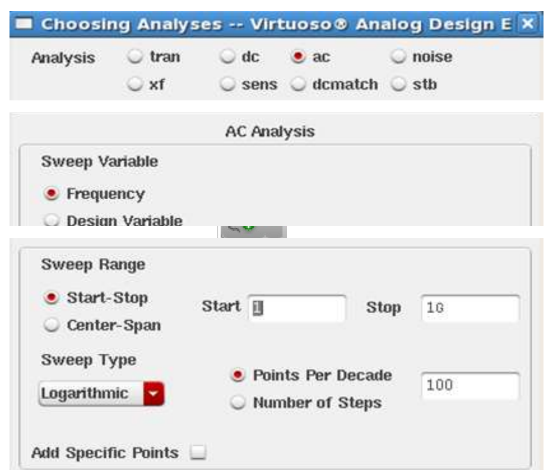
3.4.2. Power supply and Common mode rejections ratio (PSSR+, PSSr- & CMRR)

The test-bench for measuring the OTA PSSR + ; PSSR- and CMRR are:



1. Open the Testbench TB_OTA_PSRR_CMRR schematic
2. Explore the TB to understand how it works
3. Start the simulation environment: Launch **ADE Assembler**
4. Create New View "maestro"
5. Set **Glogal Variables** for "DC voltage, current sources and Load capacitor"
6. Define a new test choosing **AC_Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to **AC_Test2**).
7. Define for AC_Test2 the following expression to be plotted:
   (-dB20(VF("/VOUT_PSRR+")))
   (-dB20(VF("/VOUT_PSRR-")))
   (-dB20(VF("/VOUT_CMRR")))
8. Save, run and report the values on the following schematic, and fill-in the tables below and verify that they correspond approximately to theory (your calculations).



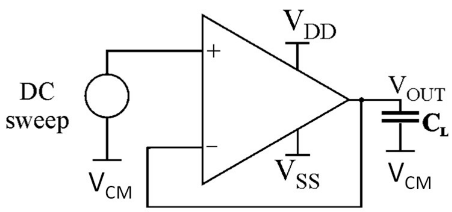
	Simulated @ low fréquency
PSRR+ [dB]	
PSRR- [dB]	
CMRR [dB]	

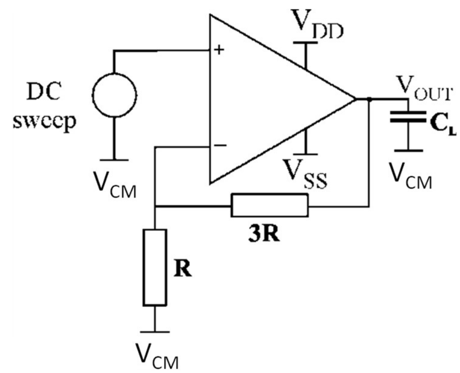
Explain briefly the equations used :

……………………………………………………………………………………………………
……………………………………………………………………………………………………
……………………………………………………………………………………………………

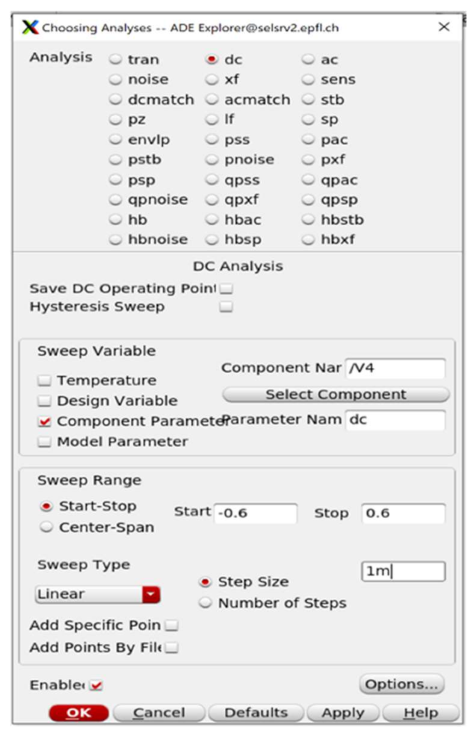
3.4.3. Input common-mode range

The test-bench for measuring the OTA input common-mode range and output range are :





1. Open the Testbench TB_OTA_CMIR_DVout
2. Explore the TB to understand how it works
3. Start the simulation environment: Launch **ADE Assembler**Create
4. New View "maestro"
5. Set **Glogal Variables** for "DC voltage, current sources and Load capacitor"
6. Define a new test and choose **DC Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to *DC_Test*)**.**
7. Define the following expression to be plotted:
   Common mode input range → deriv(VDC ("/VOUT_CMIR")) VDC("/VOUT_SW")
   Output swing → deriv(VDC("/VOUT_SW"))
8. Save, run the simulation and fill in the table below.



Measure the input and output ranges for a maximun gain variation of -10 %

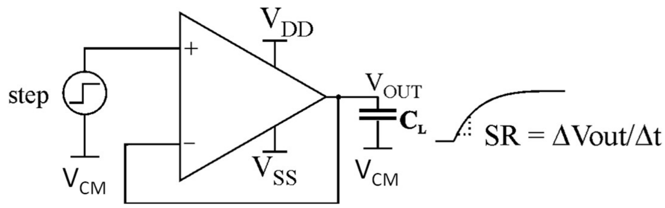
Parameter	Value		Unit
	Simulation	Optimized	
Input CMR+			V
Input CMR-			V
Output Range+			
Output Range-			

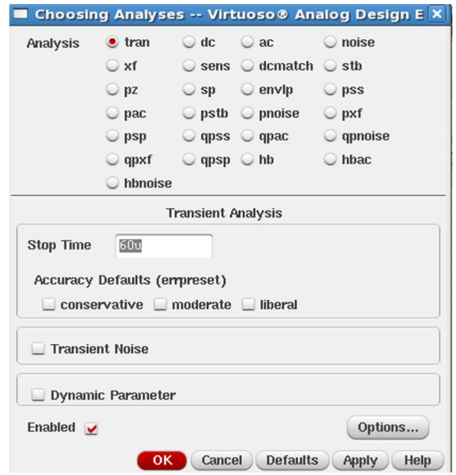
NOTE: *For the Output Swing, group /VOUT_SW and deriv(VDC("/VOUT_SW")) plots in the same subwindow in Virtuoso and Analysis Waveform XL.*

- *Select the subwindow with the two signals*
- *select the deriv(VDC("/VOUT_SW")) signal and then select Axis →Y vs Y.*

3.4.4. Slew rate

The test-bench for measuring the slew-rate is:





1. Open the Testbench_OTA_SlewRate
2. Start the simulation environment: Launch ADE Assembler
3. Open Existing View
9. Load "maestro"
10. Define a new test and choose **tran Analysis** and set the simulation parameters as shown in the snapshot on the right (you can change the default test name to SR_*Test*).
11. Define the following expression to be plotted:
    Slew Rate → deriv(VT("/VOUT_SR"))
12. Run the Simulation and fill in the table below.

Parameter	Value		Unit
	Simulation	Optimized	
SR+			V/µs
SR-			V/µs