SYNOPSYS®

SiWare Single Port High Density Leakage Control Register File 32K Sync Compiler For Common Platform 65nm LPe LowK Periphery Mixed Vt/Cell High Vt Process

User Manual

DesignWare® Embedded Memories
cp65npky1p11asdrl32ks

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Synopsys, Inc.
690 E. Middlefield Road
Mountain View, CA 94043

www.synopsys.com

Revision History

Note	Links and references to section, table, figure, and page numbers in this table are only assured to be valid for the version in which the change is made.

Date	Document Version	Description
June 2011	A04P1	Document for A04P1 Full GDS compiler release. Also updated formatting to conform to Synopsys documentation standards.
June 2014	A04P2	Data updated for A04P2 Full GDS compiler release.
November 2017	A04P3	Document to support A04P3 Full GDS compiler release. No change in compiler data.

Contents

About This Manual

This manual shows you how to use Synopsys' DesignWare Embedded Memories. It describes an overview of Synopsys' memories, compiler profile, the compiler directory structure, front-end files, back-end files, and user-configurable files.

Audience

This manual is intended for design engineers and customer support engineers assumed to be familiar with integrated circuit design technology.

Using this Manual

This manual is organized into the following chapters:

Section	Describes
Chapter 1, "Product Line Overview"	The key features of the memory compiler
Chapter 2, "Compiler Profile"	The functional features, specifications, and timing characterization of the compiler
Chapter 3, "Compiler Source and Output Files"	The directory structure of the compiler database, files, and templates
Chapter 4, "Using Front-End Files"	The files in the front-end views
Chapter 5, "Using Back-End Views"	The back end views files that support layout and fabrication
Chapter 6, "Configuring Files"	How to configure the custom global (GLB) file, the Layer Transition Table file (LTT), and the Power Place and Route (PPR) file

Minimum Operating System Requirements

- 1 gigabyte main memory
- 1 gigabyte of disk space per compiler to support installation of the compiler and generation of at least one instance.

See the Release Notes for Embed-It!® for a list of hardware and software supported.

Synopsys' Product Releases

Synopsys, Inc. releases a new version of pre-silicon products (version A) periodically. These products incorporate Product Change Requests (PCRs) that resolve bugs and provide product enhancements. To address high-priority change requests, Synopsys, Inc. also provides a patch release between quarterly updates when necessary. A patch release is denoted by the suffix p*n* where *n* is a release number such as 1, 2, or 3 (p1, p2, or p3). See the **release.txt** file in the `complib` directory for a list of release dates.

License files need not be updated for patch releases.

Related Documentation

The following documents provide more information about software used with the memory compilers.

For information on	See
How to use Synopsys' Embed-It! Integrator software interface to generate memory components.	Embed-It!® Integrator User Guide
Mentor Graphics FastScan	http://www.mentor.com/dft/fastscan_ds.pdf
Synopsys TetraMAX	http://www.synopsys.com/Tools/Implementation/RTLSynthesis/Test/Pages/TetraMAXATPG.aspx

Getting Technical Assistance

For technical support with Synopsys' products, please contact the Synopsys Support Team at http://solvnet.synopsys.com.

1 Product Line Overview

This chapter provides an overview of Synopsys' DesignWare Embedded memories and the key features of *55nm/65nm SiWare™ High-Density Leakage Control (LC) Compilers*.

1.1 High-Density Memory Compilers

The Synopsys' 55-nanometer and 65-nanometer (nm) SiWare product family of memory compilers provides a powerful dashboard of options that enables System-on-Chip (SoC) designers to explore trade-offs between performance, area, power, and statistical yield to generate optimal memory configurations. This dashboard control capability is critical at 55nm/65nm where design and process complexities require sophisticated management of the various trade-offs to effectively meet stringent end-product requirements and increasingly narrow time-to-market windows.

The Synopsys' SiWare High-Density products provide ASIC vendors and designers with:

- Memory instances optimized for area, without compromising quality.
- Memory compilers that leverage the standard foundry delivered bit cells to ensure high yield and reliability.
- Memory compilers that provide an option for including redundancy capabilities for repair purposes.
- Memory compilers with an option for leakage control.
- Front-end and back-end model views for integration into EDA tools from leading tool suppliers.

The SiWare High-Density memory compilers are optimized to generate memories with the absolute minimum area and power to enable designers to achieve aggressive critical path requirements. The SiWare High-Performance memory compilers minimize both static and dynamic power consumption and provide optimal yields.

SiWare SRAM compilers offer both performance and leakage control modes. All SiWare compilers support ultra-low voltage operation with characterization at 20% below nominal voltage. Synopsys, Inc. provides power saving design techniques to implement leakage control:

- Source Biasing
- Fine-grained Power Gating
- Selective Use of HVt and Long L Devices

The SiWare High-Density memory compilers offer three licensable features to support Test and Repair. Each of these features may be combined with advanced power management licensing. These features include:

- SiWare Light (SiWare-LT) mode without Built-in test muxes or repair.
- SiWare Integrated Test (SiWare-IT) mode that incorporates built-in test muxes and other test circuitry to enable at-speed testing
- SiWare STAR (SiWare-ST) mode that includes redundancy, test muxes and other test circuitry to enable at-speed testing and Built-In Test and Repair, BISR.

Synopsys' STAR Memory System (SMS) enables cost-effective embedding, testing and repairing of SiWare memories. The integrated test and repair capability ensures higher yielding semiconductors, and can potentially save millions of dollars in recovered silicon, substantially reduce test costs, and enable faster time to volume.

Table 1-1 displays the Synopsys' High-Density SiWare memory options available.

The availability of the options described is controlled by licensing.
Redundancy is only available for the single port, dual port and STAR 8M memory compilers.

Table 1-1 SiWare High-Density Memory Options

Configuration	Description	Parameters Required

SiWare-LT
(default configuration)
	ASAP
	(default configuration)
		`redundancy_enable=FALSE`
		`bist_enable=FALSE`
		`low_leakage=FALSE`

SiWare-IT	ASAP with BIST	`redundancy_enable=FALSE`
		`bist_enable=TRUE`
		`low_leakage=FALSE`

SiWare-ST	STAR	`redundancy_enable=TRUE`
		`bist_enable=TRUE`
		`low_leakage=FALSE`

SiWare-LT
(with Leakage Control)
	ASAP
	(with Leakage Control)
		`redundancy_enable=FALSE`
		`bist_enable=FALSE`
		`low_leakage=TRUE`

SiWare-IT
(with Leakage Control)
	ASAP with BIST
	(with Leakage Control)
		`redundancy_enable=FALSE`
		`bist_enable=TRUE`
		`low_leakage=TRUE`

SiWare-ST
(with Leakage Control)
	STAR
	(with Leakage Control)
		`redundancy_enable=TRUE`
		`bist_enable=TRUE`
		`low_leakage=TRUE`

1.2 Compiler Features

The High-Density compilers provide the following features:


Note Some of the features described might not be supported by the current compiler.

1.2.1 Power Saver Mode

The Power Saver mode, also referred to as Leakage Control (LC), is enabled when the **`low_leakage`** flag is set to **TRUE**. The Power Saver mode enables approximately 60% leakage reduction with respect to Performance Mode. Power Saver mode is a compile time option, enabled by the flag **`low_leakage=TRUE`**. The actual functionality is controlled by the memory enable pin. The memory is in standby state when the memory enable (**ME**) pin is de-asserted. It is in this condition that the leakage control circuitry within the memory will be activated and the memory will transition to a low leakage standby state.


Note The availability of the options described is controlled by licensing.

1.2.2 Performance Mode

The Performance Mode is available in the base compiler and is enabled when **`low_leakage=FALSE`**. In this mode, the compiler is optimized for maximum performance as shown in Figure 1-1. In Performance Mode the memory incorporates standard Vt transistors throughout the memory array and periphery.

Figure 1-1 Performance Mode vs. Power Saver Mode Trade-offs

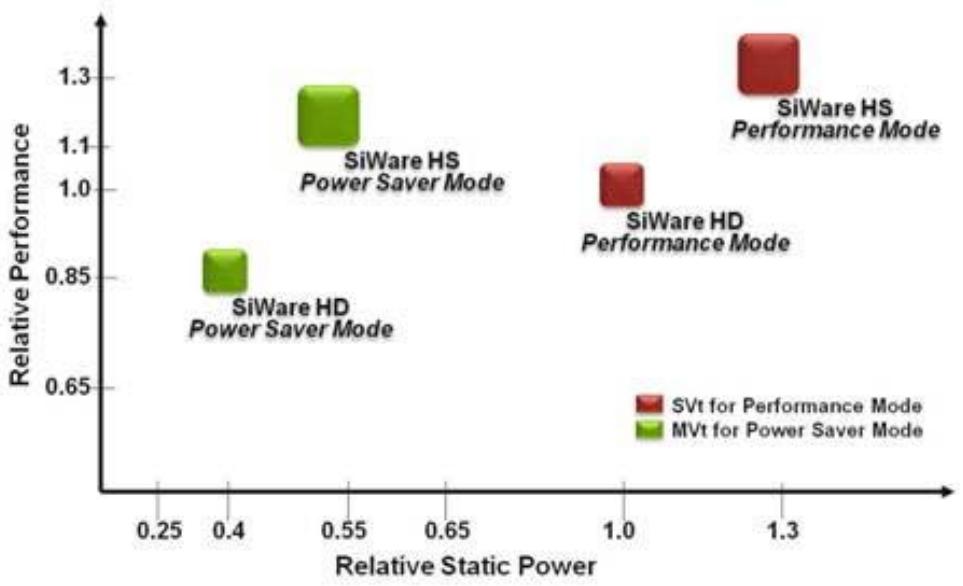
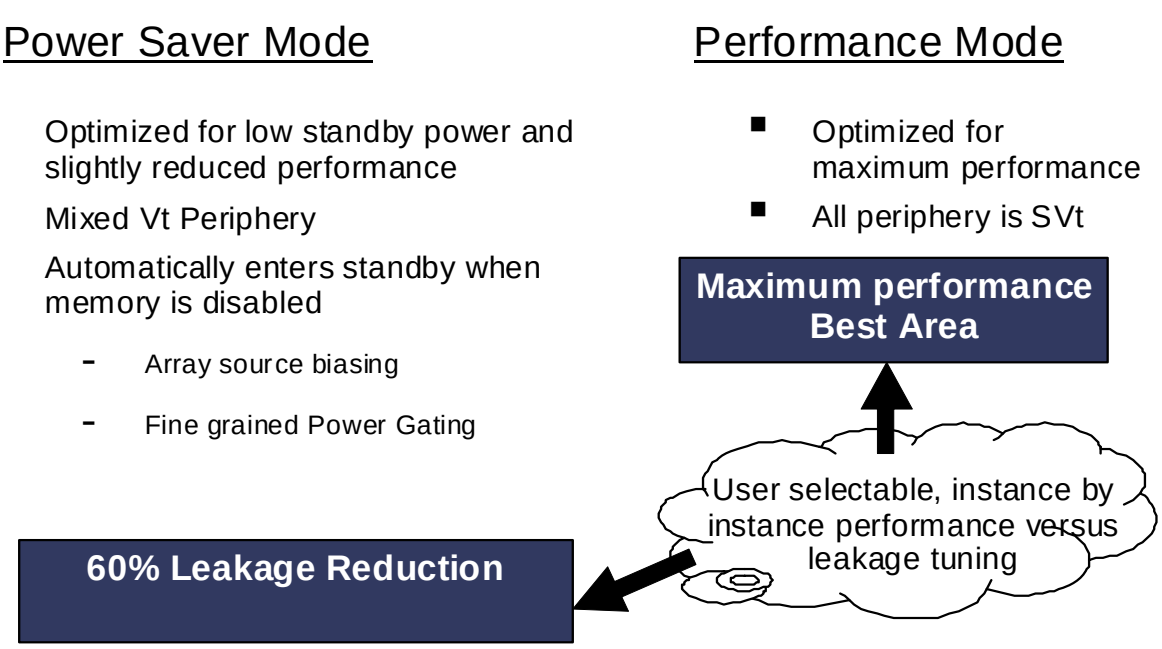


Figure 1-2 summarizes the design implementation differences between the Power Saver mode (**`low_leakge=TRUE`**) and the Performance Mode (**`low_leakage=FALSE`**).

Figure 1-2 Design Implementation Differences



1.2.3 BIST Interface

The SiWare-IT (without redundancy) and SiWare-ST (with redundancy) options create memory instances that include all of the necessary logic to facilitate at-speed Built In Self Test (**BIST**). BIST is enabled by setting the **bist_enable** GLB parameter.

When the **bist_enable** option is enabled, the generated memory instance includes multiplexers (muxes) for all address, control and data signals as well as comparators and capture logic. All output signals are fully scannable and the data flows synchronous with the external clock. Incorporating this logic into the memory instance reduces the critical path when BIST is enabled and reduces the number of wires that are required to route between the memory instance and the BIST engine.

Note Comparison logic functionality is not available for register file compilers.

The integrated logic will also enable high performance testing of functional logic surrounding the memory in your designs, using ATPG scan tools.

Synchronous Write-through is available when these options are enabled. This allows input data to flow to output pins synchronously with the clock.

Several pins are added to support BIST. Refer to Table 2-2, “Input Pin Description”.

1.2.4 Redundancy

The SiWare-ST option enables the memory compiler to generate memory instances that include redundancy for repair. Redundancy is enabled with the **redundancy_enable** GLB parameter.

When **redundancy_enable** is activated, additional memory is added to the instance to be used when BIST diagnostics determine that a repair is necessary. The number and configuration of repair elements is dependent on the compiler as described in Table 1-2.

Table 1-2 Redundancy Repair Elements

	Single Port and Dual Port	1-Port and 2-Port RF	ROM
Redundancy Type	Column	Not applicable	Not applicable
Description	1 element of 4 columns on each side of the center decoder		

1.2.5 Read Pipeline

Note This feature is not applicable for Register Files.

The 55nm/65nm compilers support one clock cycle latency for Read operation. When **pipe_line_read** flag is set to 1 in SiWare-LT mode, there will be a pin SWT controlling the output behavior. The output will

be driven through the flop when SWT pin is set to 1. However, incase of SiWare-IT and SiWare-ST mode, the SWT pin will by default control the output behavior. The output will be driven through the flop when SWT pin is set to 1 and flow-through when SWT = 0.

1.2.6 Asynchronous Write Through (AWT)

Whenever the Asynchronous Write Through (**AWT**) signal is active, the output pins receive the value of the input pins in a specified time delay (regardless of the clock). The **AWT** pin is only visible when **`bist_enable=TRUE`**. In the case of SiWare-IT and SiWare-ST mode, when **`awt_enable=TRUE`** and **`SW=1`**, Q=D xor WEM, and when **`awt_enable=TRUE`** and **`SW=0`**, **`Q=D`**. Use the AWT option for test coverage improvement. It lets signals travel across the memory and enables the internal memory logic to be visible to the external test circuit. This eliminates the hidden embedded circuit effect of the internal memory logic. The test circuit can be a scan circuit or any other type of circuit.

1.2.7 Read Margin Control

There are four Read Margin (**RM**) pins that provide the ability to trade-off between speed and robustness by adjusting the time to strobe the sense amplifiers.

Setting the RM defines when the sense amplifiers are strobed. The bitlines (BT & BC) are precharged to a level before a memory cell is accessed. When the memory cell is accessed, it generates a differential signal between the bitlines. This differential signal is fed to the sense amplifier. It takes time for the differential signal to develop and the longer you wait to strobe the signal, the greater the differential signal to the sense amplifier. The longer you wait, the easier it is for the sense amplifier to determine what was stored in the memory cell. Thus the term *Robustness*. The longer you wait, the longer it takes to access the cell (i.e., access time). Thus, the term *Speed Tradeoff*.

The **timing mode** option allows you to choose the process-sigma characterization and read-write margin settings to use during instance generation All memories are characterized for RM [3:0] =4'b0000 to 4'b0011. The default RM setting for all memories will be RM [3:0] =4'b0010.

Timing views for different RM settings can be generated by setting the **`timing_mode`** parameter. The valid values for the **`timing_mode`** parameter are **slow**, **default**, and **fast.**

Table 1-3 Timing Mode Options

Value	RM1	RM0	Description
DEFAULT (Medium)	1	0	Used for optimal trade-off between performance and yield during volume production.
FAST	1	1	Used for increased performance for designs with low memory count on the chip.
SLOW	0	1	Used slower performance for very high memory count on the chip.

RM values specified in the datasheet are the values used in characterization and recommended to set for RM pins. Default RM setting is also hard-coded inside memory and selectable by RME pin (set to low).

1.2.8 Self Time Bypass

In the Self Time bypass mode is controlled by toggling the **TEST1** pin. In this mode (**TEST1=1**), the memory self time circuitry is bypassed. The memory timing is controlled by the external clock signal (**CLK**). Self Time bypass mode is initiated after the rising edge of **CLK** and is terminated by the falling edge. The Self Time bypass mode may be used to determine the margin of the internal self-timed circuitry.

1.2.9 Bit Write

The Bit Write feature lets you independently write to any subset of the memory word. You can write to each bit separately, and still retain the value of other bits before the write operation. The Bit Write feature provides a Write-Enable Mask (**WEM**) pin for each I/O pin.

Assuming active high control:

- If the **WEM** pin for an I/O is high, the data on the input pin (**D**) is written to the corresponding bit cell in the addressed location.
- If the **WEM** pin for an I/O is low, the data on the input pin (**D**) is not written to the corresponding bit cell in the addressed location.

There is no loss of power or speed when you enable the Bit Write feature. However, power will be reduced by disabling writes using these pins. See "Functional Options" on page 28 for more information about enabling this option.

1.2.10 Performance Boosters

There are several performance boosting features available within the 55nm/65nm SiWare compilers. Table 1-4 provides the parameters used to enable the options, as well as the performance enhancement obtained with each option.

Table 1-4 Performance Booster Options

Feature	GLB Parameter	Description
Banks	**BK**	Setting the number of banks provides a compile time option to split the memory into more than one bank. Memory banking is efficient for large instances. It improves performance and active power at the cost of area.
Column Mux	**CM**	Allows you to change the aspect ratio of the instance for chip floorplan for a trade-off between area and performance.

User-selectable banking is available in Single Port and Dual Port SRAM compilers only.

2 Compiler Profile

This chapter describes the functional features, specifications, and timing characterization of the *SiWare Single Port High Density Leakage Control Register File 32K Sync Compiler For Common Platform 65nm LPe LowK Periphery Mixed Vt/Cell High Vt Process*.

2.1 Compiler Naming Convention

Synopsys, Inc. uses the same name for a compiler and for the directory that contains the compiler library files. Compiler names contain segments of lowercase, alphanumeric characters with each segment denoting a characteristic of that specific compiler. For example, Table 2-1 explains the structure of the name for the current compiler cp65npky1p11asdrl32ks.

Table 2-1 Compiler Naming Convention

Name Segment	Value in cp65npky1p11asdrl32ks	Description
Foundry	cp	Common Platform
Technology	65n	65 nanometers
Process	pky	LPe LowK Periphery Mixed Vt/Cell High Vt
Ports	1p	Single Port The format is *n*p, where *n* is the number of ports
Read/Write	11	One read and one write port The format is *nm*, where *n* is the number of read ports and *m* is the number of write ports.
Product family	as	SiWare, ASAP only.
Product subfamily	drl	High-Density Leakage Control Register File
Size	32k	32K bits
Protocol	s	Synchronous clock

2.2 Compiler Features and Benefits

The *SiWare Single Port High Density Leakage Control Register File 32K Sync Compiler For Common Platform 65nm LPe LowK Periphery Mixed Vt/Cell High Vt Process* provides:

- Over 600 MHz worst-case clock frequency for a 64 x 16, CM=4 instance (ss, 1p08v, n40c).
- Two aspect ratios for maximum area and performance optimization.
- Zero quiescent current consumption when all Register File inputs including clocks are stable.
- Separate input (D) and output (Q) pins that support a synchronous write-through feature.
- Built-in BIST interface that provides easy connection to memBIST or other third party BIST applications.
- Configured active high or active low control signals.
- Optional sub-word capability, which allows each bit in a word to be independently selected by a bit in the write enable-mask for write for column-mux 4.
- Flexibility in specifying the logical size of the RAM, including both word size and number of address locations and column mux.
- Dynamic Voltage and Frequency Scaling support: Foundry specified VDDMIN supported (0.96V), (license needed). If parameter is available for use, a lower voltage range of operation is enabled.

2.3 Specifications

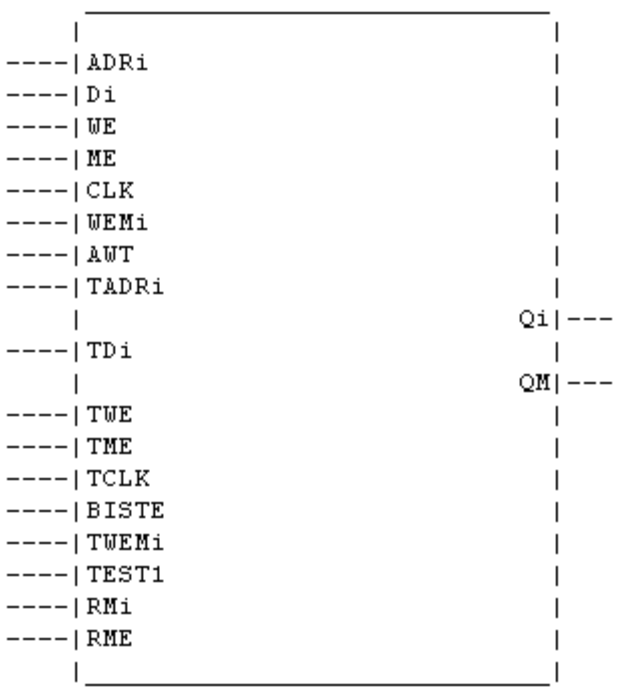
This section describes the specifications of the *SiWare Single Port High Density Leakage Control Register File 32K Sync Compiler For Common Platform 65nm LPe LowK Periphery Mixed Vt/Cell High Vt Process*.

2.3.1 Memory Symbol

Figure 2-1 shows the circuit symbol for a memory instance generated for the *SiWare Single Port High Density Leakage Control Register File 32K Sync Compiler For Common Platform 65nm LPe LowK Periphery Mixed Vt/Cell High Vt Process*.

Note Figure 2-1 contains all possible pins. Not all pins are present on all instances. See Figure 2-5 on page 27 for illustrations of the different pinout options.

Figure 2-1 Memory Symbol



2.3.2 Pin Capacitance and Description

Table 2-2 shows a list of input signal pins and provides a brief description. The number of bits against the pin names in following tables applies to the instance configuration specified in Table 2-21 on page 44. Values may differ for different instances.

Table 2-2 Input Pin Description

Signal	Enabled	Description
ADR [5:0]	always	Address input. The address input port is used to address the location to be written during the Write cycle and read during the Read cycle.
D [15:0]	always	Data input. The data input bus is used to write the data into the memory location specified by the address input port during the Write cycle.

WEM [15:0]	`wem_enable=TRUE`
	`use_sw=yes`
	`SW=1`
		Maskable Write Enable. It includes the Bit Write feature where selective write to individual I/O's can be done using the Maskable Write Enable signals. When the memory is in Write cycle, one can write selectively on some I/O's.

WE	always	Write Enable input. When the Write Enable input is Logic High, the memory is in the Write cycle. When the Write Enable input is Logic Low, the memory is in the Read cycle.
ME	always	Memory Enable input. When the Memory Enable input is Logic High, the memory is enabled and read/write operations can be performed. When the Memory Enable input is Logic Low, the memory is deactivated & the leakage is significantly reduced.
CLK	always	Clock input. This is the external clock for the memory.
AWT	`bist_enable=TRUE` or `awt_enable=TRUE`	Asynchronous Write Through. This signal is not dependent on clock. Therefore, no setup or hold time is required and used for datapath checking. Whenever this signal is active, memory array is bypassed to test interface shadow logic.
TADR [5:0]	`bist_enable=TRUE`	Address inputs for BIST. This address input port is used to address the location to be written during the Write cycle and read during the Read cycle. This pin is used when BIST is enabled.
TD [15:0]	`bist_enable=TRUE`	Data Inputs for BIST. This data input bus is used to write the data into the memory location specified by the address input port during the Write cycle. This is used only when the BIST is enabled.

TWEM [15:0]	`bist_enable=TRUE`
	`wem_enable=TRUE`
	`use_sw=yes`
	`SW=1`
		Maskable Write Enable for BIST. It includes the Bit Write feature where selective write to individual I/O's can be done using the Maskable Write Enable signals. When the memory is in Write cycle, you can write selectively on some I/O's. This pin is used only when BIST is enabled.

TWE	`bist_enable=TRUE`	Write Enable for BIST. When the BIST Write enable input is Logic High, the memory is in the Write cycle. When the BIST Write Enable is Logic Low, the memory is in the Read Cycle. This pin is used only when BIST is enable.

Table 2-2 Input Pin Description

Signal	Enabled	Description
TME	`bist_enable=TRUE`	Memory Enable for BIST. When the BIST Memory Enable is Logic High, the memory is enabled and read/write operations can be performed. When the BIST Memory Enable is Logic Low, the memory is deactivated & the leakage is significantly reduced. This is used only when BIST is enabled.
TCLK	`bist_enable=TRUE`	BIST Clock Input. This is the external clock for the memory. This is used only when BIST is enabled.
BISTE	`bist_enable=TRUE`	BIST Enable. It controls the BIST test mode. When enabled, it can be used for testing memory without modifying the main circuit.
TEST1	always	Test pin to bypass self-timed circuit. The external clock controls the read and write control signals.
RME	always	Read Margin Enable Input. This input selects between the default RM setting (RME = 0), and the external RM pin setting (RME=1).
RM [3:0]	always	Read margin Input. This input is used for setting the read margin It programs the sense amp differential setting. and allows the trade off between speed and robustness. RM[1:0] = 2'b00 is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. RM[1:0] values control access time & cycle time of the memory. Refer to the timing table for more details. RM[3:2] are factory pins reserved for debug mode. User should tie these pins to ''logic 0''.

Table 2-3 and Table 2-4 provide the pin capacitance data for SiWare-LT and SiWare-IT. All values are in ''pf''.

Table 2-3 Input Pin Capacitance - SiWare-LT- 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=TRUE)

Pin Name	tt1p2v 25c	ff1p32v n40c	ss1p08v 125c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
ADR [5:0]	0.002962	0.003010	0.002931	0.002900	0.003052	0.003009	0.002897
D [15:0]	0.000499	0.000558	0.000463	0.000436	0.000613	0.000557	0.000433
WE	0.002946	0.003023	0.002894	0.002855	0.003071	0.003022	0.002851
ME	0.003038	0.003112	0.002988	0.002948	0.003160	0.003111	0.002944
CLK	0.021043	0.022053	0.020129	0.020123	0.022115	0.022073	0.020123
WEM [15:0]	0.000499	0.000558	0.000463	0.000436	0.000613	0.000557	0.000433
TEST1	0.003560	0.003567	0.003564	0.003527	0.003603	0.003565	0.003523
RM [3:0]	0.015500	0.015500	0.015500	0.015500	0.015500	0.015500	0.015500
RME	0.004303	0.004357	0.004274	0.004225	0.004422	0.004354	0.004220

Table 2-4 Input Pin Capacitance - SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=TRUE)

Pin Name	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
ADR[5:0]	0.001852	0.001912	0.001803	0.001785	0.001942	0.001913	0.001784
D[15:0]	0.000312	0.000329	0.000299	0.000291	0.000344	0.000328	0.000290
WE	0.001493	0.001525	0.001468	0.001452	0.001549	0.001525	0.001451
ME	0.001499	0.001531	0.001474	0.001459	0.001555	0.001531	0.001458
CLK	0.017754	0.018245	0.017238	0.017414	0.018123	0.018268	0.017434
WEM[15:0]	0.000312	0.000329	0.000299	0.000291	0.000344	0.000328	0.000290
AWT	0.011898	0.012092	0.011760	0.011540	0.012241	0.012080	0.011521
TADR[5:0]	0.001852	0.001912	0.001803	0.001785	0.001942	0.001913	0.001784
TD[15:0]	0.000312	0.000329	0.000299	0.000291	0.000344	0.000328	0.000290
TWE	0.001493	0.001525	0.001468	0.001452	0.001549	0.001525	0.001451
TME	0.001499	0.001531	0.001474	0.001459	0.001555	0.001531	0.001458
TCLK	0.017754	0.018245	0.017238	0.017414	0.018123	0.018268	0.017434

Table 2-4 Input Pin Capacitance - SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=TRUE)

Pin Name	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
BISTE	0.004103	0.004189	0.004043	0.003887	0.004308	0.004179	0.003875
TWEM[15:0]	0.000312	0.000329	0.000299	0.000291	0.000344	0.000328	0.000290
TEST1	0.004562	0.004569	0.004565	0.004528	0.004605	0.004567	0.004524
RM[3:0]	0.015500	0.015500	0.015500	0.015500	0.015500	0.015500	0.015500
RME	0.004762	0.004814	0.004733	0.004685	0.004877	0.004811	0.004681

Table 2-5 shows the output signal pins, their capacitance, and provides a brief description.

Table 2-5 Output Pin Capacitance and Description - 64x16CM4SW1BK1

Signal	Enabled	Pin Capacitance (pf)		Description
		SiWare-LT	SiWare-IT	
Q [15:0]	always	0.015	0.015	Data output bus. It outputs the contents of the memory location addressed by the Address Input signals.
QM	`bist_enable=TRUE`	N/A	0.015	AWT XOR function Output.This output is used to control and observe the test mux output in the Control block.

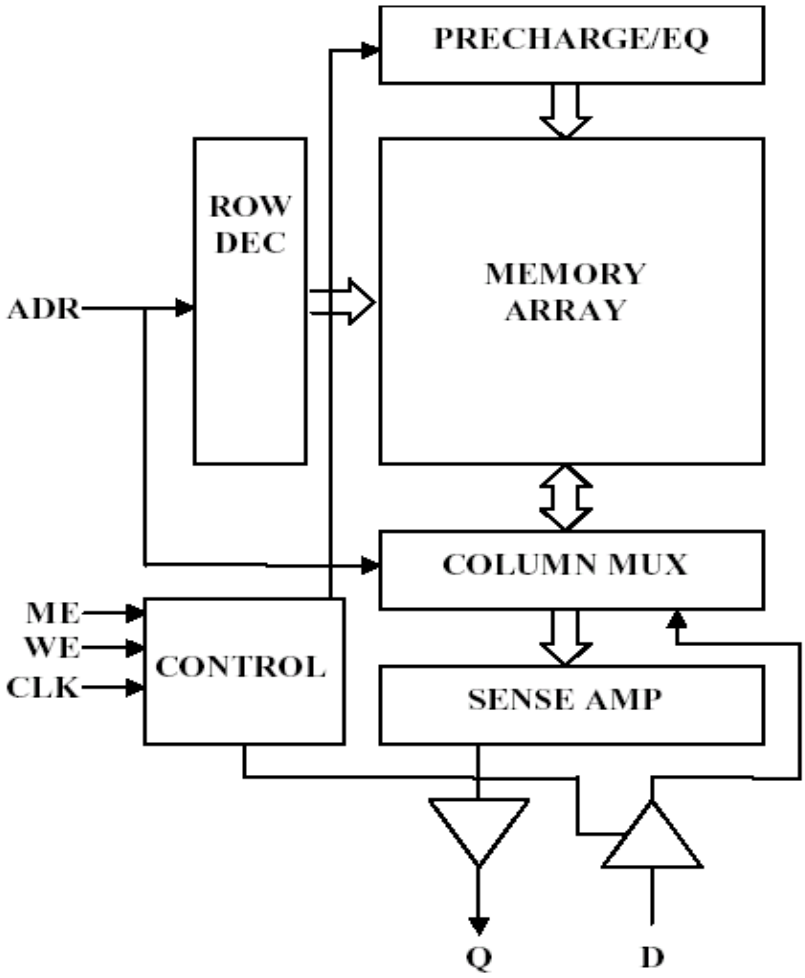
2.3.3 Block Diagrams

This section shows the block diagrams for *SiWare Single Port High Density Leakage Control Register File 32K Sync Compiler For Common Platform 65nm LPe LowK Periphery Mixed Vt/Cell High Vt Process.*

2.3.3.1 BIST Disabled Block Diagram for CM=2

Figure 2-2 shows the block diagram for CM=2 when the BIST mode is disabled.

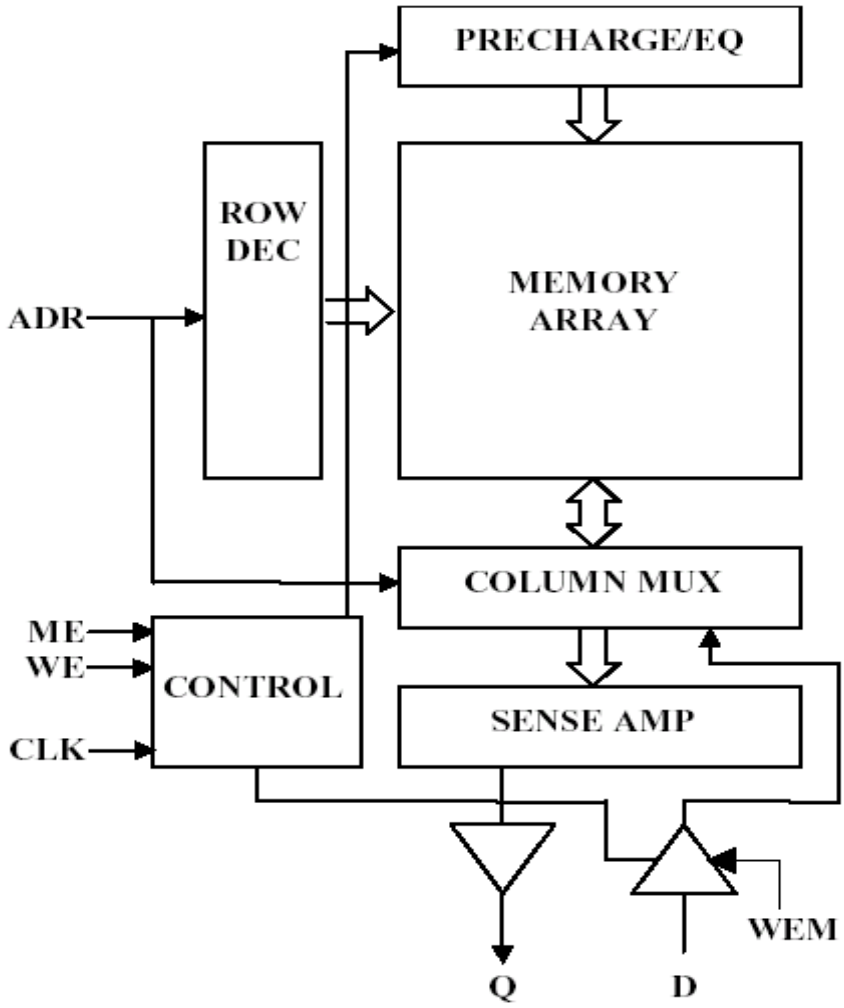
Figure 2-2 BIST Disabled Block Diagram for CM=2



2.3.3.2 BIST Disabled Block Diagram for CM=4

Figure 2-3 shows the block diagram for CM=4 when the BIST mode is disabled.

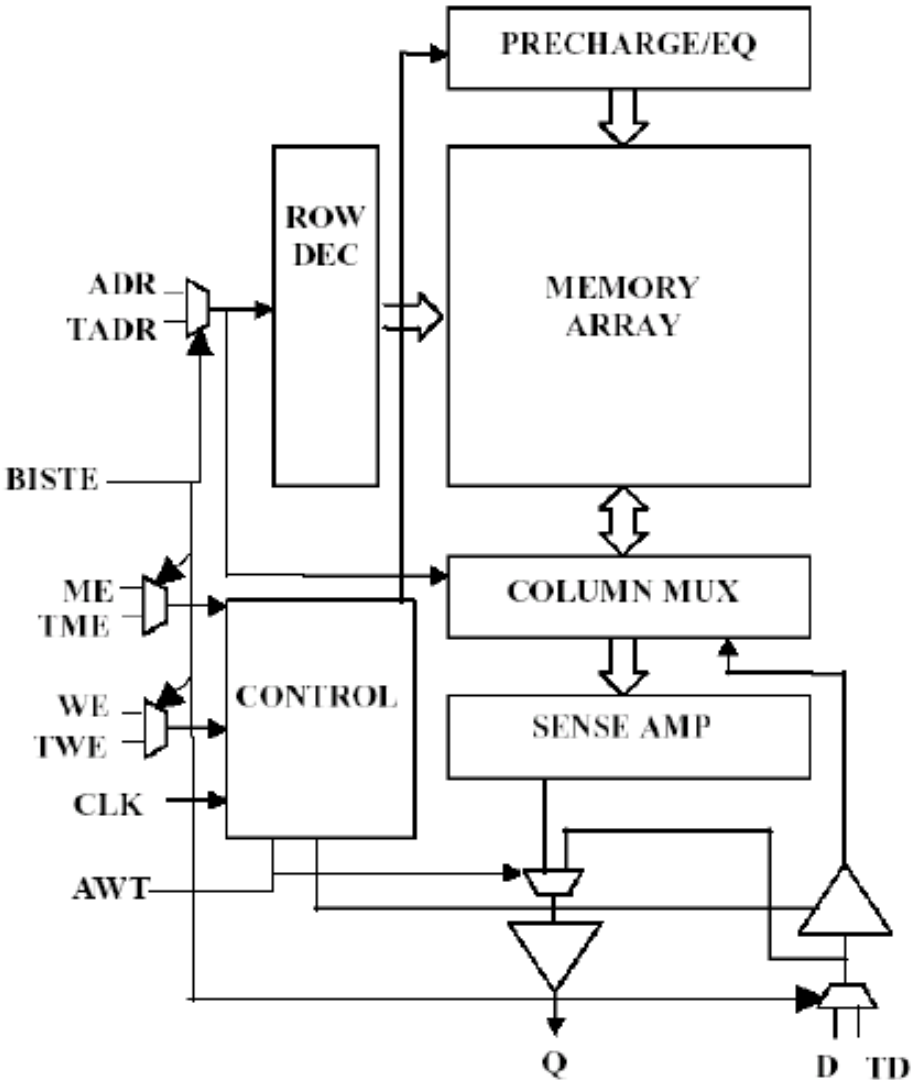
Figure 2-3 BIST Disabled Block Diagram for CM=4



2.3.3.3 BIST Enabled Block Diagram for CM=2

Figure 2-4 shows the block diagram for CM=2 when the BIST mode is enabled.

Figure 2-4 BIST Enabled Block Diagram for CM=2

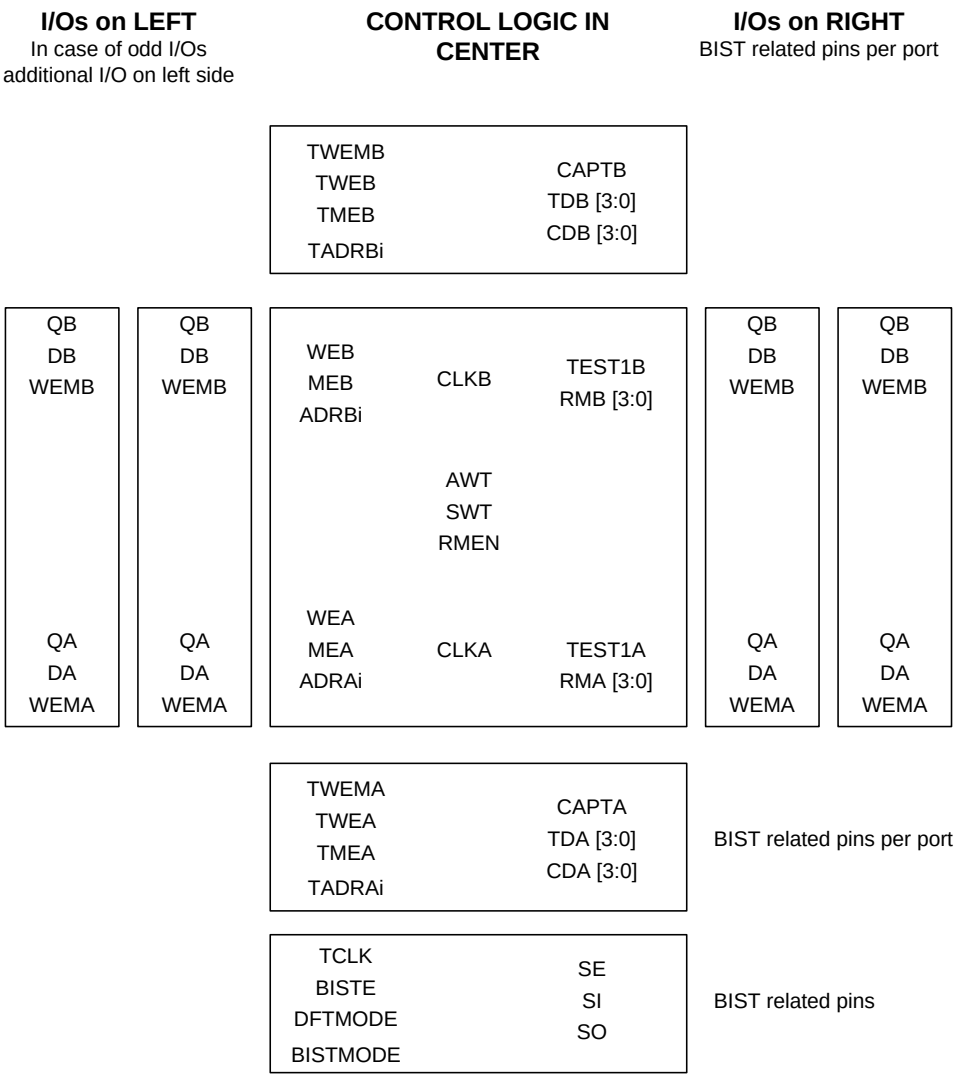


2.3.3.4 Pin Position

Figure 2-5 shows the positions of various pins in the SiWare-LT and SiWare-IT compilers.

> **Note** The BIST related pins shown in Figure 2-5 will only be present for SiWare-IT when **`bist_enable=TRUE`**.

Figure 2-5 Pin Position (SiWare-LT and SiWare-IT)



2.3.4 Functional Options

The *SiWare Single Port High Density Leakage Control Register File 32K Sync Compiler For Common Platform 65nm LPe LowK Periphery Mixed Vt/Cell High Vt Process* provides the following functional options:

- This compiler supports the configurations shown in Table 2-6. The flags **`bist_enable`** and **`low_leakage`** determine the selection of the configuration that is to be used.

Table 2-6 SiWare High-Density Memory Options

Configuration	Description	Parameters Required

SiWare-LT (default configuration)	ASAP (default configuration)	`redundancy_enable=FALSE`
		`bist_enable=FALSE`
		`low_leakage=FALSE`

SiWare-IT	ASAP with BIST	`redundancy_enable=FALSE`
		`bist_enable=TRUE`
		`low_leakage=FALSE`

SiWare-LT (with leakage control)	ASAP (with leakage control)	`redundancy_enable=FALSE`
		`bist_enable=FALSE`
		`low_leakage=TRUE`

SiWare-IT (with leakage control)	ASAP LC with BIST (with leakage control)	`redundancy_enable=FALSE`
		`bist_enable=TRUE`
		`low_leakage=TRUE`

- ME, WE, and WEM can be configured all active high or all active low.
- WEM [0:NB-1] input is optional sub-word write enable. One WEM signal is provided for every bit. (NB is total number of bits). It is enabled by setting **`wem_enable=TRUE`**, **`use_sw=yes`** and **`SW=1`** in the custom global file.
- AWT pin controls the asynchronous write through option. It is enabled when **`bist_enable=TRUE`**. SWT pin should be held low for the AWT pin to be functional.
- BISTE pin, AWT pin and test inputs (TADR, TD, TME, TWE, TWEM, and TCLK) are optional. These input pins will be generated only if bist is enabled by setting **`bist_enable=TRUE`** in the custom global file.

2.3.5 Functional Descriptions

2.3.5.1 Bit Write Mask

This memory includes the Sub Word feature where selective writes to individual I/O's can be done using the maskable write enable signals (WEM). Each I/O has its own WEM control signal that allows completely flexible masking capability. The WEM signals need to be tied together externally to support different sub-word sizes. TWEM is 1 bit and controlled by the SMS interface.

The SW option in the GLB file can remove the WEM/TWEM signals.

2.3.5.2 Test Modes, RM [3:0]

The memory function, when any of the test modes are enabled is explained below:

TEST1: Test1 disables the memory self-timed clock, and controls the memory with the external clock. Q will appear on the output after the falling edge of external clock when TEST1=TRUE.

RME: Read Margin Enable selects between the default RM setting, and the external pin RM setting. If RME is set low the default RM values will be applied to the memory.

RM[3:0]: There are four Read Margin RM[3:0] pins available in the Synopsys DesignWare embedded memories. Two of the pins, RM[1:0], are used to trade-off between speed and robustness (yield). The other two pins, RM[3:2], are used for test purposes. There is also a Read Margin Enable (RME) pin that selects between the internal default RM[2:0] value set during compilation, and the external, user provided RM[2:0] settings. It is required that external access to all RM pins, including RME, is provided for debug and yield analysis purposes. Registers can be used to access the RM pins for debug. If Synopsys' STAR Memory System is used, the RM pins will be automatically registered during compilation.

Table 2-7 Read Margin Control Pins

Signal	< >_custom.glb Setting	Description
RME	None, always enabled	Read Margin Enable pin. Selects between internal and external RM[2:0]* settings. RME = 0: Internal settings; RME = 1: External settings.
RME[3:0]	None, always enabled	RM[1:0] are used to change Read Margin settings. RM[3:2] are for Synopsys' test purposes.

Note * RM3 is not controlled by RME.

2.3.6 Compiler Range Information

Table 2-8 shows the range for the address, Number of Words (**NW**), Number of Bits (**NB**), Column Mux (**CM**) options, and bit size ranges for total instance size.

Table 2-8 Compiler Range Values

CM	Address Inputs Min	Address Inputs Max	NW Increment	NW Min	NW Max	NB Min	NB Max	Maximum Number of Bits
2	3	8	4	8	256	2	256	65536
4	4	9	8	16	512	2	128	65536

The Column Mux is an option that helps change the physical aspect ratio of the instance generated by the compiler. When you lower the Column Mux value, the number of selection levels (multiplexing) of instance I/O used is reduced.

If the instance has a high number of bits per word and a low number of words, use the lowest possible value for the Column Mux option to obtain a square aspect ratio. If the instance has a high number of words and a low number of bits per word, use the highest possible value Column Mux.

2.3.7 Metal Layer Usage

Figure 2-6 shows the metal layer usage in the compiler. Table 2-9 explains the routing instructions for various metal layers.

- Metal1, Metal2, and Metal3 layers are completely blocked.
- Metal layers 4 and above available for routing over the instance. Metal4 is mainly used for power routing, and can also be used for signal routing. In addition, the Metal4 direction is vertical.
- Internal metal layers used are Metal3 and Metal2. Metal3 is used horizontally for word lines, power, and control signals. Metal2 is used vertically for bit lines, pre-decoded X address lines, and local signals.
- The top thick metal layer is Metal6 and above.

Figure 2-6 Metal Layer Usage

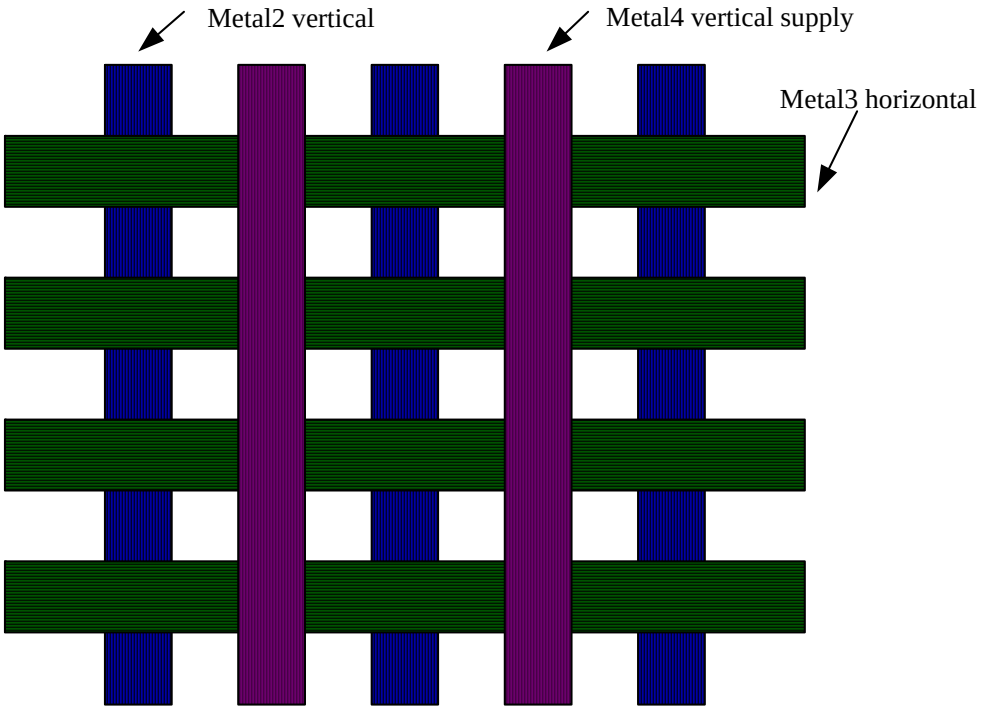


Table 2-9 Metal Layer Routing

	Routing Instructions		
	Single Bank		Multibank
Metal Layer	low_leakage=TRUE	low_leakage=FALSE	low_leakage=TRUE/FALSE
Metal layer availability	Metal1, Metal2, and Metal3 are completely blocked. Metal4 can be used for array_biasing.	Metal1, Metal2, and Metal3 are completely blocked. Metal4 used mainly for power routing.	Metal1, Metal2, and Metal3 are completely blocked. Metal4 is mainly used for power routing and some signal routing
Metal4 routing porosity	>40%, vertical	60%, vertical	>40%, vertical
Routing porosity for Metal5 and above (including the power mesh)	100%, freely	100%, freely	100%, freely
Thick metal supported	Metal6 and above	Metal6 and above	Metal6 and above

2.3.8 IP Tagging

Synopsys, Inc. labels its Intellectual Property (IP) with either the use of the IP marking layer or a VSIA tag layer, noted in the **.ltt** file. This GDSII layer identification is required to correctly label Synopsys' IP at the foundry.

It is imperative that customers include this layer, in the form **layer:datatype**, when ordering masks.

2.3.9 Physical Grids

The physical grids are:

- Routing grid: 0.20µm to 0.28µm
- Layout grid: 0.005µm

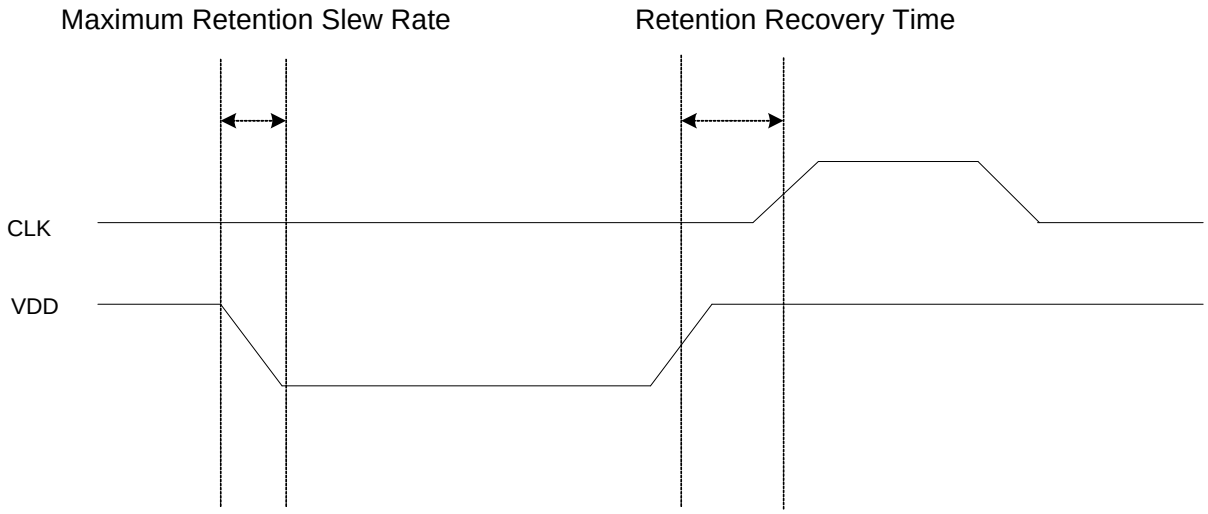
2.3.10 Data Retention

Retention can be measured with two components, namely:

- Maximum Retention Slew Rate which can be defined as the maximum rate at which Vdd may be raised and lowered.
- Retention Recovery Time which is the time the memory must be kept in quiescent state after Vdd returns to a normal operating range before functional operation may occur.

Figure 2-7 represent these components in a waveform.

Figure 2-7 Data Retention



The foundry will provide memory bit cells that are capable of reliably retaining their state to a minimum voltage not to exceed 0.7xVnom. Synopsys, Inc. will ensure that the memory compilers will support a quiescent operation of lowering the Vdd supply of the instance to 0.7xVnom and then raising the Vdd supply to normal operating range without disturbing the state of the bit cell. To ensure data retention, Vdd supply should be lowered only for instances compiled with the option **`low_leakage=FALSE`**.

Table 2-10 shows the Slew Rate and Recovery Time for the current compiler. Please note that these values represent the component for Worst Case only.

Table 2-10 Data Retention

Component Name	Value
Maximum Retention Slew Rate	620mV/10pS
Retention Recovery Time	Tcc at SS_1.08_125

2.3.11 Logic Truth Tables

2.3.11.1 Memory Function Truth Table

Note

Q-1: Remain the same state from previous cycle.
Q-2: Having the same state from two previous cycle.
Q+1: Output with one latency delay.
Q or Data-in: Output with no CLK latency.
Negedge(1->0) of RSCRST is necessary prior to start of normal memory operation (read/write).

Table 2-11 shows the memory function truth table for the SiWare-LT/SiWare-IT compilers.

Table 2-11 Memory Function Truth Table - SiWare-LT/SiWare-IT

Function	CLK	ME	WE	WEM	D	AWT	Q
Idle	L	X	X	X	X	L	Q-1
Disabled	H	L	X	X	X	X	Q-1
Read	H	H	L	X	X	L	Data-out
Write	H	H	H	H	Data-in	L	Q-1
Mask	H	H	H	L	X	L	Q-1

Note The status of test signals for the above truth table is TEST1=L.

2.3.11.2 BIST Mode Truth Table

Table 2-12 shows the truth table for BIST mode.

Table 2-12 BIST Mode Truth Table

Function	BISTE	Active Pins					
Normal mode	L	ME	WE	ADR	D	WEM	CLK
BIST mode	H	TME	TWE	TADR	TD	TWEM	TCLK

2.3.11.3 Test Mode Truth Table

Table 2-13 shows the truth table for TEST mode.

Table 2-13 Test Mode Truth Table

Function	TEST1	CLK
TEST1 Mode	H	H

2.3.11.4 Control Mux Architecture in AWT Mode Truth Table

Table 2-14 shows the logic truth table for control mux architecture in AWT mode.

Table 2-14 Control Mux Architecture in AWT Mode Truth Table

Function	AWT	BISTE	WE	ME*	ADR[n-2:0]*	ADR[n-1]*	QM
Normal	L	L	X	X	X	X	Q-1
ADR	H	L	L	L	L	ADR	L XOR ADR
ME	H	L	L	ME	L	L	L XOR ME
WE	H	L	WE	L	L	L	L XOR WE

2.3.11.5 I/O Mux Architecture in AWT Mode Truth Table

Table 2-15 shows the logic truth table for I/O mux architecture in AWT mode.

Table 2-15 I/O Mux Architecture in AWT Mode Truth Table

Function	AWT	BISTE	D[n]	WEM[n]	Q
Normal	L	L	X	X	Q-1
WEM[n]	H	L	L	WEM[n]	L XOR WEM[n]
D[n]	H	L	D[n]	L	L XOR D[n]

2.3.12 Hazard Information

NC - No Change
CCL - Corrupt Current Location
CEM - Corrupt Entire Memory

2.3.12.1 Hazard Information for Read/Write Cycle

Table 2-16 shows the Read/Write cycle hazard information for the compiler.

Table 2-16 Hazard Information for Read/Write Cycle

Mode	ME	WE	ADR	DI	Memory	Q
Read	High	Low	-	-	NC	Valid
Write	High	High	-	-	Data-In	Valid
Read	High	Low	-	Violation	NC	Valid
Write	High	High	-	Violation	CCL	NC
Read	High	Low	Violation	-	CEM	Q=X
Write	High	High	Violation	-	CEM	NC
Read	High	Low	Violation	Violation	CEM	Q=X
Write	High	High	Violation	Violation	CEM	NC
Read/write	High	Violation	-	-	CCL	Q=X
Read/write	High	Violation	-	Violation	CCL	Q=X
Read/write	High	Violation	Violation	-	CEM	Q=X
Read/write	High	Violation	Violation	Violation	CEM	Q=X
Read/write	Violation	-	-	-	CEM	NC
Read/write	Low	-	-	-	NC	Previous Dataout

2.3.12.2 Hazard Information for Clock Violations

Table 2-17 shows the clock violations hazard information for the compiler.

Table 2-17 Hazard Information for Clock Violations

Mode	Violation	Memory	Q
Read/Write	Clock Cycle Width	CEM	Q=X
Read/Write	Clock High Pulse Width	CEM	Q=X
Read/Write	Clock Low Pulse Width	CEM	Q=X

2.3.13 Waveform Diagrams

This section shows the various timing waveforms.

Note

If ME is High, it is necessary to ensure that the timing spec of each signal is kept with respect to the clock.
If ME is Low, it is not necessary to meet the timing spec of each signal.
These waveforms represent the case where all control signals (including ME, BISTE, and AWT) are active High.

Figure 2-8 shows the conventions used in the waveform diagrams.

Figure 2-8 Waveform Conventions

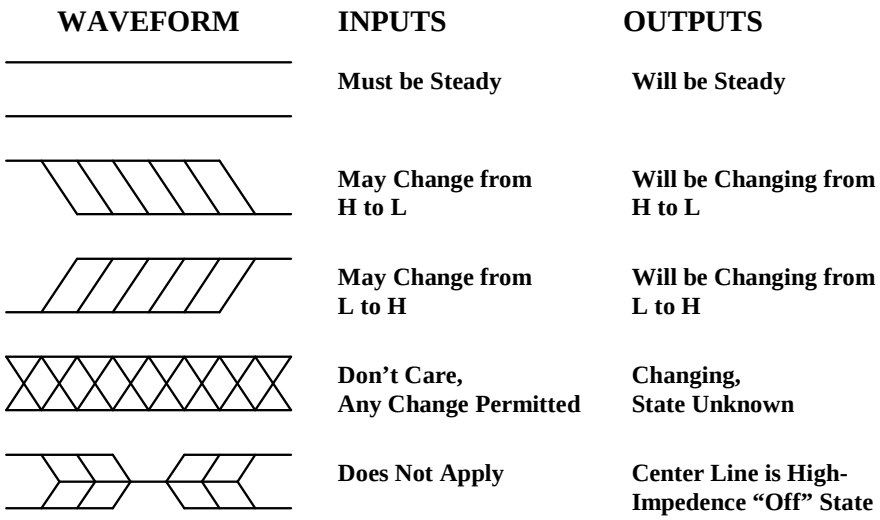


Figure 2-9 Read Cycle Timing

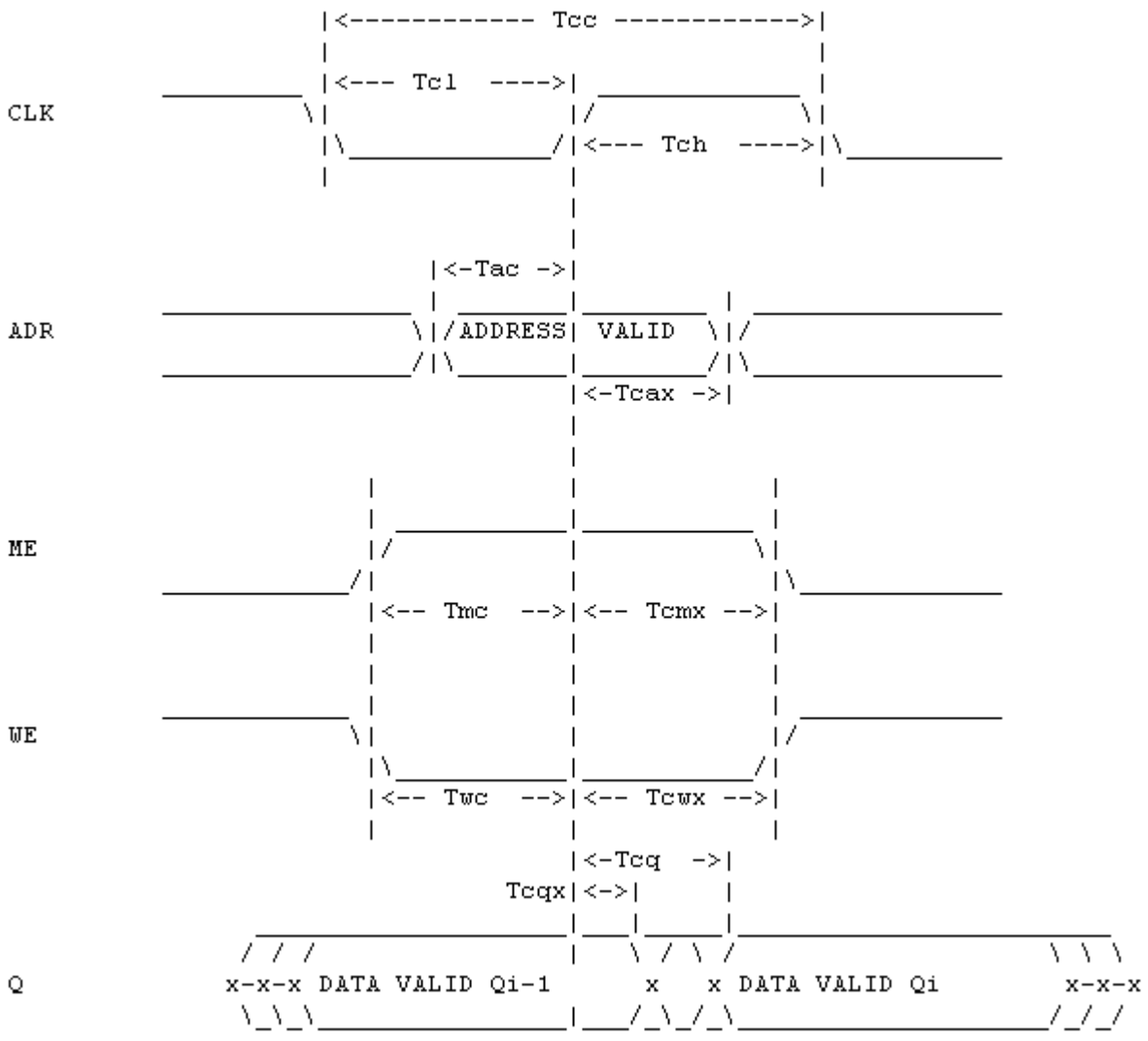


Figure 2-10 Write Cycle Timing

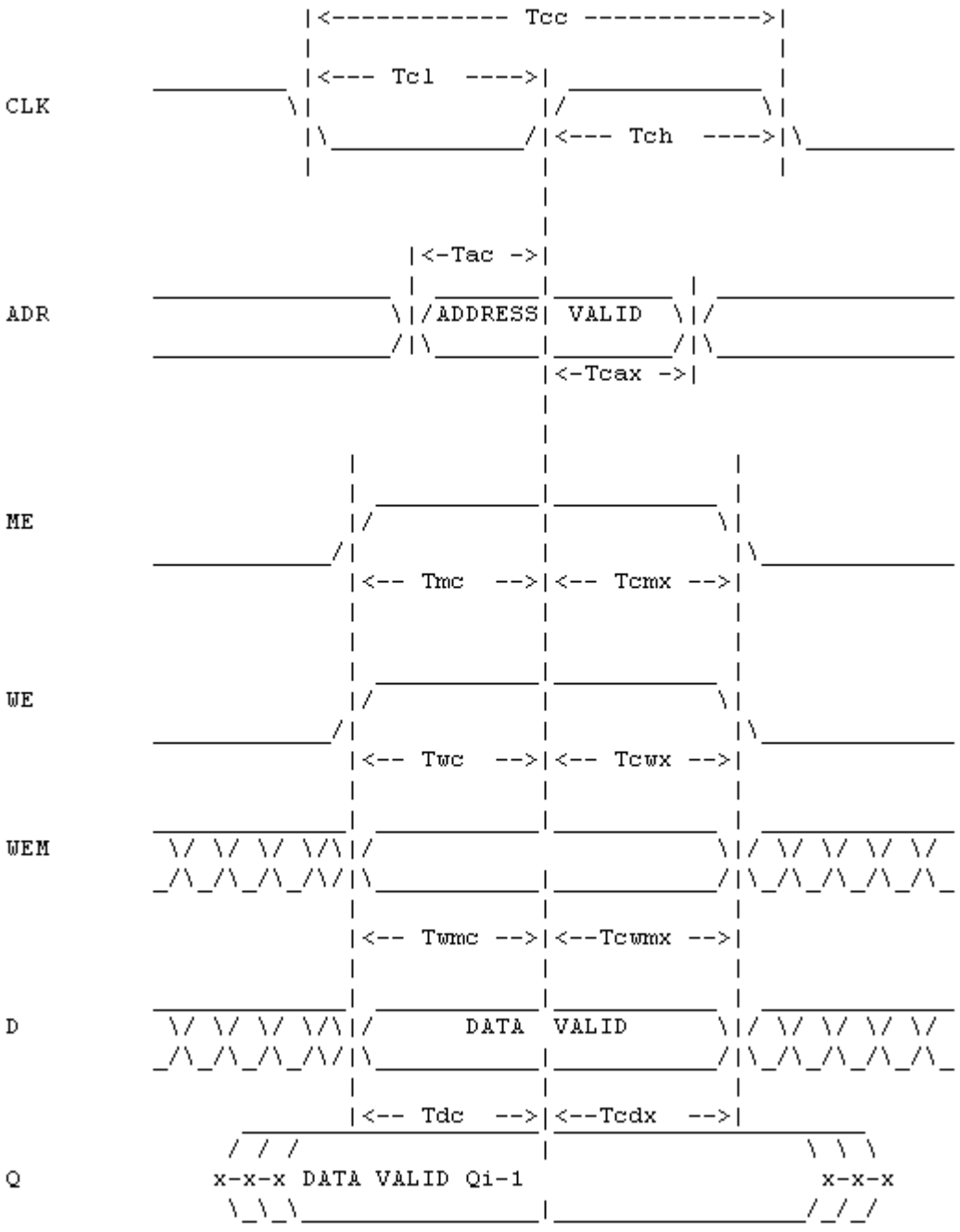


Figure 2-11 BIST Mode Timing

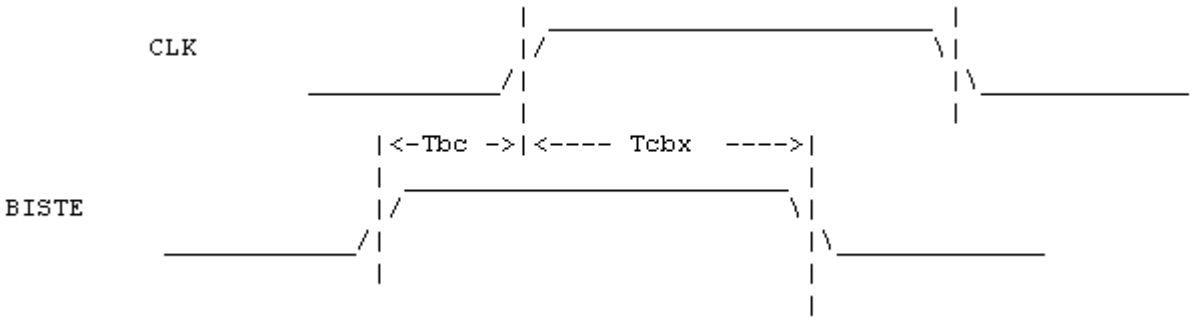


Figure 2-12 Asynchronous Write Through Timing

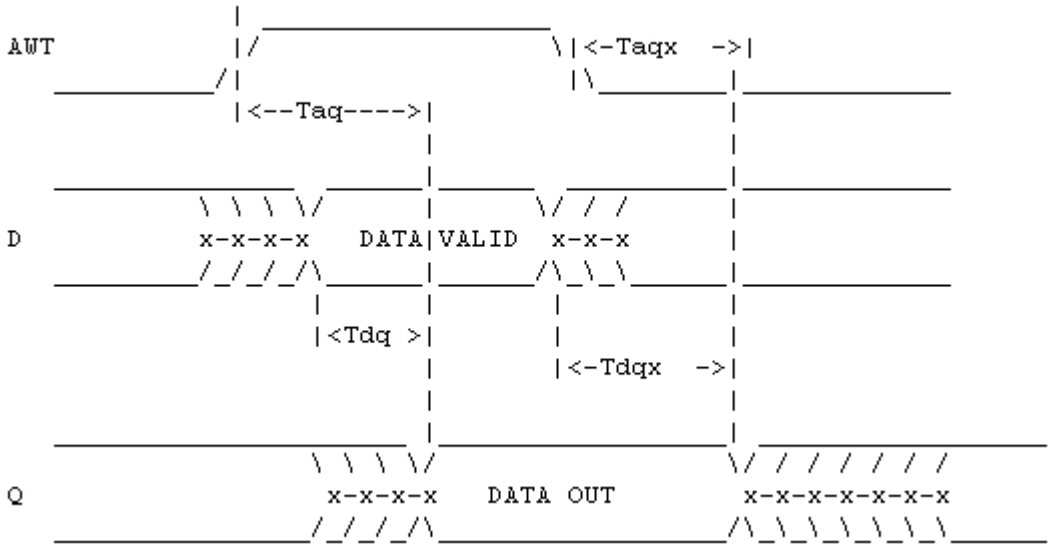


Figure 2-13 TEST1 Mode Timing

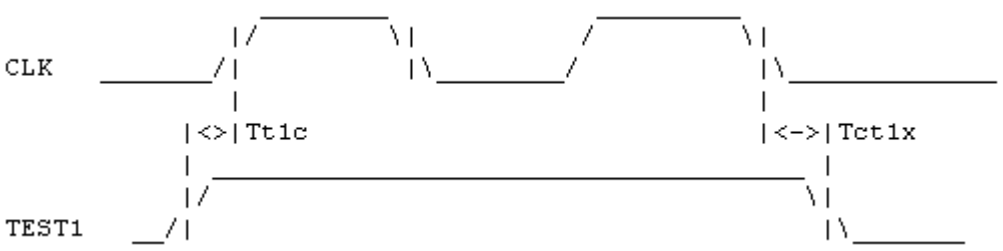
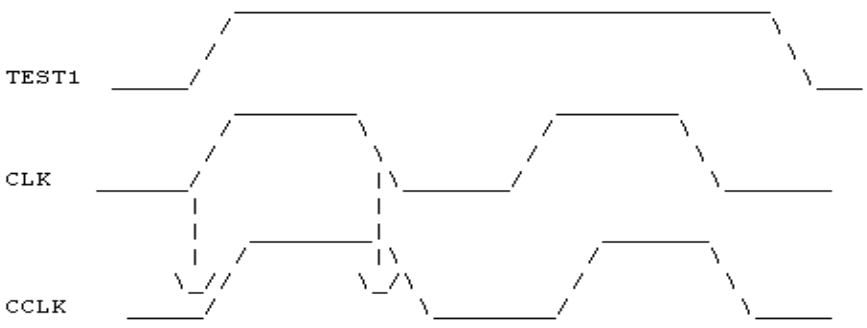


Figure 2-14 TEST1 Mode - Bypassing Read and Self Timed Circuits



- - Word Line active - Word line inactive
- - bit line discharged - bit line precharged
- - sense amp enabled - sense amp disabled
- - input latches close - input latches open
- - output latches open - output laches close

Note If the TEST1 signal is active, internal SRAM clocks will be controlled by the external clock instead of self timed circuits.

2.3.14 Internal Memory Area

Table 2-18 shows the estimated internal memory area for instance configuration specified in Table 2-21 on page 44. It shows the internal dimensions for x-axis, y-axis, and area for an instance with 256K bits.

Table 2-18 Internal Memory Area - 64x16CM4SW1BK1

Configuration	X-dim (µm)	Y-dim (µm)	Area (μm^2)
SiWare-LT Single Port High-Density	102.5	32.095	3290
SiWare-LT Single Port High-Density with Leakage Control	102.5	32.895	3372
SiWare-IT Single Port High-Density	102.5	34.42	3528
SiWare-IT Single Port High-Density with Leakage Control	102.5	35.22	3610

2.3.15 Timing Characterization

Timing tables are based on 5 input slew rates and 5 output loads. Path delays are modeled with 5x5 tables, based upon 5 output loads and 5 input slew rates. Setup and Hold timing is modeled with 5x5 tables, based upon 5 clock slew rates and 5 signal slew rates. Slew rates are measured from 30% to 70%, extrapolated to 10% to 90% of the power supply. All timing is measured from a logic threshold at 50% of the power supply. Timing is evaluated at three timing conditions to produce three timing libraries with worst, typical and best case timing.

2.3.16 Lookup Table (5x5)

Table 2-19 shows the variables of 5x5 lookup tables in the .lib files.

Table 2-19 Lookup Table (5x5)

Index	1	2	3	4	5
Input Slope (ns)	0.020	0.050	0.100	0.200	0.500
Output Load (pf)	0.005	0.020	0.050	0.100	0.250

2.3.17 Standard Operating Characterization Conditions

Table 2-20 shows the typical, best, and worst operating characterization conditions supported by this compiler. The tables in this document contain data for selected PVTs only. However, the data for all supported PVTs is available in the generated datasheets.

Table 2-20 Standard Operating Conditions

PVT Corner	Process	VDD (V)	Temperature (C)	Notes
tt1p2v25c (Default)	TT	1.2 (Vnom)	25	Typical Case Corner
ff1p32vn40c (Default)	FF	1.32 (Vnom +10%)	-40	Best Case Corner
ss1p08v125c (Default)	SS	1.08 (Vnom -10%)	125	Traditional Worst Case Corner
ss1p08vn40c (Default)	SS	1.08 (Vnom -10%)	-40	Temperature Inversion Corner
ff1p32v125c (Worst Case Leakage)	FFF	1.32 (Vnom +10%)	125	Leakage only
ff1p32vn55c (Foundry Preferred Corner)	FF	1.32 (Vnom +10%)	-55	Best Case Corner
ss1p08vn55c (Foundry Preferred Corner)	SS	1.08 (Vnom - 10%)	-55	Temperature Inversion Corner

2.3.18 Using Licensed Custom PVTs

Customers may license additional characterized PVTs, beyond the standard PVTs listed in "Standard Operating Characterization Conditions" on page 41, for the compiler.

Example 2-1 shows the PVT block from a custom GLB file. In order for instances to be generated with these PVTs, the custom GLB file will need to be edited to set the appropriate values for the variable "pvt_enable". For example, pvt_enable = {1 2 3 4 5 6 7} would generate data corresponding to **pvt1, pvt2, pvt3, pvt4,pvt5, pvt6** and **pvt7**.

Also, vddmin licensing is required to generate instances for **pvt8** and **pvt9**. In order for instances to be generated with these PVTs, the license file needs to contain the vddmin license statement. Refer to Chapter 6 of the Integrator Manual for steps to edit the custom GLB file.

Example 2-1 PVT List from Custom GLB

```
/*- PVT   DEFAULT     TYPE     RANGE     SMS-REQRMNT     DEFINITION ----------------------------------------------------*/
pvt1    = { T 1.20 25   tt1p2v25c     } /*string  Process; voltage; temperature and name for typical operating point */
pvt2    = { B 1.32 -40 ff1p32vn40c    } /*string  Process; voltage; temperature and name for typical operating point */
pvt3    = { W 1.08 125 ss1p08v125c    } /*string  Process; voltage; temperature and name for typical operating point */
pvt4    = { W 1.08 -40 ss1p08vn40c    } /*string  Process; voltage; temperature and name for typical operating point */
pvt5    = { FFF 1.32 125 ff1p32v125c } /*string  Process; voltage; temperature and name for typical operating point */
pvt6    = { B 1.32 -55 ff1p32vn55c    } /*string  Process; voltage; temperature and name for typical operating point */
pvt7    = { W 1.08 -55 ss1p08vn55c    } /*string  Process; voltage; temperature and name for typical operating point */
/* Note: the following 0.96v PVTs should be enabled with vddmin license only                    */
//pvt8 = { W 0.96 125 ss0p96v125c    } /*string  Process; voltage; temperature and name for typical operating point */
//pvt9 = { W 0.96 -40 ss0p96vn40c    } /*string  Process; voltage; temperature and name for typical operating point */
```

2.3.19 AC Characterization

The data in the tables in this section are specified with no additional load on the output pins. To obtain Tcq timing under a specified load (CL) use the following equation:

```
Tcq with load = Tcq + (Ktd * CL)
```

Here, the value of Ktd (Slope ns/pf in the extrinsic delay) is:

Description	low_leakage	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
Slope ns/pf in the extrinsic delay	FALSE	1.133	0.784	1.711	1.585	0.823	0.771	1.565
	TRUE	1.133	0.784	1.711	1.585	0.823	0.771	1.565

Memory Enable setup time and Address setup time in the tables have a minimum value regardless of PVT condition.

All timing numbers are in nanoseconds.

The AC Characterization tables for the different SiWare configurations are as follows:

- Table 2-22, "Read and Write Cycle Timing for SiWare-LT - 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=FALSE)"

All tables include the Read and Write cycle timing for the instance configuration specified in Table 2-21.

Table 2-21 Benchmark Instance Configuration Parameters

Instance Name	64x16CM4SW1BK1
Number of Words (**NW**)	64
Number of Bits (**NB**)	16
Column Mux (**CM**)	4
Subword (**SW**)	1
Timing Mode	DEFAULT

2.3.19.1 Read and Write Cycle Timings for SiWare-LT

Table 2-22 shows the AC characterization for the *SiWare-LT Single Port High-Density*.

Table 2-22 Read and Write Cycle Timing for SiWare-LT - 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=FALSE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
CLK Low Cycle Width	Tcl	Min	0.341	0.225	0.538	0.517	0.222	0.222	0.512
CLK High Cycle Width	Tch	Min	0.168	0.115	0.258	0.252	0.119	0.113	0.250
CLK Cycle Time(RME = 0)	Tcc	Min	0.789	0.509	1.304	1.328	0.517	0.501	1.324
CLK to Q Delay(RME = 0)	Tcq	Max	0.618	0.400	0.978	0.988	0.403	0.394	0.979
Q hold time after CLK rises (RME = 0)	Tcqx	Min	0.606	0.391	0.960	0.973	0.395	0.385	0.964
ADR setup time before CLK rises	Tac	Min	0.291	0.184	0.473	0.467	0.185	0.181	0.463
ADR hold time after CLK rises	Tcax	Min	0.097	0.066	0.149	0.143	0.072	0.065	0.142
D setup time before CLK rises	Tdc	Min	0.278	0.178	0.450	0.435	0.163	0.175	0.431
D hold time after CLK rises	Tcdx	Min	0.082	0.056	0.126	0.121	0.061	0.055	0.119
WE setup time before CLK rises	Twc	Min	0.341	0.225	0.538	0.517	0.222	0.222	0.512
WE hold time after CLK rises	Tcwx	Min	0.078	0.054	0.117	0.112	0.059	0.053	0.111
ME setup time before CLK rises	Tmc	Min	0.485	0.312	0.778	0.767	0.320	0.307	0.760
ME hold time after CLK rises	Tcmx	Min	0.000	0.000	0.000	0.000	0.000	0.000	0.000
WEM setup time before CLK rises	Twmc	Min	0.300	0.192	0.482	0.468	0.172	0.188	0.461

Table 2-22 Read and Write Cycle Timing for SiWare-LT - 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=FALSE)

Description	Symbol	Condition	tt1p2v25c	ss1p08v125c	ff1p32vn40c	ss1p08vn40c	ff1p32v125c	ff1p32vn55c	ss1p08vn55c
WEM hold time after CLK rises	Tcwmx	Min	0.085	0.057	0.132	0.127	0.062	0.056	0.126
TEST1 setup time before CLK rises	Tt1c	Min	0.341	0.225	0.538	0.517	0.222	0.222	0.512
TEST1 hold time after CLK falls	Tct1x	Min	0.789	0.509	1.304	1.328	0.517	0.501	1.324
RM setup time before CLK rises	Trmc	Min	0.306	0.193	0.495	0.489	0.176	0.190	0.486
RM hold time after CLK rises	Tcrmx	Min	0.789	0.509	1.304	1.328	0.517	0.501	1.324
RME setup time before CLK rises	Trmc	Min	0.306	0.193	0.495	0.489	0.176	0.190	0.486
RME hold time after CLK rises	Tcrmx	Min	0.789	0.509	1.304	1.328	0.517	0.501	1.324

2.3.19.2 Read and Write Cycle Timing Based on RME & RM Pins for SiWare-LT

Table 2-23 shows the AC characterization based on RME and RM pins for the *SiWare-LT Single Port High-Density*.

Table 2-23 Read/Write Cycle Timing Based on RME & RM for SiWare-LT - 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=FALSE)

Condition	Description	Condition	tt1p2v25c	ss1p08v125c	ff1p32vn40c	ss1p08vn40c	ff1p32v125c	ff1p32vn55c	ss1p08vn55c
RME = 1, RM[3:0] = 0011	CLK Cycle Time	Min	0.789	0.509	1.304	1.328	0.517	0.501	1.324
	CLK to Q Delay	Max	0.618	0.400	0.978	0.988	0.403	0.394	0.979
	Q hold time after CLK rises	Min	0.606	0.391	0.960	0.973	0.395	0.385	0.964
RME = 1, RM[3:0] = 0010	CLK Cycle Time	Min	0.789	0.509	1.304	1.328	0.517	0.501	1.324
	CLK to Q Delay	Max	0.618	0.400	0.978	0.988	0.403	0.394	0.979
	Q hold time after CLK rises	Min	0.606	0.391	0.960	0.973	0.395	0.385	0.964
RME = 1, RM[3:0] = 0001	CLK Cycle Time	Min	1.146	0.759	1.777	1.719	0.778	0.744	1.701
	CLK to Q Delay	Max	1.024	0.664	1.616	1.612	0.664	0.652	1.600
	Q hold time after CLK rises	Min	1.012	0.656	1.598	1.596	0.655	0.644	1.585
RME = 1, RM[3:0] = 0000	CLK Cycle Time	Min	1.147	0.758	1.779	1.718	0.778	0.744	1.701
	CLK to Q Delay	Max	1.025	0.664	1.618	1.611	0.664	0.652	1.600
	Q hold time after CLK rises	Min	1.013	0.655	1.599	1.596	0.655	0.644	1.585

2.3.19.3 Read and Write Cycle Timings for SiWare-LT with Leakage Control

Table 2-24 shows the AC characterization for the *SiWare-LT Single Port High-Density with Leakage Control*.

Table 2-24 Read and Write Cycle Timing for SiWare-LT - 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=TRUE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
CLK Low Cycle Width	Tcl	Min	0.464	0.286	0.749	0.817	0.269	0.281	0.821
CLK High Cycle Width	Tch	Min	0.170	0.116	0.260	0.255	0.120	0.114	0.252
CLK Cycle Time(RME = 0)	Tcc	Min	0.850	0.551	1.401	1.410	0.562	0.542	1.405
CLK to Q Delay(RME = 0)	Tcq	Max	0.631	0.408	0.992	1.001	0.411	0.402	0.995
Q hold time after CLK rises (RME = 0)	Tcqx	Min	0.617	0.400	0.974	0.984	0.401	0.393	0.979
ADR setup time before CLK rises	Tac	Min	0.329	0.201	0.540	0.582	0.202	0.198	0.591
ADR hold time after CLK rises	Tcax	Min	0.101	0.068	0.154	0.148	0.075	0.067	0.146
D setup time before CLK rises	Tdc	Min	0.399	0.239	0.669	0.772	0.207	0.236	0.784
D hold time after CLK rises	Tcdx	Min	0.113	0.072	0.178	0.199	0.075	0.071	0.201
WE setup time before CLK rises	Twc	Min	0.464	0.286	0.749	0.817	0.269	0.281	0.821
WE hold time after CLK rises	Tcwx	Min	0.081	0.056	0.123	0.116	0.062	0.056	0.115
ME setup time before CLK rises	Tmc	Min	0.518	0.326	0.837	0.873	0.333	0.321	0.880
ME hold time after CLK rises	Tcmx	Min	0.000	0.000	0.000	0.000	0.000	0.000	0.000
WEM setup time before CLK rises	Twmc	Min	0.436	0.258	0.720	0.808	0.223	0.253	0.818
WEM hold time after CLK rises	Tcwmx	Min	0.115	0.073	0.182	0.205	0.076	0.072	0.207
TEST1 setup time before CLK rises	Tt1c	Min	0.464	0.286	0.749	0.817	0.269	0.281	0.821
TEST1 hold time after CLK falls	Tct1x	Min	0.850	0.551	1.401	1.410	0.562	0.542	1.405
RM setup time before CLK rises	Trmc	Min	0.300	0.189	0.487	0.482	0.171	0.186	0.479
RM hold time after CLK rises	Tcrmx	Min	0.850	0.551	1.401	1.410	0.562	0.542	1.405

Table 2-24 Read and Write Cycle Timing for SiWare-LT - 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=TRUE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
RME setup time before CLK rises	Trmc	Min	0.300	0.189	0.487	0.482	0.171	0.186	0.479
RME hold time after CLK rises	Tcrmx	Min	0.850	0.551	1.401	1.410	0.562	0.542	1.405

2.3.19.4 Read and Write Cycle Timing Based on RME & RM Pins for SiWare-LT

Table 2-25 shows the AC characterization based on RME and RM pins for the *SiWare-LT Single Port High-Density with Leakage Control*.

Table 2-25 Read and Write Cycle Timing Based on RME and RM for SiWare-LT - 64x16CM4SW1BK1 (bist_enable=FALSE, low_leakage=TRUE)

Condition	Description	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
RME = 1, RM[3:0] = 0011	CLK Cycle Time	Min	0.850	0.551	1.401	1.409	0.562	0.542	1.405
	CLK to Q Delay	Max	0.631	0.408	0.992	1.001	0.411	0.402	0.995
	Q hold time after CLK rises	Min	0.617	0.400	0.974	0.984	0.401	0.393	0.979
RME = 1, RM[3:0] = 0010	CLK Cycle Time	Min	0.850	0.551	1.401	1.410	0.562	0.542	1.405
	CLK to Q Delay	Max	0.631	0.408	0.992	1.001	0.411	0.402	0.995
	Q hold time after CLK rises	Min	0.617	0.400	0.974	0.984	0.401	0.393	0.979
RME = 1, RM[3:0] = 0001	CLK Cycle Time	Min	1.142	0.756	1.771	1.741	0.774	0.742	1.727
	CLK to Q Delay	Max	1.037	0.672	1.633	1.627	0.673	0.661	1.616
	Q hold time after CLK rises	Min	1.023	0.664	1.615	1.610	0.663	0.652	1.600
RME = 1, RM[3:0] = 0000	CLK Cycle Time	Min	1.142	0.756	1.773	1.739	0.775	0.742	1.724
	CLK to Q Delay	Max	1.037	0.673	1.634	1.627	0.673	0.661	1.615
	Q hold time after CLK rises	Min	1.024	0.664	1.616	1.610	0.663	0.653	1.599

2.3.19.5 Read and Write Cycle Timings for SiWare-IT

Table 2-26 shows the AC characterization for the *SiWare-IT Single Port High-Density.*

Table 2-26 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=FALSE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
CLK Low Cycle Width	Tcl	Min	0.432	0.281	0.681	0.663	0.278	0.277	0.657
CLK High Cycle Width	Tch	Min	0.334	0.218	0.530	0.524	0.221	0.215	0.521
CLK Cycle Time(RME = 0)	Tcc	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
TCLK Low Cycle Width	Tcl	Min	0.432	0.281	0.681	0.663	0.278	0.277	0.657
TCLK High Cycle Width	Tch	Min	0.334	0.218	0.530	0.524	0.221	0.215	0.521
TCLK Cycle Time(RME = 0)	Tcc	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
CLK to Q Delay(RME = 0)	Tcq	Max	0.636	0.409	1.013	1.023	0.417	0.403	1.013
Q hold time after CLK rises (RME = 0)	Tcqx	Min	0.621	0.399	0.989	1.002	0.406	0.392	0.993
TCLK to Q Delay(RME = 0)	Tcq	Max	0.636	0.409	1.013	1.023	0.417	0.403	1.013
Q hold time after TCLK rises (RME = 0)	Tcqx	Min	0.621	0.399	0.989	1.002	0.406	0.392	0.993
D to Q Delay	Tdq	Max	0.330	0.208	0.534	0.539	0.202	0.205	0.537
Q hold time after D High/Low	Tdqx	Min	0.299	0.189	0.486	0.496	0.178	0.186	0.495
AWT to Q Delay	Taq	Max	0.231	0.157	0.351	0.348	0.166	0.155	0.346
Q hold time after AWT High/Low	Taqx	Min	0.101	0.072	0.152	0.145	0.076	0.071	0.143
WEM to Q Delay	Tdq	Max	0.330	0.208	0.534	0.539	0.202	0.205	0.537
TD to Q Delay	Tdq	Max	0.330	0.208	0.534	0.539	0.202	0.205	0.537
Q hold time after TD High/Low	Tdqx	Min	0.299	0.189	0.486	0.496	0.178	0.186	0.495
TWEM to Q Delay	Tdq	Max	0.330	0.208	0.534	0.539	0.202	0.205	0.537
BISTE to Q Delay	Tbq	Max	0.315	0.216	0.474	0.469	0.228	0.213	0.466
Q hold time after BISTE High/Low	Tbqx	Min	0.127	0.091	0.190	0.178	0.100	0.090	0.176
AWT to QM Delay	Taqm	Max	0.077	0.053	0.117	0.121	0.049	0.052	0.121
WE to QM Delay	Tmxqm	Max	0.511	0.330	0.809	0.827	0.321	0.326	0.824

Table 2-26 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=FALSE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
TWE to QM Delay	Tmxqm	Max	0.511	0.330	0.809	0.827	0.321	0.326	0.824
BISTE to QM Delay	Tbqm	Max	0.511	0.330	0.809	0.827	0.321	0.326	0.824
ME to QM Delay	Tmxqm	Max	0.511	0.330	0.809	0.827	0.321	0.326	0.824
ADR to QM Delay	Tmxqm	Max	0.511	0.330	0.809	0.827	0.321	0.326	0.824
TME to QM Delay	Tmxqm	Max	0.511	0.330	0.809	0.827	0.321	0.326	0.824
TADR to QM Delay	Tmxqm	Max	0.511	0.330	0.809	0.827	0.321	0.326	0.824
ADR setup time before CLK rises	Tac	Min	0.317	0.200	0.515	0.504	0.203	0.197	0.499
ADR hold time after CLK rises	Tcax	Min	0.089	0.061	0.135	0.130	0.066	0.060	0.130
D setup time before CLK rises	Tdc	Min	0.369	0.232	0.602	0.599	0.211	0.228	0.600
D hold time after CLK rises	Tcdx	Min	0.000	0.006	0.000	0.000	0.017	0.006	0.000
WE setup time before CLK rises	Twc	Min	0.432	0.281	0.681	0.663	0.278	0.277	0.657
WE hold time after CLK rises	Tcwx	Min	0.007	0.009	0.000	0.000	0.014	0.009	0.000
ME setup time before CLK rises	Tmc	Min	0.575	0.369	0.925	0.905	0.378	0.363	0.897
ME hold time after CLK rises	Tcmx	Min	0.000	0.000	0.000	0.000	0.000	0.000	0.000
WEM setup time before CLK rises	Twmc	Min	0.371	0.237	0.594	0.579	0.213	0.233	0.572
WEM hold time after CLK rises	Tcwmx	Min	0.026	0.021	0.034	0.030	0.031	0.021	0.030
TADR setup time before TCLK rises	Tac	Min	0.317	0.200	0.515	0.504	0.203	0.197	0.499
TADR hold time after TCLK rises	Tcax	Min	0.089	0.061	0.135	0.130	0.066	0.060	0.130
TD setup time before TCLK rises	Tdc	Min	0.369	0.232	0.602	0.599	0.211	0.228	0.600
TD hold time after TCLK rises	Tcdx	Min	0.000	0.006	0.000	0.000	0.017	0.006	0.000
TWE setup time before TCLK rises	Twc	Min	0.432	0.281	0.681	0.663	0.278	0.277	0.657

Table 2-26 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=FALSE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
TWE hold time after TCLK rises	Tcwx	Min	0.007	0.009	0.000	0.000	0.014	0.009	0.000
TME setup time before TCLK rises	Tmc	Min	0.575	0.369	0.925	0.905	0.378	0.363	0.897
TME hold time after TCLK rises	Tcmx	Min	0.000	0.000	0.000	0.000	0.000	0.000	0.000
BISTE setup time before CLK rises	Tbc	Min	0.663	0.434	1.047	1.026	0.448	0.427	1.018
BISTE setup time before TCLK rises	Tbc	Min	0.663	0.434	1.047	1.026	0.448	0.427	1.018
BISTE hold time after CLK falls	Tcbx	Min	0.089	0.061	0.135	0.130	0.066	0.060	0.130
BISTE hold time after TCLK falls	Tcbx	Min	0.089	0.061	0.135	0.130	0.066	0.060	0.130
TWEM setup time before TCLK rises	Twmc	Min	0.371	0.237	0.594	0.579	0.213	0.233	0.572
TWEM hold time after TCLK rises	Tcwmx	Min	0.026	0.021	0.034	0.030	0.031	0.021	0.030
TEST1 setup time before CLK rises	Tt1c	Min	0.432	0.281	0.681	0.663	0.278	0.277	0.657
TEST1 setup time before TCLK rises	Tt1c	Min	0.432	0.281	0.681	0.663	0.278	0.277	0.657
TEST1 hold time after CLK falls	Tct1x	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
TEST1 hold time after TCLK falls	Tct1x	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
RM setup time before CLK rises	Trmc	Min	0.294	0.187	0.473	0.467	0.169	0.184	0.464
RM setup time before TCLK rises	Trmc	Min	0.294	0.187	0.473	0.467	0.169	0.184	0.464
RM hold time after CLK rises	Tcrmx	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
RM hold time after TCLK rises	Tcrmx	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316

Table 2-26 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=FALSE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
RME setup time before CLK rises	Trmc	Min	0.294	0.187	0.473	0.467	0.169	0.184	0.464
RME setup time before TCLK rises	Trmc	Min	0.294	0.187	0.473	0.467	0.169	0.184	0.464
RME hold time after CLK rises	Tcrmx	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
RME hold time after TCLK rises	Tcrmx	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316

2.3.19.6 Read and Write Cycle Timing Based on RME & RM Pins for SiWare-IT

Table 2-27 shows the AC characterization based on RME and RM pins for the *SiWare-IT Single Port High-Density*.

Table 2-27 Read/Write Cycle Timing Based on RME & RM for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=FALSE)

Condition	Description	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
RME = 1, RM[3:0] = 0011	CLK Cycle Time	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
	CLK to Q Delay	Max	0.636	0.409	1.013	1.023	0.417	0.403	1.013
	Q hold time after CLK rises	Min	0.621	0.399	0.989	1.002	0.406	0.392	0.993
RME = 1, RM[3:0] = 0010	CLK Cycle Time	Min	0.785	0.507	1.295	1.320	0.512	0.499	1.316
	CLK to Q Delay	Max	0.636	0.409	1.013	1.023	0.417	0.403	1.013
	Q hold time after CLK rises	Min	0.621	0.399	0.989	1.002	0.406	0.392	0.993
RME = 1, RM[3:0] = 0001	CLK Cycle Time	Min	1.134	0.752	1.755	1.695	0.771	0.737	1.678
	CLK to Q Delay	Max	1.043	0.674	1.651	1.646	0.678	0.661	1.634
	Q hold time after CLK rises	Min	1.027	0.664	1.627	1.626	0.667	0.651	1.614
RME = 1, RM[3:0] = 0000	CLK Cycle Time	Min	1.134	0.751	1.756	1.694	0.771	0.737	1.677
	CLK to Q Delay	Max	1.043	0.674	1.653	1.645	0.678	0.661	1.633
	Q hold time after CLK rises	Min	1.028	0.663	1.629	1.625	0.667	0.651	1.614

2.3.19.7 Read and Write Cycle Timings for SiWare-IT

Table 2-28 shows the AC characterization for the *SiWare-IT Single Port High-Density with Leakage Control*.

Table 2-28 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=TRUE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
CLK Low Cycle Width	Tcl	Min	0.554	0.342	0.919	1.094	0.326	0.337	1.118
CLK High Cycle Width	Tch	Min	0.335	0.219	0.531	0.525	0.222	0.215	0.522
CLK Cycle Time(RME = 0)	Tcc	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
TCLK Low Cycle Width	Tcl	Min	0.554	0.342	0.919	1.094	0.326	0.337	1.118
TCLK High Cycle Width	Tch	Min	0.335	0.219	0.531	0.525	0.222	0.215	0.522
TCLK Cycle Time(RME = 0)	Tcc	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
CLK to Q Delay(RME = 0)	Tcq	Max	0.647	0.416	1.024	1.033	0.423	0.410	1.029
Q hold time after CLK rises (RME = 0)	Tcqx	Min	0.629	0.405	1.000	1.011	0.410	0.399	1.008
TCLK to Q Delay(RME = 0)	Tcq	Max	0.647	0.416	1.024	1.033	0.423	0.410	1.029
Q hold time after TCLK rises (RME = 0)	Tcqx	Min	0.629	0.405	1.000	1.011	0.410	0.399	1.008
D to Q Delay	Tdq	Max	0.522	0.305	0.881	1.049	0.281	0.301	1.072
Q hold time after D High/Low	Tdqx	Min	0.470	0.270	0.810	0.888	0.244	0.265	0.891
AWT to Q Delay	Taq	Max	0.355	0.229	0.561	0.588	0.254	0.225	0.590
Q hold time after AWT High/Low	Taqx	Min	0.142	0.097	0.231	0.215	0.107	0.095	0.213
WEM to Q Delay	Tdq	Max	0.522	0.305	0.881	1.049	0.281	0.301	1.072
TD to Q Delay	Tdq	Max	0.522	0.305	0.881	1.049	0.281	0.301	1.072
Q hold time after TD High/Low	Tdqx	Min	0.470	0.270	0.810	0.888	0.244	0.265	0.891
TWEM to Q Delay	Tdq	Max	0.522	0.305	0.881	1.049	0.281	0.301	1.072
BISTE to Q Delay	Tbq	Max	0.508	0.325	0.800	0.852	0.361	0.320	0.856
Q hold time after BISTE High/Low	Tbqx	Min	0.184	0.125	0.299	0.272	0.142	0.123	0.269
AWT to QM Delay	Taqm	Max	0.149	0.092	0.230	0.280	0.091	0.090	0.286
WE to QM Delay	Tmxqm	Max	0.662	0.410	1.052	1.178	0.402	0.404	1.189

Table 2-28 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=TRUE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
TWE to QM Delay	Tmxqm	Max	0.662	0.410	1.052	1.178	0.402	0.404	1.189
BISTE to QM Delay	Tbqm	Max	0.662	0.410	1.052	1.178	0.402	0.404	1.189
ME to QM Delay	Tmxqm	Max	0.662	0.410	1.052	1.178	0.402	0.404	1.189
ADR to QM Delay	Tmxqm	Max	0.662	0.410	1.052	1.178	0.402	0.404	1.189
TME to QM Delay	Tmxqm	Max	0.662	0.410	1.052	1.178	0.402	0.404	1.189
TADR to QM Delay	Tmxqm	Max	0.662	0.410	1.052	1.178	0.402	0.404	1.189
ADR setup time before CLK rises	Tac	Min	0.352	0.217	0.579	0.616	0.219	0.213	0.625
ADR hold time after CLK rises	Tcax	Min	0.093	0.064	0.141	0.136	0.069	0.063	0.135
D setup time before CLK rises	Tdc	Min	0.533	0.310	0.919	1.094	0.271	0.305	1.118
D hold time after CLK rises	Tcdx	Min	0.000	0.005	0.000	0.000	0.014	0.005	0.000
WE setup time before CLK rises	Twc	Min	0.554	0.342	0.893	0.966	0.326	0.337	0.971
WE hold time after CLK rises	Tcwx	Min	0.011	0.012	0.006	0.004	0.017	0.012	0.004
ME setup time before CLK rises	Tmc	Min	0.606	0.383	0.980	1.010	0.391	0.376	1.015
ME hold time after CLK rises	Tcmx	Min	0.000	0.000	0.000	0.000	0.000	0.000	0.000
WEM setup time before CLK rises	Twmc	Min	0.541	0.319	0.888	1.014	0.278	0.315	1.031
WEM hold time after CLK rises	Tcwmx	Min	0.031	0.026	0.022	0.047	0.034	0.026	0.052
TADR setup time before TCLK rises	Tac	Min	0.352	0.217	0.579	0.616	0.219	0.213	0.625
TADR hold time after TCLK rises	Tcax	Min	0.093	0.064	0.141	0.136	0.069	0.063	0.135
TD setup time before TCLK rises	Tdc	Min	0.533	0.310	0.919	1.094	0.271	0.305	1.118
TD hold time after TCLK rises	Tcdx	Min	0.000	0.005	0.000	0.000	0.014	0.005	0.000
TWE setup time before TCLK rises	Twc	Min	0.554	0.342	0.893	0.966	0.326	0.337	0.971

Table 2-28 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=TRUE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
TWE hold time after TCLK rises	Tcwx	Min	0.011	0.012	0.006	0.004	0.017	0.012	0.004
TME setup time before TCLK rises	Tmc	Min	0.606	0.383	0.980	1.010	0.391	0.376	1.015
TME hold time after TCLK rises	Tcmx	Min	0.000	0.000	0.000	0.000	0.000	0.000	0.000
BISTE setup time before CLK rises	Tbc	Min	0.754	0.480	1.204	1.433	0.503	0.472	1.465
BISTE setup time before TCLK rises	Tbc	Min	0.754	0.480	1.204	1.433	0.503	0.472	1.465
BISTE hold time after CLK falls	Tcbx	Min	0.093	0.064	0.141	0.156	0.069	0.063	0.176
BISTE hold time after TCLK falls	Tcbx	Min	0.093	0.064	0.141	0.156	0.069	0.063	0.176
TWEM setup time before TCLK rises	Twmc	Min	0.541	0.319	0.888	1.014	0.278	0.315	1.031
TWEM hold time after TCLK rises	Tcwmx	Min	0.031	0.026	0.022	0.047	0.034	0.026	0.052
TEST1 setup time before CLK rises	Tt1c	Min	0.554	0.342	0.919	1.094	0.326	0.337	1.118
TEST1 setup time before TCLK rises	Tt1c	Min	0.554	0.342	0.919	1.094	0.326	0.337	1.118
TEST1 hold time after CLK falls	Tct1x	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
TEST1 hold time after TCLK falls	Tct1x	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
RM setup time before CLK rises	Trmc	Min	0.289	0.183	0.466	0.460	0.165	0.180	0.458
RM setup time before TCLK rises	Trmc	Min	0.289	0.183	0.466	0.460	0.165	0.180	0.458
RM hold time after CLK rises	Tcrmx	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
RM hold time after TCLK rises	Tcrmx	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642

Table 2-28 Read and Write Cycle Timing for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=TRUE)

Description	Symbol	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
RME setup time before CLK rises	Trmc	Min	0.289	0.183	0.466	0.460	0.165	0.180	0.458
RME setup time before TCLK rises	Trmc	Min	0.289	0.183	0.466	0.460	0.165	0.180	0.458
RME hold time after CLK rises	Tcrmx	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
RME hold time after TCLK rises	Tcrmx	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642

2.3.19.8 Read and Write Cycle Timing Based on RME & RM Pins for SiWare-IT

Table 2-29 shows the AC characterization based on RME and RM pins for the *SiWare-IT Single Port High-Density with Leakage Control*

Table 2-29 Read and Write Cycle Timing Based on RME and RM for SiWare-IT - 64x16CM4SW1BK1 (bist_enable=TRUE, low_leakage=TRUE)

Condition	Description	Condition	tt1p2v 25c	ss1p08v 125c	ff1p32v n40c	ss1p08v n40c	ff1p32v 125c	ff1p32v n55c	ss1p08v n55c
RME = 1, RM[3:0] = 0011	CLK Cycle Time	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
	CLK to Q Delay	Max	0.647	0.416	1.024	1.033	0.423	0.410	1.028
	Q hold time after CLK rises	Min	0.629	0.405	1.000	1.011	0.410	0.399	1.007
RME = 1, RM[3:0] = 0010	CLK Cycle Time	Min	0.891	0.563	1.453	1.621	0.553	0.554	1.642
	CLK to Q Delay	Max	0.647	0.416	1.024	1.033	0.423	0.410	1.029
	Q hold time after CLK rises	Min	0.629	0.405	1.000	1.011	0.410	0.399	1.008
RME = 1, RM[3:0] = 0001	CLK Cycle Time	Min	1.129	0.748	1.747	1.716	0.766	0.735	1.704
	CLK to Q Delay	Max	1.053	0.680	1.665	1.660	0.685	0.669	1.649
	Q hold time after CLK rises	Min	1.035	0.669	1.641	1.638	0.672	0.658	1.628
RME = 1, RM[3:0] = 0000	CLK Cycle Time	Min	1.129	0.748	1.749	1.714	0.766	0.735	1.701
	CLK to Q Delay	Max	1.053	0.681	1.666	1.659	0.685	0.669	1.649
	Q hold time after CLK rises	Min	1.036	0.670	1.642	1.637	0.672	0.658	1.627

2.3.20 Intrinsic Capacitance Information

Table 2-30 shows the sum of nwell capacitance and non-switching capacitance for the instance configuration specified in Table 2-21 on page 44

Table 2-30 Intrinsic Capacitance Information

PVT	Capacitance (pf)
tt1p2v25c (Default)	1.4336
ff1p32vn40c (Default)	1.4336
ss1p08v125c (Default)	1.4336
ss1p08vn40c (Default)	1.4336
ff1p32v125c (Worst Case Leakage)	1.4336
ff1p32vn55c (Foundry Preferred Corner)	1.4336
ss1p08vn55c (Foundry Preferred Corner)	1.4336

2.3.21 Peak Current Information

The tables in this section show time-current pairs for the peak current at corresponding PVT with the time of occurrence during consecutive Read/Write cycles for the instance configuration specified in Table 2-21 on page 44.

Table 2-31 Peak Current (PWL) for SiWare-LT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = FALSE)

tt1p2v25c		ss1p08v125c		ff1p32vn40c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000
0.048580	0.000000	0.068327	0.000000	0.065588	0.000000	0.069286	0.000000	0.065753	0.000000	0.067721	0.000000	0.069000	0.000000
0.063272	6.007139	0.077376	6.156537	0.089706	3.529246	0.092347	3.821947	0.075538	6.297396	0.076944	6.237976	0.092143	3.824660
0.136728	6.007139	0.122624	6.156537	0.210294	3.529246	0.207653	3.821947	0.124462	6.297396	0.123056	6.237976	0.207857	3.824660
0.151420	0.000000	0.131673	0.000000	0.234412	0.000000	0.230714	0.000000	0.134247	0.000000	0.132279	0.000000	0.231000	0.000000
0.355052	0.000000	0.290354	0.000000	0.550350	0.000000	0.608787	0.000000	0.270355	0.000000	0.232174	0.000000	0.478047	0.000000

Table 2-31 Peak Current (PWL) for SiWare-LT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = FALSE)

tt1p2v25c		ss1p08v125c		ff1p32vn40c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.396466	7.651325	0.307396	17.107188	0.607393	4.877910	0.663419	4.841248	0.293111	15.282300	0.251553	16.909403	0.800000	4.788748
0.603534	7.651325	0.392604	17.107188	0.892607	4.877910	0.936581	4.841248	0.406889	15.282300	0.348447	16.909403	1.121953	0.000000
0.644948	0.000000	0.409646	0.000000	0.949650	0.000000	0.991213	0.000000	0.429645	0.000000	0.367826	0.000000	7.450000	0.000000
7.450000	0.000000	7.450000	0.000000	7.450000	0.000000	7.450000	0.000000	7.450000	0.000000	7.450000	0.000000	7.500000	0.000000
7.500000	0.000000	7.500000	0.000000	7.500000	0.000000	7.500000	0.000000	7.500000	0.000000	7.500000	0.000000	7.550000	0.000000
7.550000	0.000000	7.550000	0.000000	7.550000	0.000000	7.550000	0.000000	7.550000	0.000000	7.550000	0.000000	7.600000	0.000000
7.600000	0.000000	7.600000	0.000000	7.600000	0.000000	7.600000	0.000000	7.600000	0.000000	7.600000	0.000000	7.650000	0.000000
7.650000	0.000000	7.650000	0.000000	7.650000	0.000000	7.650000	0.000000	7.650000	0.000000	7.650000	0.000000	7.700000	0.000000
7.700000	0.000000	7.700000	0.000000	7.700000	0.000000	7.700000	0.000000	7.700000	0.000000	7.700000	0.000000	7.750000	0.000000

Table 2-32 Peak Current (PWL) for SiWare-LT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = TRUE)

tt1p2v25c		ff1p32vn40c		ss1p08v125c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000
0.027924	0.000000	0.066009	0.000000	0.048022	0.000000	0.052958	0.000000	0.098012	0.000000	0.064911	0.000000	0.054300	0.000000
0.048517	5.403307	0.075720	5.001468	0.077159	3.139561	0.080685	3.510976	0.112866	7.319345	0.074936	4.820058	0.081643	3.595901
0.151483	5.403307	0.124280	5.001468	0.222841	3.139561	0.219315	3.510976	0.187134	7.319345	0.125064	4.820058	0.218357	3.595901
0.172076	0.000000	0.133991	0.000000	0.251978	0.000000	0.247042	0.000000	0.200000	0.979737	0.135089	0.000000	0.245700	0.000000

Table 2-32 Peak Current (PWL) for SiWare-LT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = TRUE)

tt1p2v25c		ff1p32vn40c		ss1p08v125c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.411871	0.000000	0.262668	0.000000	0.574803	0.000000	0.440442	0.000000	0.201988	0.000000	0.259334	0.000000	0.564419	0.000000
0.451336	6.939274	0.287620	13.173134	0.624859	5.323050	0.750000	5.047489	0.272182	0.000000	0.285239	13.292462	0.617442	4.758342
0.648664	6.939274	0.412380	13.173134	0.875141	5.323050	1.059558	0.000000	0.294416	12.766946	0.414761	13.292462	0.882558	4.758342
0.688129	0.000000	0.437332	0.000000	0.925197	0.000000	7.450000	0.000000	0.405584	12.766946	0.440666	0.000000	0.935581	0.000000
7.450000	0.000000	7.450000	0.000000	7.450000	0.000000	7.500000	0.000000	0.427818	0.000000	7.450000	0.000000	7.450000	0.000000
7.500000	0.000000	7.500000	0.000000	7.500000	0.000000	7.550000	0.000000	7.450000	0.000000	7.500000	0.000000	7.500000	0.000000
7.550000	0.000000	7.550000	0.000000	7.550000	0.000000	7.600000	0.000000	7.500000	0.000000	7.550000	0.000000	7.550000	0.000000
7.600000	0.000000	7.600000	0.000000	7.600000	0.000000	7.650000	0.000000	7.550000	0.000000	7.600000	0.000000	7.600000	0.000000
7.650000	0.000000	7.650000	0.000000	7.650000	0.000000	7.700000	0.000000	7.600000	0.000000	7.650000	0.000000	7.650000	0.000000
7.700000	0.000000	7.700000	0.000000	7.700000	0.000000	7.750000	0.000000	7.650000	0.000000	7.700000	0.000000	7.700000	0.000000

Table 2-33 Peak Current (PWL) for SiWare-IT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = FALSE)

tt1p2v25c		ff1p32vn40c		ss1p08v125c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000
0.027009	0.000000	0.068256	0.000000	0.041714	0.000000	0.047788	0.000000	0.065753	0.000000	0.067721	0.000000	0.047459	0.000000
0.047863	6.007139	0.077326	6.172919	0.072653	3.529246	0.076991	3.828919	0.075538	6.297396	0.076944	6.237976	0.076757	3.824660
0.152137	6.007139	0.122674	6.172919	0.227347	3.529246	0.223009	3.828919	0.124462	6.297396	0.123056	6.237976	0.223243	3.824660

Table 2-33 Peak Current (PWL) for SiWare-IT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = FALSE)

tt1p2v25c		ff1p32vn40c		ss1p08v125c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.172991	0.000000	0.131744	0.000000	0.258286	0.000000	0.252212	0.000000	0.134247	0.000000	0.132279	0.000000	0.252541	0.000000
0.369911	0.000000	0.274179	0.000000	0.564559	0.000000	0.487429	0.000000	0.270355	0.000000	0.232174	0.000000	0.624481	0.000000
0.407079	7.651325	0.295842	17.123570	0.617542	4.877910	0.800000	4.848220	0.293111	15.282300	0.251553	16.909403	0.674629	4.788748
0.592921	7.651325	0.404158	17.123570	0.882458	4.877910	1.112571	0.000000	0.406889	15.282300	0.348447	16.909403	0.925371	4.788748
0.630089	0.000000	0.425821	0.000000	0.935441	0.000000	7.450000	0.000000	0.429645	0.000000	0.367826	0.000000	0.975519	0.000000
7.450000	0.000000	7.450000	0.000000	7.450000	0.000000	7.500000	0.000000	7.450000	0.000000	7.450000	0.000000	7.450000	0.000000
7.500000	0.000000	7.500000	0.000000	7.500000	0.000000	7.550000	0.000000	7.500000	0.000000	7.500000	0.000000	7.500000	0.000000
7.550000	0.000000	7.550000	0.000000	7.550000	0.000000	7.600000	0.000000	7.550000	0.000000	7.550000	0.000000	7.550000	0.000000
7.600000	0.000000	7.600000	0.000000	7.600000	0.000000	7.650000	0.000000	7.600000	0.000000	7.600000	0.000000	7.600000	0.000000
7.650000	0.000000	7.650000	0.000000	7.650000	0.000000	7.700000	0.000000	7.650000	0.000000	7.650000	0.000000	7.650000	0.000000
7.700000	0.000000	7.700000	0.000000	7.700000	0.000000	7.750000	0.000000	7.700000	0.000000	7.700000	0.000000	7.700000	0.000000

Table 2-34 Peak Current (PWL) for SiWare-IT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = TRUE)

tt1p2v25c		ff1p32vn40c		ss1p08v125c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000
0.027924	0.000000	0.066009	0.000000	0.026931	0.000000	0.052958	0.000000	0.098012	0.000000	0.064911	0.000000	0.054134	0.000000
0.048517	5.403307	0.075720	5.001468	0.062093	3.139561	0.080685	3.510976	0.112866	7.319345	0.074936	4.820058	0.081524	3.603441

Table 2-34 Peak Current (PWL) for SiWare-IT - Standard PVTs - 64x16CM4SW1BK1 (low_leakage = TRUE)

tt1p2v25c		ff1p32vn40c		ss1p08v125c		ss1p08vn40c		ff1p32v125c		ff1p32vn55c		ss1p08vn55c	
ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA	ns	mA
0.151483	5.403307	0.124280	5.001468	0.237907	3.139561	0.219315	3.510976	0.187134	7.319345	0.125064	4.820058	0.218476	3.603441
0.172076	0.000000	0.133991	0.000000	0.273069	0.000000	0.247042	0.000000	0.200000	0.979737	0.135089	0.000000	0.245866	0.000000
0.411871	0.000000	0.262668	0.000000	0.585032	0.000000	0.440442	0.000000	0.201988	0.000000	0.259334	0.000000	0.559066	0.000000
0.451336	6.939274	0.287620	13.173134	0.632166	5.323050	0.750000	5.047489	0.272182	0.000000	0.285239	13.292462	0.613618	4.765882
0.648664	6.939274	0.412380	13.173134	0.867834	5.323050	1.059558	0.000000	0.294416	12.766946	0.414761	13.292462	0.886382	4.765882
0.688129	0.000000	0.437332	0.000000	0.914968	0.000000	7.450000	0.000000	0.405584	12.766946	0.440666	0.000000	0.940934	0.000000
7.450000	0.000000	7.450000	0.000000	7.450000	0.000000	7.500000	0.000000	0.427818	0.000000	7.450000	0.000000	7.450000	0.000000
7.500000	0.000000	7.500000	0.000000	7.500000	0.000000	7.550000	0.000000	7.450000	0.000000	7.500000	0.000000	7.500000	0.000000
7.550000	0.000000	7.550000	0.000000	7.550000	0.000000	7.600000	0.000000	7.500000	0.000000	7.550000	0.000000	7.550000	0.000000
7.600000	0.000000	7.600000	0.000000	7.600000	0.000000	7.650000	0.000000	7.550000	0.000000	7.600000	0.000000	7.600000	0.000000
7.650000	0.000000	7.650000	0.000000	7.650000	0.000000	7.700000	0.000000	7.600000	0.000000	7.650000	0.000000	7.650000	0.000000
7.700000	0.000000	7.700000	0.000000	7.700000	0.000000	7.750000	0.000000	7.650000	0.000000	7.700000	0.000000	7.700000	0.000000

2.3.22 Power Dissipation

> **Note** The data in the tables does not include sub-threshold and junction leakage current.

2.3.22.1 Leakage Current

Table 2-35 shows the Peak Current and Static Idd values for active and inactive ME for the instance configuration specified in Table 2-21 on page 44.

Table 2-35 Power Dissipation for Leakage Current - 64x16CM4SW1BK1

	Static Idd (uA) for active ME				Static Idd (uA) for inactive ME	
bist_enable	**FALSE**	**TRUE**	**FALSE**	**TRUE**	**FALSE**	**TRUE**
low_leakage	**FALSE**	**FALSE**	**TRUE**	**TRUE**	**TRUE**	**TRUE**
tt1p2v25c (Default)	1.067E-01	1.113E-01	5.212E-02	5.390E-02	4.283E-02	4.461E-02
ff1p32vn40c (Default)	5.379E-02	5.626E-02	3.982E-02	4.170E-02	3.903E-02	4.091E-02
ss1p08v125c (Default)	1.000E+00	1.040E+00	5.517E-01	5.619E-01	3.844E-01	3.946E-01
ss1p08vn40c (Default)	1.105E-02	1.148E-02	1.020E-02	1.055E-02	1.017E-02	1.052E-02
ff1p32v125c (Worst Case Leakage)	2.629E+01	2.764E+01	1.521E+01	1.581E+01	1.248E+01	1.308E+01
ff1p32vn55c (Foundry Preferred Corner)	3.960E-02	4.140E-02	3.594E-02	3.756E-02	3.586E-02	3.748E-02
ss1p08vn55c (Foundry Preferred Corner)	1.078E-02	1.119E-02	1.009E-02	1.044E-02	1.008E-02	1.043E-02

2.3.22.2 Power Dissipation for Typical Cycle

In a typical power cycle:

- Alternate cycles are active
- 1/2 address bits are switching
- 1/2 data bits are switching
- Average of read 1/read 0
- Average of address high/low

Table 2-36 shows the typical cycle power dissipation for the instance configuration specified in Table 2-21 on page 44.

Table 2-36 Power Dissipation for Typical Cycle - 64x16CM4SW1BK1

		Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable		FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage		FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
tt1p2v25c (Default)	RD	1.913E+00	1.913E+00	1.834E+00	1.834E+00	1.594E+00	1.594E+00	1.528E+00	1.528E+00
	WR	1.903E+00	1.903E+00	1.800E+00	1.800E+00	1.586E+00	1.586E+00	1.500E+00	1.500E+00
ss1p08v125c (Default)	RD	2.326E+00	2.326E+00	2.237E+00	2.237E+00	1.762E+00	1.762E+00	1.695E+00	1.695E+00
	WR	2.300E+00	2.300E+00	2.174E+00	2.174E+00	1.742E+00	1.742E+00	1.647E+00	1.647E+00
ff1p32vn40c (Default)	RD	1.505E+00	1.505E+00	1.445E+00	1.445E+00	1.394E+00	1.394E+00	1.338E+00	1.338E+00
	WR	1.515E+00	1.515E+00	1.432E+00	1.432E+00	1.403E+00	1.403E+00	1.326E+00	1.326E+00
ss1p08vn40c (Default)	RD	1.452E+00	1.452E+00	1.394E+00	1.394E+00	1.344E+00	1.344E+00	1.290E+00	1.290E+00
	WR	1.469E+00	1.469E+00	1.389E+00	1.389E+00	1.360E+00	1.360E+00	1.287E+00	1.287E+00
ff1p32v125c (Worst Case Leakage)	RD	2.452E+00	2.452E+00	2.353E+00	2.353E+00	1.858E+00	1.858E+00	1.782E+00	1.782E+00
	WR	2.426E+00	2.426E+00	2.283E+00	2.283E+00	1.838E+00	1.838E+00	1.730E+00	1.730E+00
ff1p32vn55c (Foundry Preferred Corner)	RD	2.322E+00	2.322E+00	2.231E+00	2.231E+00	1.759E+00	1.759E+00	1.690E+00	1.690E+00
	WR	2.293E+00	2.293E+00	2.172E+00	2.172E+00	1.737E+00	1.737E+00	1.645E+00	1.645E+00
ss1p08vn55c (Foundry Preferred Corner)	RD	1.445E+00	1.445E+00	1.389E+00	1.389E+00	1.338E+00	1.338E+00	1.286E+00	1.286E+00
	WR	1.464E+00	1.464E+00	1.384E+00	1.384E+00	1.355E+00	1.355E+00	1.282E+00	1.282E+00

2.3.22.3 Power Dissipation for Worst Cycle

In a worst power cycle:

- Back to back cycles
- All address bits are switching
- All data bits are switching
- Worst of read 1/read 0
- Worst of address high/low

Table 2-37 shows the worst cycle power dissipation for the instance configuration specified in Table 2-21 on page 44.

Table 2-37 Power Dissipation for Worst Cycle - 64x16CM4SW1BK1

		Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable		FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage		FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
tt1p2v25c (Default)	RD	3.989E+00	3.989E+00	3.830E+00	3.830E+00	3.324E+00	3.324E+00	3.192E+00	3.192E+00
	WR	4.230E+00	4.230E+00	4.024E+00	4.024E+00	3.525E+00	3.525E+00	3.354E+00	3.354E+00
ss1p08v125c (Default)	RD	4.850E+00	4.850E+00	4.672E+00	4.672E+00	3.674E+00	3.674E+00	3.539E+00	3.539E+00
	WR	5.112E+00	5.112E+00	4.856E+00	4.856E+00	3.873E+00	3.873E+00	3.679E+00	3.679E+00
ff1p32vn40c (Default)	RD	3.143E+00	3.143E+00	3.024E+00	3.024E+00	2.910E+00	2.910E+00	2.800E+00	2.800E+00
	WR	3.377E+00	3.377E+00	3.215E+00	3.215E+00	3.127E+00	3.127E+00	2.977E+00	2.977E+00
ss1p08vn40c (Default)	RD	3.033E+00	3.033E+00	2.917E+00	2.917E+00	2.808E+00	2.808E+00	2.700E+00	2.700E+00
	WR	3.276E+00	3.276E+00	3.119E+00	3.119E+00	3.033E+00	3.033E+00	2.888E+00	2.888E+00
ff1p32v125c (Worst Case Leakage)	RD	5.143E+00	5.143E+00	4.938E+00	4.938E+00	3.897E+00	3.897E+00	3.741E+00	3.741E+00
	WR	5.456E+00	5.456E+00	5.143E+00	5.143E+00	4.133E+00	4.133E+00	3.896E+00	3.896E+00
ff1p32vn55c (Foundry Preferred Corner)	RD	4.842E+00	4.842E+00	4.660E+00	4.660E+00	3.668E+00	3.668E+00	3.530E+00	3.530E+00
	WR	5.098E+00	5.098E+00	4.851E+00	4.851E+00	3.862E+00	3.862E+00	3.675E+00	3.675E+00
ss1p08vn55c (Foundry Preferred Corner)	RD	3.018E+00	3.018E+00	2.907E+00	2.907E+00	2.794E+00	2.794E+00	2.692E+00	2.692E+00
	WR	3.264E+00	3.264E+00	3.107E+00	3.107E+00	3.022E+00	3.022E+00	2.877E+00	2.877E+00

2.3.22.4 Power Dissipation for Data Pin

Table 2-38 shows the power consumed due to the toggle of all bits of the data bus for the instance configuration defined in Table 2-21 on page 44.

Table 2-38 Power Dissipation for Data Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage	FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
tt1p2v25c (Default)	5.478E-01	5.478E-01	5.505E-01	5.505E-01	4.565E-01	4.565E-01	4.588E-01	4.588E-01
ss1p08v125c (Default)	6.611E-01	6.611E-01	6.540E-01	6.540E-01	5.008E-01	5.008E-01	4.955E-01	4.955E-01
ff1p32vn40c (Default)	4.497E-01	4.497E-01	4.545E-01	4.545E-01	4.164E-01	4.164E-01	4.209E-01	4.209E-01
ss1p08vn40c (Default)	4.382E-01	4.382E-01	4.419E-01	4.419E-01	4.058E-01	4.058E-01	4.091E-01	4.091E-01
ff1p32v125c (Worst Case Leakage)	7.666E-01	7.666E-01	7.207E-01	7.207E-01	5.808E-01	5.808E-01	5.460E-01	5.460E-01
ff1p32vn55c (Foundry Preferred Corner)	6.583E-01	6.583E-01	6.517E-01	6.517E-01	4.987E-01	4.987E-01	4.937E-01	4.937E-01
ss1p08vn55c (Foundry Preferred Corner)	4.372E-01	4.372E-01	4.402E-01	4.402E-01	4.048E-01	4.048E-01	4.076E-01	4.076E-01

2.3.22.5 Power Dissipation for Address Pin

Table 2-39 shows the power consumed due to the toggle of all bits of the address bus for the instance configuration specified in Table 2-21 on page 44.

Table 2-39 Power Dissipation for Address Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage	FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
tt1p2v25c (Default)	2.983E-01	2.983E-01	2.995E-01	2.995E-01	2.486E-01	2.486E-01	2.496E-01	2.496E-01
ss1p08v125c (Default)	3.645E-01	3.645E-01	3.621E-01	3.621E-01	2.762E-01	2.762E-01	2.744E-01	2.744E-01
ff1p32vn40c (Default)	2.433E-01	2.433E-01	2.463E-01	2.463E-01	2.253E-01	2.253E-01	2.280E-01	2.280E-01
ss1p08vn40c (Default)	2.368E-01	2.368E-01	2.373E-01	2.373E-01	2.193E-01	2.193E-01	2.197E-01	2.197E-01

Table 2-39 Power Dissipation for Address Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage	FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
ff1p32v125c (Worst Case Leakage)	4.408E-01	4.408E-01	4.313E-01	4.313E-01	3.340E-01	3.340E-01	3.268E-01	3.268E-01
ff1p32vn55c (Foundry Preferred Corner)	3.644E-01	3.644E-01	3.631E-01	3.631E-01	2.761E-01	2.761E-01	2.750E-01	2.750E-01
ss1p08vn55c (Foundry Preferred Corner)	2.359E-01	2.359E-01	2.375E-01	2.375E-01	2.184E-01	2.184E-01	2.199E-01	2.199E-01

2.3.22.6 Power Dissipation for WRITE_ENABLE Pin

Table 2-40 shows the power consumed due to the toggle of the WE pin for the instance configuration specified in Table 2-21 on page 44.

Table 2-40 Power Dissipation for WRITE_ENABLE Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage	FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
tt1p2v25c (Default)	4.397E-01	4.397E-01	4.460E-01	4.460E-01	3.664E-01	3.664E-01	3.717E-01	3.717E-01
ss1p08v125c (Default)	5.319E-01	5.319E-01	5.320E-01	5.320E-01	4.030E-01	4.030E-01	4.030E-01	4.030E-01
ff1p32vn40c (Default)	3.620E-01	3.620E-01	3.676E-01	3.676E-01	3.352E-01	3.352E-01	3.404E-01	3.404E-01
ss1p08vn40c (Default)	3.533E-01	3.533E-01	3.565E-01	3.565E-01	3.271E-01	3.271E-01	3.301E-01	3.301E-01
ff1p32v125c (Worst Case Leakage)	5.606E-01	5.606E-01	5.403E-01	5.403E-01	4.247E-01	4.247E-01	4.093E-01	4.093E-01
ff1p32vn55c (Foundry Preferred Corner)	5.297E-01	5.297E-01	5.298E-01	5.298E-01	4.013E-01	4.013E-01	4.013E-01	4.013E-01
ss1p08vn55c (Foundry Preferred Corner)	3.513E-01	3.513E-01	3.574E-01	3.574E-01	3.253E-01	3.253E-01	3.310E-01	3.310E-01

2.3.22.7 Power Dissipation for MEMORY_ENABLE Pin

Table 2-41 shows the power consumed due to the toggle of ME pin for the instance configuration specified in Table 2-21 on page 44.

Table 2-41 Power Dissipation for MEMORY_ENABLE Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	**FALSE**	**TRUE**	**FALSE**	**TRUE**	**FALSE**	**TRUE**	**FALSE**	**TRUE**
low_leakage	**FALSE**	**FALSE**	**TRUE**	**TRUE**	**FALSE**	**FALSE**	**TRUE**	**TRUE**
tt1p2v25c (Default)	4.838E-01	4.838E-01	5.726E-01	5.726E-01	4.032E-01	4.032E-01	4.772E-01	4.772E-01
ss1p08v125c (Default)	5.862E-01	5.862E-01	6.856E-01	6.856E-01	4.441E-01	4.441E-01	5.194E-01	5.194E-01
ff1p32vn40c (Default)	3.964E-01	3.964E-01	4.730E-01	4.730E-01	3.670E-01	3.670E-01	4.380E-01	4.380E-01
ss1p08vn40c (Default)	3.861E-01	3.861E-01	4.551E-01	4.551E-01	3.575E-01	3.575E-01	4.214E-01	4.214E-01
ff1p32v125c (Worst Case Leakage)	6.470E-01	6.470E-01	7.504E-01	7.504E-01	4.902E-01	4.902E-01	5.685E-01	5.685E-01
ff1p32vn55c (Foundry Preferred Corner)	5.832E-01	5.832E-01	6.854E-01	6.854E-01	4.419E-01	4.419E-01	5.192E-01	5.192E-01
ss1p08vn55c (Foundry Preferred Corner)	3.845E-01	3.845E-01	4.539E-01	4.539E-01	3.560E-01	3.560E-01	4.203E-01	4.203E-01

2.3.22.8 Power Dissipation for Dataout Pin

Table 2-42 shows the power consumed due to the toggle of all bits of output bus for the instance configuration specified in Table 2-21 on page 44.

Table 2-42 Power Dissipation for Dataout Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	**FALSE**	**TRUE**	**FALSE**	**TRUE**	**FALSE**	**TRUE**	**FALSE**	**TRUE**
low_leakage	**FALSE**	**FALSE**	**TRUE**	**TRUE**	**FALSE**	**FALSE**	**TRUE**	**TRUE**
tt1p2v25c (Default)	2.999E-02	2.999E-02	3.048E-02	3.048E-02	2.500E-02	2.500E-02	2.540E-02	2.540E-02
ss1p08v125c (Default)	3.621E-02	3.621E-02	3.638E-02	3.638E-02	2.743E-02	2.743E-02	2.756E-02	2.756E-02
ff1p32vn40c (Default)	2.454E-02	2.454E-02	2.504E-02	2.504E-02	2.272E-02	2.272E-02	2.319E-02	2.319E-02

Table 2-42 Power Dissipation for Dataout Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage	FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
ss1p08vn40c (Default)	2.392E-02	2.392E-02	2.449E-02	2.449E-02	2.215E-02	2.215E-02	2.268E-02	2.268E-02
ff1p32v125c (Worst Case Leakage)	4.133E-02	4.133E-02	3.819E-02	3.819E-02	3.131E-02	3.131E-02	2.893E-02	2.893E-02
ff1p32vn55c (Foundry Preferred Corner)	3.603E-02	3.603E-02	3.630E-02	3.630E-02	2.730E-02	2.730E-02	2.750E-02	2.750E-02
ss1p08vn55c (Foundry Preferred Corner)	2.389E-02	2.389E-02	2.444E-02	2.444E-02	2.212E-02	2.212E-02	2.263E-02	2.263E-02

2.3.22.9 Power Dissipation for MASK Pin

Table 2-43 shows the power consumed due to the toggle of all bits of the WEM bus for the instance configuration specified in Table 2-21 on page 44.

Table 2-43 Power Dissipation for MASK Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage	FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
tt1p2v25c (Default)	5.478E-01	5.478E-01	5.505E-01	5.505E-01	4.565E-01	4.565E-01	4.588E-01	4.588E-01
ss1p08v125c (Default)	6.611E-01	6.611E-01	6.540E-01	6.540E-01	5.008E-01	5.008E-01	4.955E-01	4.955E-01
ff1p32vn40c (Default)	4.497E-01	4.497E-01	4.545E-01	4.545E-01	4.164E-01	4.164E-01	4.209E-01	4.209E-01
ss1p08vn40c (Default)	4.382E-01	4.382E-01	4.419E-01	4.419E-01	4.058E-01	4.058E-01	4.091E-01	4.091E-01
ff1p32v125c (Worst Case Leakage)	7.666E-01	7.666E-01	7.207E-01	7.207E-01	5.808E-01	5.808E-01	5.460E-01	5.460E-01
ff1p32vn55c (Foundry Preferred Corner)	6.583E-01	6.583E-01	6.517E-01	6.517E-01	4.987E-01	4.987E-01	4.937E-01	4.937E-01

Table 2-43 Power Dissipation for MASK Pin Toggling - 64x16CM4SW1BK1

	Power Dissipation (uW/MHz)				Current (uA/MHz)			
bist_enable	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
low_leakage	FALSE	FALSE	TRUE	TRUE	FALSE	FALSE	TRUE	TRUE
ss1p08vn55c (Foundry Preferred Corner)	4.372E-01	4.372E-01	4.402E-01	4.402E-01	4.048E-01	4.048E-01	4.076E-01	4.076E-01

2.3.22.10 Power Dissipation for Clock Read, Write, and Disable Cycle

The tables in this section show clock Read, Write, and Disable cycle data for the instance configuration specified in Table 2-21 on page 44. The values are given when no other signal except clock is switching. They assume full data and address switching.

- **Clock read power dissipation** - Pure read power. Current consumed in a cycle in which read operation is performed. No input other than CLK toggles, all outputs toggle.
- **Clock write power dissipation** - Pure write power. Current consumed in a cycle in which write operation is performed. No input other than CLK toggles, all data inputs are changed with respect to the previous Write cycle.
- **Clock disabled power dissipation** (**`ME=0`**) - Current consumed in the cycle with memory disabled, only CLK toggles.

Table 2-44 Power Dissipation for Clock Read, Write and Disable Cycle SiWare-LT - 64x16CM4SW1BK1

	low_leakage=FALSE						low_leakage=TRUE					
	READ		WRITE		DISABLED		READ		WRITE		DISABLED	
	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)
tt1p2v25c (Default)	3.56E+00	2.97E+00	3.28E+00	2.73E+00	1.05E-01	8.71E-02	3.40E+00	2.83E+00	3.07E+00	2.56E+00	1.04E-01	8.65E-02
ss1p08v125c (Default)	4.33E+00	3.28E+00	3.96E+00	3.00E+00	1.23E-01	9.33E-02	4.16E+00	3.15E+00	3.72E+00	2.82E+00	1.23E-01	9.31E-02
ff1p32vn40c (Default)	2.79E+00	2.58E+00	2.60E+00	2.40E+00	8.72E-02	8.08E-02	2.67E+00	2.47E+00	2.43E+00	2.25E+00	8.71E-02	8.07E-02
ss1p08vn40c (Default)	2.69E+00	2.49E+00	2.52E+00	2.33E+00	8.23E-02	7.62E-02	2.57E+00	2.38E+00	2.36E+00	2.18E+00	8.34E-02	7.72E-02

Table 2-44 Power Dissipation for Clock Read, Write and Disable Cycle SiWare-LT - 64x16CM4SW1BK1

	low_leakage=FALSE						low_leakage=TRUE					
	READ		WRITE		DISABLED		READ		WRITE		DISABLED	
	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)
ff1p32v125c (Worst Case Leakage)	4.53E+00	3.44E+00	4.12E+00	3.12E+00	1.31E-01	9.89E-02	4.33E+00	3.28E+00	3.84E+00	2.91E+00	1.47E-01	1.12E-01
ff1p32vn55c (Foundry Preferred Corner)	4.32E+00	3.28E+00	3.95E+00	2.99E+00	1.23E-01	9.30E-02	4.14E+00	3.14E+00	3.71E+00	2.81E+00	1.23E-01	9.35E-02
ss1p08vn55c (Foundry Preferred Corner)	2.68E+00	2.48E+00	2.51E+00	2.32E+00	8.28E-02	7.67E-02	2.57E+00	2.38E+00	2.35E+00	2.17E+00	8.25E-02	7.64E-02

Table 2-45 Power Dissipation for Clock Read, Write and Disable Cycle SiWare-IT - 64x16CM4SW1BK1

	low_leakage=FALSE						low_leakage=TRUE					
	READ		WRITE		DISABLED		READ		WRITE		DISABLED	
	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)
tt1p2v25c (Default)	3.56E+00	2.97E+00	3.28E+00	2.73E+00	1.05E-01	8.71E-02	3.40E+00	2.83E+00	3.07E+00	2.56E+00	1.04E-01	8.65E-02
ss1p08v125c (Default)	4.33E+00	3.28E+00	3.96E+00	3.00E+00	1.23E-01	9.33E-02	4.16E+00	3.15E+00	3.72E+00	2.82E+00	1.23E-01	9.31E-02
ff1p32vn40c (Default)	2.79E+00	2.58E+00	2.60E+00	2.40E+00	8.72E-02	8.08E-02	2.67E+00	2.47E+00	2.43E+00	2.25E+00	8.71E-02	8.07E-02
ss1p08vn40c (Default)	2.69E+00	2.49E+00	2.52E+00	2.33E+00	8.23E-02	7.62E-02	2.57E+00	2.38E+00	2.36E+00	2.18E+00	8.34E-02	7.72E-02

Table 2-45 Power Dissipation for Clock Read, Write and Disable Cycle SiWare-IT - 64x16CM4SW1BK1

	low_leakage=FALSE						low_leakage=TRUE					
	READ		WRITE		DISABLED		READ		WRITE		DISABLED	
	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)	Power Dissipation (uW/MHz)	Current (uA/MHz)
ff1p32v125c (Worst Case Leakage)	4.53E+00	3.44E+00	4.12E+00	3.12E+00	1.31E-01	9.89E-02	4.33E+00	3.28E+00	3.84E+00	2.91E+00	1.47E-01	1.12E-01
ff1p32vn55c (Foundry Preferred Corner)	4.32E+00	3.28E+00	3.95E+00	2.99E+00	1.23E-01	9.30E-02	4.14E+00	3.14E+00	3.71E+00	2.81E+00	1.23E-01	9.35E-02
ss1p08vn55c (Foundry Preferred Corner)	2.68E+00	2.48E+00	2.51E+00	2.32E+00	8.28E-02	7.67E-02	2.57E+00	2.38E+00	2.35E+00	2.17E+00	8.25E-02	7.64E-02

3 Compiler Source and Output Files

This chapter describes the directory structure of the compiler database, files, and templates.

3.1 Using Compiler Library Files

The files that make up the compiler are located in the **<compiler>** directory. Each compiler directory is located in a compiler library. See the Embed-It! Integrator User Guide for details on specifying the compiler library path information. Table 3-1 provides a description of these files.

The files described in the figures and tables in this chapter represent a complete list of the files that may be included in a Synopsys compiler. However, these files are independent of the technology/process and some of them may not be included and/or supported by the current compiler. Contact Synopsys support for additional assistance.

Table 3-1 Files in the <compiler> Library

Filename	Contains
User-editable files	
<Compiler_name>_custom.glb	Customer-specific overrides to flags in the compiler global parameters (glb) file.
design2<foundry>.ltt	GDSII layer mapping details-the design layer numbers are mapped to foundry layers.
Read-only files	
release.txt	Information about the changes made to the compiler in each patch release of the compiler such as patch notes and release notes.
release_templates.txt	Template updates and release notes.
Information files	
check.tcl	Tcl file to check range of the values for NW, NB, CM and SW for the compiler.
gdsview.cfg	Layer display and window position options for the gdsview tool.
<Compiler_name>.cir	Netlist file that represents the circuit design. It is used for LVS.

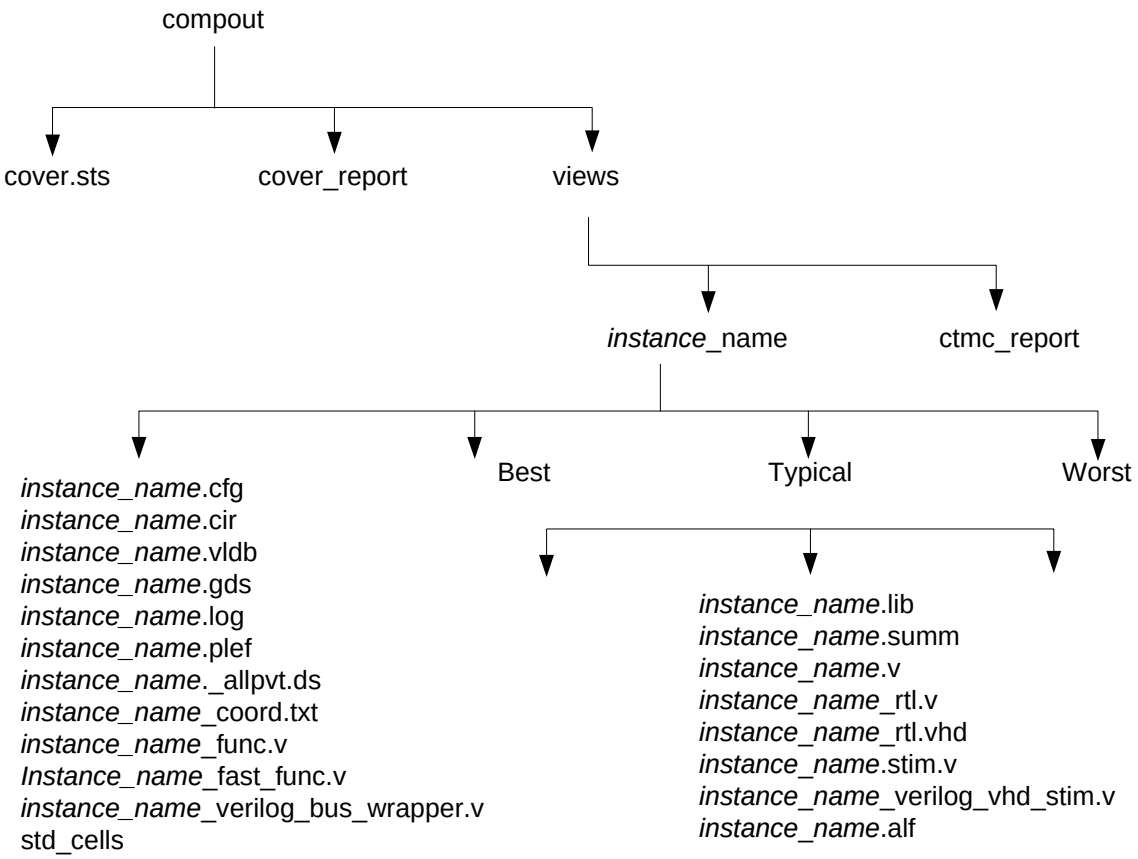
Table 3-1 Files in the <compiler> Library

Filename	Contains
<Compiler_name>.del	Delay equation file with commands to process data from the raw file (<Compiler_name>.raw) and send the result to the relevant templates.
<Compiler_name>.gds	Graphical information for the leaf cells used in building a memory instance.
<Compiler_name>.pf	Memory instance structure information placement file. It contains the layout tiling and netlist generation instructions to build an instance in the compiler range.
<Compiler_name>.raw	Characterization measurement data such as timing and power data for all configurations across the compiler range.
<Compiler_name>.v	Switch-level representation of all cells used to build instances. The macros defined in this library are called by the switch-level netlist generated by the placement file <Compiler_name>.pf.
<Compiler_name>.glb	Global parameters file to set up compiler specific instance generation options. The other compiler-specific files (with the extensions .del, .gds, .pf, .raw, .cir, and .ppr) are referenced in this file.
<Compiler_name>.prm	Parameter definitions file for the compiler.
<Compiler_name>.cpj	This is a database file for autochar enabled compilers. It contains all the information that is required for characterization of the compiler.
<Compiler_name>.ppr	Pin and power ring configuration file.
*.tpl	Front-End Template files (encrypted).

3.2 Accessing Output Files

The compiler generates output files and directories and stores them in the compout directory, which is the root output directory. Figure 3-1 shows an example of a compout directory structure.

Figure 3-1 compout Directory Structure Example



3.2.1 compout Directory

Table 3-2 lists and describes the contents of the compout directory.

Table 3-2 compout Directory

Filename	Description
cover.sts	Shows the error and warning statistics during instance generation.
cover_report	Reports the number of errors and warnings after the COVER file completes execution.
views/	Directory that contains the ctmc_report and the instance directory. See *compout/views Subdirectory*.

3.2.1.1 compout/views Subdirectory

Table 3-3 lists and describes the compout/views directory files, ctmc_report and *instance_name*. The *instance_name* is substituted with the name of the memory instance generated.

Table 3-3 compout/views Subdirectory

Filename	Description
ctmc_report	Reports the number of errors and warnings after the instance is generated.
instance_name/	Instance directory. See compout/views/instance_name Subdirectory.

compout/views/instance_name Subdirectory

Table 3-4 lists and describes the compout/views/instance_name subdirectory.

Table 3-4 compout/views/instance_name Subdirectory

Filename	Description
Best/	Subdirectory containing front-end views for the best operating point.
Typical/	Subdirectory containing front-end views for the typical operating point.
Worst/	Subdirectory containing front-end views for the worst operating point.
instance_name.cfg	Instance configuration file.
instance_name.cir	Instance SPICE netlist for LVS.
instance_name.db	Synopsys' internal database that records all options set for this instance.
instance_name.gds	Instance GDSII view.
instance_name.log	Instance log file.
instance_name.plef	Physical LEF view of the ring structure. Includes instance blockages.
*instance_name*_allpvt.ds	All PVT datasheet that provides pin descriptions, logic truth table, timing characterization, Read and Write cycle timing, and power dissipation.
*instance_name*_coord.txt	File that contains the x and y coordinates of the power ring edges and memory core in the instance.
*instance_name*_func.v	A switch-level Verilog netlist file. The same switch-level or transistor-level netlist that the compiler generates in SPICE format can also be generated in Verilog. The difference is that the Verilog netlist can be used for logic simulation and not for LVS.
*instance_name*_fast_func.v	Verilog model with limited functionality to speed up the simulation time. It is useful during initial phase of implementation and should not be mistaken for a signed-off quality Verilog model. This model supports only basic read/write operations (without bist muxes), LS, DS, SD and PIPEME functionality. It supports X-handling and "virage_ignore_read_addx" option. The **$readmemh** task can be used to load the memory.

Table 3-4 compout/views/instance_name Subdirectory

Filename	Description
*instance_name*_verilog_bus_wrapper.v	Verilog file used to test the basic functionality of the memory without consideration for BIST or ATPG.
std_cells.v	Verilog model for the dummy standard cells used in Verilog netlist for ATPG.
*instance_name*_hcell.txt	Hcell equivalence file for hierarchical LVS matching with Calibre.

3.2.2 compout/views/instance_name/Best, Typical, and Worst Subdirectory Files

Table 3-5 shows the files in the compout/views/instance_name/Best, Typical, and Worst Subdirectory. The directory representing each process condition (best, typical, and worst) contains a list of these files.

Table 3-5 compout/views/instance_name/Best, Typical, and Worst Subdirectory Files

Filename	Description
instance_name.lib	Synopsys timing model.
instance_name.summ	Summary (generated from mc_dssum.tpl) of values such as configuration, CM, Address Setup, Cycle time, Area, Power, PVT value, Width and Height. The *instance_name*.summ template provides a quick reference to all of these features.
instance_name.v	Instance Verilog model.
*instance_name*_rtl.vhd	VHDL RTL core model.
*instance_name*_stim.v	Verilog behavioral model testbench.
*instance_name*_verilog_vhd_stim.v	Verilog behavioral model and VHDL behavioral model testbench.

4 Using Front-End Files

This chapter describes the front-end files, which support documentation, simulation and testing of memory instances. The front-end files are the raw data file, the delay equation file, and the template files. They provide the front-end views of the memory instance. The following sections describe these files:

- "Using Template Files" on page 79
- "Setting Front-End Flags" on page 84

Note For detailed description of all output views, please refer to Chapter 13 of the Embed-It!® Integrator Manual.

4.1 Using Template Files

The compiler library contains a template for each front-end view. The compiler software uses these templates to generate the corresponding front-end files.

The following sections describe the front-end views that Synopsys, Inc. supports.

- "Using ATPG Tools" on page 80
- "Using MemoryBIST Tools" on page 80
- "Performing Power Analysis" on page 81
- "Performing Simulations" on page 81
- "Performing Static Timing Analysis" on page 82
- "Using Switch-Level Verilog Models" on page 83
- "Power Verilog Models" on page 83
- "RTL Power Optimization" on page 84

4.1.1 Using ATPG Tools

Synopsys, Inc. supports the ATPG tools TetraMAX and FastScan.

The Synopsys compilers use the **mc_spf.tpl** template file as the initialization file for Tetramax. The **mc_fastscan.tpl** template file generates the FastScan (**.fs_lib**) model and the **mc_atpg_netlist.tpl** generates a Verilog Netlist for ATPG (**_atpg_netlist.v**). The template provides both FastScan and mBIST solutions based on how you set the front-end flag **mbist_on**.

- If **mbist_on=0**, the .fs_lib model provides only FastScan solution.
- If **mbist_on=1**, the .fs_lib model provides both FastScan and mBIST solutions.
- Use the **mc_tpf.tpl** template file to obtain test procedures for FastScan.

4.1.2 Using MemoryBIST Tools

This section is not applicable for **bist_enable=TRUE** or **redundancy_enable=TRUE**. When the **bist_enable** option is enabled, the generated memory instance includes multiplexers (muxes) for all address, control and data signals as well as comparators and capture logic. Third party memory BIST will not yet support this additional logic.

Synopsys, Inc. provides both BIST and scan solutions to verify memory. The time taken to scan in inputs and scan out results increases the total test time. The BIST models generate synthesis scripts for the BIST controller and test cases based on standard algorithms.

Synopsys, Inc. supports the STAR Memory System and third party MemoryBIST tools. The STAR Memory System is more advantageous when integrated test logic is included when compiling the memory instances. The integrated test logic enables high speed test and reduces the routing congestion between the memory instance and the wrapper.

Synopsys' memory compilers support third party Tessent MemoryBIST and BoundaryScan solutions with views generated by the **mc_fastscan.tpl** template file.

- If **mbist_on=0**, the .fs_lib model provides only BoundaryScan solution.
- If **mbist_on=1**, the .fs_lib model provides both BoundaryScan and MemoryBIST solutions.

The **MemoryBIST** view is generated using the **mc_membist.tpl** template file. The **.membist** file is the memBISTGenerate configuration file. It contains the:

- MemoryController wrapper file—Describes each memory instance
- MemoryCollar template wrapper file—Describes the sequence of memory tests. This file references a MemoryTemplate in the memory library file **.lvlib**.

The **.lvlib** library file contains the MemoryTemplate wrapper, which describes the ports and behavior of the memory.

4.1.3 Performing Power Analysis

Synopsys, Inc. supports the power analysis model Advanced Library Format (ALF).

4.1.3.1 Using ALF

Use the **mc_alf.tpl** template file to generate the ALF view. The view consists of library and cell sections. The cell section contains the pin descriptions and input pin constraints. It also contains the power information for the memory similar to the Synopsys model. Use the ALF format to perform power analysis with the help of Powertheatre from Sequence Design.

The Synopsys ALF format denotes the Advanced Library Format. There are other products such as the Cadence Ambit tool format Ambit Library Format, which are different from the Synopsys ALF.

4.1.4 Performing Simulations

The following sections describe the simulation models that Synopsys, Inc. supports:

- "Using Verilog Behavioral Model" on page 81
- "Using Verilog RTL Model" on page 82
- "Using VHDL RTL Model" on page 82

4.1.4.1 Using Verilog Behavioral Model

The simulation model that Synopsys, Inc. supports is Verilog Behavioral Model.

Use the **mc_verilog.tpl** template file to generate the .v Verilog behavioral model. This model describes the logic in different modes with every possible transition of every pin along with X handling and timing violations. The timing values include all path delays, input pins, constraint timing, and recovery.

To help perform simulations with parallel testbench from ATPG tools like Mentor fastscan & Synopsys tetramax, the Verilog behavioral model contains dummy standard cells with exactly same hierarchy as ATPG netlist.

The Compiler contains the **std_cells.v** file. This file is a Verilog model for the dummy standard cells used in Verilog netlist for ATPG.

To perform verilog simulations, use verilog **<mem>.v -v std_cells.v**.

When Verilog Behavioral model is used with command line arguments **+define+VIRAGE_FAST_VERILOG**, the model will act as the RTL model describing only memory functions in all modes. It does not contain timing information.

Verilog Compiler Directives

The verilog behavioral model supports following compiler directives to provide flexibility and extra features to the customers.

- VIRAGE_FAST_VERILOG: When this flag is used, the model will act as the RTL model describing only memory functions in all modes. It does not contain timing information. However, verilog modeling this mode is faster during simulations by 20 - 40% (the range depends on the Simulator and the instance size), when compared to regular behavioral mode with full timing.
- MEM_CHECK_OFF: This flag turns off most display messages from verilog model. These display messages are mostly warnings about hazardous conditions.
- virage_ignore_read_addx: By default, memory is corrupted when address is unknown during read or write cycle. However, if you think it is extra conservative to corrupt memory during read, you can use this switch to make sure memory is not corrupted during unknown address in a read cycle.
- VIRAGE_IGNORE_RESET: This flag ignores the initialization required by the memory verilog model.

An application note is available for a detailed description of Verilog simulation. Contact the Synopsys Support Team at http://solvnet.synopsys.com.

4.1.4.2 Using Verilog RTL Model

Use the **mc_verilog_rtl.tpl** template file to generate the **.v** model and use the "VIRAGE_FAST_VERILOG" define option to simulate this model in Verilog RTL. The Verilog RTL model is the main RTL functional model that describes all functions in different modes. It does not contain timing information.

4.1.4.3 Using VHDL RTL Model

Use the **mc_vhd_rtl.tpl** template file to generate the VHDL RTL **model_rtl.vhd**. The VHDL RTL model is the core RTL model that describes the memory functions in all modes. It does not contain timing information.

4.1.5 Performing Static Timing Analysis

The timing library models contain:

- Memory characterization data in a specific format
- Path delays with transition values for corresponding to slew rates and output loads
- Timing values for input pin constraints such as setup/hold, period, width, and recovery

Use the timing model files to generate SDF data and back-annotate the SDF data into the Verilog/Vital models and verify functionality and timing.

The following section describes the timing analysis tools that Synopsys, Inc. supports:

- Using Synopsys .lib Models

4.1.5.1 Using Synopsys .lib Models

Use the **mc_syn.tpl** template file to generate the Synopsys .lib model.

The Synopsys .lib model contains:

- Delay model—Provides table lookup information for delay calculations

- Environment conditions - Provides various operating conditions and k-factors for circuit timing evaluation.
- Lookup table—Describes timing information for:
  - Describing delays
  - Specifying constraints

The Synopsys .lib model:

- Enables Synopsys tools with library information including cell timing function, physical, power, test data for optimized tools performance while meeting the technology requirements
- Makes the library development process faster through simplified data entry
- Provides low cost library maintenance by using a single library source while minimizing library generation and verification costs
- Offers comprehensive modeling capabilities for design flows
- Develops high quality library that produces better designs
- Generates VHDL test-benches, and eases transition to the VITAL ' 95 standard by leveraging existing synthesis source library
- Offers a reliable, and low-cost, library development solution that is available and ready to use today
- Produces protected platform independent binary library file for delivery to customers

4.1.6 Using Switch-Level Verilog Models

The same switch-level or transistor-level netlist that the compiler generates in SPICE format can also be generated in Verilog. The changes in the Verilog format include replacing the bit cell with a behavioral model, adding delays for simulation, and changing gates to Verilog primitives. The Verilog netlist is generated from the same source that generates the SPICE netlist both for the compiler libraries and instance-specific modules. The output filename is **`<instance>_func.v`**. The difference is that you can use the Verilog netlist for logic simulation and not for LVS.

4.1.7 Power Verilog Models

The Power Verilog Model, ***.mv**, is similar to existing Verilog Behavioral Model. It contains power pins in the port list of memory as well as includes their functionality in the model. There is no role of power pins in the timing checks. The power pins are only included in the functional part of the view.

The following items are modelled with respect to the power pins:

If the power pins are not valid **(VDD /= 1 or VSS /= 0)** then the memory is corrupt (not in case of ROM) and outputs, and no memory operation is allowed.

If the power pins are valid **(VDD = 1 & VSS = 0)** then the power model will behave similar to Verilog Behavioral Model, that is, the memory will operate normally.

4.1.8 RTL Power Optimization

The SiWare compilers generate views to run RTL power optimization tools. These tools reduce both dynamic and leakage power in memories by automatically performing sequential analysis on a design to generate conditions to remove redundant reads/writes to embedded memories and may add controls to enable the use of the light sleep mode.

The power optimization view **<instance_name>_power_opt.v,** if enabled, will be generated and will be located in the compout/views directory.

This view is not yet available for the 2-Port Register File, STAR 8M, and 2-Port Asynchronous Register File compilers. These views will be ready in the next release of these compilers. Contact Customer Support for further information.

4.2 Setting Front-End Flags

This section describes the front-end flags that you can set for your compiler.

You can set or change the front-end flags in three ways:

- When using the GUI, you can set or change the front-end flags to affect all instances generated by the compiler by defining them in the custom global file.
- When using the GUI or when running ISH, you can change the front-end flags to affect all instances generated in the project.
- When using VMC, you can set or change the front-end flags for a particular instance by defining them in the VMC configuration file (**`filename.cfg`**).

In the **`custom.glb`** file or the VMC configuration file, you can set parameters with commands in the format:

```
parameter=value
```

In the ISH script, you can set parameters with commands in the format:

```
component <obj> set_parameter <string:parameter_name> <string:parameter_value>
```

In all cases, each parameter setting is a separate line in the file, and they can appear in any order.

See the GLB Reference Chapter in the Integrator Manual for a complete list of the front-end flags and their descriptions. Also reference the Integrator Shell chapter for additional information on the use of ISH commands.

The parameters that are supported by the current compiler are described in the compiler's custom global file. For further information please contact the Synopsys Support Team at http://solvnet.synopsys.com.

5 Using Back-End Views

This chapter describes the back-end views, which contain the files that support layout and fabrication. The compiler supports the following back-end views:

5.1 Using LEF Models

Layout Exchange Format (LEF) provides an abstract for the memory. This is the minimum information required by the Cadence place and route tools to handle the memory macro generated by the compiler. The abstract defines the size of the macro, pin names and locations, pin layers, pin capacitance, and (optionally) diode/diffusion area information. It also includes all of the physical segments generated by the Power and Pin Router (PPR), which can be associated either with power routing or signal routing. You can also define obstruction regions (regions that the router must avoid during global or detail routing) in Left macro core is marked by obstruction to avoid capacitance coupling crosstalk with critical internal signals such as bit or bitbar, se or seb.

The LEF view contains only the MACRO and SITE definition. You must provide technology definitions (layer names, layer properties, and viagens) that should be loaded into the router before reading the LEF view. LEF layer names are set up in the global file to match the layer names from the technology definition file.

The LEF view contains the power ring configurations of via structures using via layer representation, not instances. These are via structures used in the power ring.

Please contact Synopsys Support Team at http://solvnet.synopsys.com or refer to the Embed-It! software documentation for further information to change layer names, change LEF version, or to add other optional LEF information.

5.2 Using GDSII

The GDSII file contains layouts of the leaf cells in the GDSII format. It contains the mask data used to create the macro. It is also used to extract the physical layout netlist for LVS verification.

To change the GDSII layers used, you can modify the **.ltt** file in the compiler directory or reference another layer map file using the **layers_file** variable. For example:

```
set cfg(layers_file) <path>/file.ltt
```

You can place the power ring and pin geometries at the top level of the instance hierarchy, or in a separate cell one level below the top. Your choice will not alter the LEF view, but the separate ring-and-pins cell is easier to feed to a non-LEF router.

5.2.1 Naming GDSII Libraries

Synopsys' DesignWare memory GDSII library names start with a prefix of the form **Mnnnxn_**. The prefix denotes the internal compiler design project name and the library revision. It is applied to every cell in the GDSII library and ensures that there are no conflicts in cellnames when you combine instances from different compilers or different versions of a compiler into a design. The maximum length of a cell name in the compiler library is 32 characters so that they are compatible with industry-standard layout tools.

Apart from compiler-specific leaf cells, an instance also contains compiler-generated, instance-specific cells. The instance-specific cellnames start with a user-defined prefix of an instance name. Compiler-generated block names can have a maximum length of 14 characters because if an instance name is 17 characters long, the total length of any generated cell name is a maximum of 32 characters.

5.2.2 Using the Layer Translation Table File

The Layer Translation Table (LTT) file maps the Design layers to the foundry layers. Layers that are not needed for production are deleted (marked with a **D** in the LTT file).

5.3 Using SPICE Netlists

Embed-It! Integrator generates the SPICE netlist (transistor-level netlist) for the macro. You can use this SPICE netlist only for LVS verification.

The compiler SPICE netlist contains the subcircuit representations of leaf cells used for building an instance. The compiler library of subcircuits use the same prefix as the GDSII library. So, you can combine netlists when combining instances from different compilers on to one design. The SPICE subcircuits match with the GDSII leaf cells. Cells that match GDSII cell contents (for hierarchical LVS) are defined in the **<instance>_hcell.txt** output file produced for each instance.

The SPICE netlist generated for an instance uses the compiler subcircuit library as the base, and adds the subcircuit definitions for all generated blocks to it.

5.4 Reading the Bitmap (Scramble) Information

The bitmap file **<instance>.bitmap** is created during memory generation. This file contains the logical to physical scrambling information related to the memory instance being generated, taking into consideration the memory type, pin names and properties, memory port information and physical organization of the memory.

Refer to the Embed-It!® Integrator User Guide for further information reading the bit map file using Bit Browser.

6 Configuring Files

This chapter shows you how to configure the following files:

- "Configuring the Custom GLB File" on page 89 -- The custom GLB file contains parameters that influence the memory generation tool.
- "Configuring the Layer Translation Table File" on page 90 -- The Layer Transition Table (or LTT) file has GDS layer mapping details and can be used to convert a compiler from one technology to another.
- "Controlling Power and Pin Router Capabilities Through the Custom GLB File" on page 91.

6.1 Configuring the Custom GLB File

The custom GLB file (**<compiler>_custom.glb**) is located under the compiler directory in the compiler library. The following subsection explains how to set and change the custom GLB file parameters.

6.1.1 Setting Parameters

This section shows you how to set parameters in the customer global file and the COVER control file.

- Parameter names are case sensitive and must appear as entered in the custom GLB file.
- In the custom GLB file, the values that appear on the right sides of equal signs are only sample values. Instead of directly using these values, use the values that correspond to your processes and designs in your custom GLB files.
- To disable a parameter setting in the custom GLB file (and not override it with a new value), assign it the value **FALSE** or **TRUE**, where **FALSE** or **0** stands for disable and **TRUE** or **1** stands for enable. For example, the setting **bist_enable=TRUE** makes the **BIST** and **test** pins visible in the design and lets you use these features.
- To set a parameter in the custom GLB file, enter the following command in the file:

```
parameter = value
```

To set a parameter in the COVER control file, enter the following command in the file:

```
set cfg(parameter) value
```

- The parameter setting is a separate line in the file. The setting can be in any order.
- Parameter values must be specified using the same syntax as presented in the custom GLB. Parameter values can be surrounded by curly braces **{ }** or double-quotes (**" "**). Double quotes are required if a string value contains spaces, or if the string looks like a number that can be incorrectly reformatted such as "0123". Double quotes are used in the custom GLB and configuration files for parameters whose values are character strings other than **yes** or **no**.
- Comments in the custom GLB file must be enclosed within the symbols **/*** and ***/**. Comments in the COVER control file must be preceded by the symbol **#**.

The parameters that are supported by the current compiler are described in the compiler's custom global file. For further information please contact the Synopsys Support Team at http://solvnet.synopsys.com.

6.1.2 Generating Pins

The pin table is based on pin names already defined and should not require customization. If additional customization is required, contact Synopsys, Inc. for assistance.

6.2 Configuring the Layer Translation Table File

The LTT file defines the GDS layer mapping. It maps the design layer numbers to foundry layers. The design layers are listed in one column and the foundry layers in another column with a corresponding layer name for each layer.

The **layers_file** parameter defined in the custom GLB file specifies the name of the layer mapping file. Use the **layers_file** to convert from one technology to another. The filename signifies the layers mapped. For example, to represent the design-to-<foundry> layer translation table set the following parameter in the custom GLB file:

```
layers_file = "design2<foundry>.ltt"
```

While the LTT file is open for user modifications, it is imperative that either the VSIA tag layer or IP Marker Layer are not removed.

6.3 Controlling Power and Pin Router Capabilities Through the Custom GLB File

The standard (default) power ring has many flexible attributes. You can control the layer and position of each power ring strip. If the power ring exceeds the wide metal width, the appropriate slotting rules for the technology is applied.

The PPR has the ability to independently specify the metal layer used by each power ring on each side of the memory. Signal route layers can be specified, signal routing and power ring can be gridded, vias can be added to the end of signal routes, etc. It can also stack power rings, so that VSS is in metal 1 and 2 and VDD is on top of the VSS ring in metal 2 and metal 4 to reduce instance size. Overall width and height can be snapped on grid. If additional customization is required beyond the default capabilities, the PPR file must be modified which requires assistance from Synopsys, Inc.

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