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Logical Effort Summary

- Purpose: delay characterization and sizing
- Delays are relative to a unit delay τ: intrinsic min. inv. delay (unloaded)
- Model: no technology constants

Principle: $d = p + h \cdot g$ ← logical effort

- d: cell delay
- p: parasitic delay
- h: electrical effort

d: from an input to an output (different d's per gate are possible)

How to find parameters p, d, h?

p: multiples of a unit capacitance connected ~~to~~ directly to the output net of the gate, divided by that of min-size inverter

„unit capacitance" = capacitance presented to the output by an NMOS of minimum size

For $\beta = 2$, a min-size inv. has 3 unit caps at the output. Its $p = 1$.

A NAND has 6 unit sizes (~~speed~~ drive-matched to a unit inverter. $p_{NAND} = 2$

p: independent of sizing

g: Logical effort; logic-overhead in terms of input-load to realize logic function, relative to an inverter

$$g = \frac{C_{in}^{gate}(\text{min-size})}{C_{in}^{INV}(\text{min-size})}$$

C_{in}^{*}: ~~input~~ input/gate capacitance "(normalized): Capacitance of the relevant input relative to that of a minimum size NMOS (C^0)

h: Electrical effort; requires knowledge of the „context" output-load relative to the driving capability (input load)

$$h = \frac{C_{load}}{C_{in}^{gate}(\text{actual-size})} = \frac{C_{load}}{\gamma_\ell C_\ell^0} = \frac{C_{load}}{\gamma_\ell \underbrace{C_{in}^{gate(\ell)}(\text{min}) \cdot C^0}_{C_\ell^0}}$$

γ_ℓ: Upsizing factor of the gate ℓ relative to the

$C_{load} = \gamma_{e+1} C_{in}^{(gate(e+1))}(min)\, C$

$\rightarrow h_e = \dfrac{\gamma_{e+1} C_{in}^{(gate(e+1))}(min)}{\gamma_e C_{in}^{gate(e)}(min)}$ (independent of C°)

- For first gate: $\gamma_e \equiv 1$
- For last gate ($e=N$)

$\rightarrow h_e = \dfrac{C_L/C^\circ}{\gamma_e C_{in}^{gate(e)}(min)}$ $\quad e=N$

$\boxed{C_e^\circ = C_{in}^{gate(e)}(min) \cdot C^\circ}$ (C°: global; $C_{in}^{gate(e)}(min)$: per gate-type)

Sizing: Define Path-Electrical Effort(H) and Path-Logical Effort(G) (indep. of sizing)

$$G = \prod_{e=1}^{N} g_e \qquad H = \prod_{e=1}^{N} h_e = \frac{C_L}{\gamma_1 C_1^\circ}, \ \gamma_1 \equiv 1$$

(H: indep. of sizing; C_1°: first gate)

Define: Path-Intrinsic Delay (indep. of sizing)

$$P = \sum_{e=1}^{N} p_e$$

Min path delay: $D_{min} = P + N\sqrt[N]{GH}$

Effort-Delay of each stage for min delay: $\hat{f} = \sqrt[N]{GH}$

Gate sizing:

- Stage-by-stage: left-to-right ($n = 1, \dots, N$): $\gamma_n = \hat{f}\,\gamma_{n-1} \dfrac{C_{n-1}^\circ}{C_n^\circ} \cdot \dfrac{1}{g_{n-1}}$

  right-to-left ($n = N, N-1, \dots, 2$): $\gamma_n = \dfrac{1}{\hat{f}}\, g_n \dfrac{\gamma_{n+1} C_{n+1}^\circ}{C_n^\circ}$

- Immediate: $\gamma_n = \hat{f}^{n-1}\gamma_1 \dfrac{\prod_{i=1}^{n} \frac{1}{g_i}}{\hat{f}^{N-n+1}} = \dfrac{1}{\hat{f}^{N-n+1}} \prod_{i=1}^{N} g_i \dfrac{C_L}{C_n^\circ}$