



Cadence Virtuoso Simulation Tutorial

osman.kiziltug@epfl.ch

September 25, 2024

1 Objectives

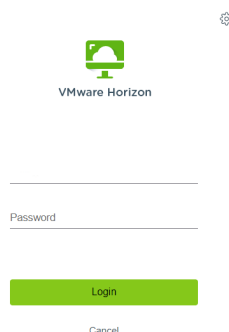
The aim of this tutorial is to familiarize you with creating test benches for any circuit you may wish to simulate. While we will skip certain non-essential steps, we'll focus on the more practical and relevant aspects for this course. For additional details, you can always refer to the **Cadence Reference Tutorials** by Alexandre Levisse, available on the Moodle. This tutorial is prepared based on those Cadence Reference Tutorials. Throughout this guide, we will introduce a few basic commands for running simple simulations.

2 Launching to Cadence Virtuoso

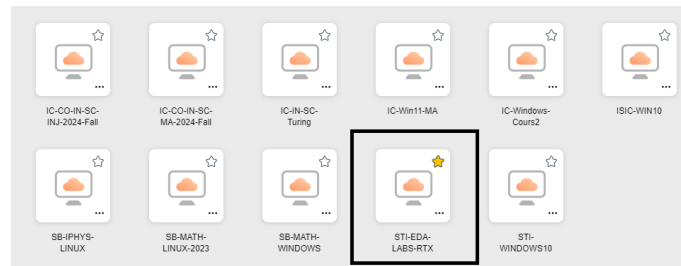
Through this section, we will try to address how to launch the Cadence environment from your own computer or from the computers available in the EPFL labs. Here, we will try to explain each step with an image. If you are not familiar with the environment, try to follow the procedure step by step to launch Cadence Virtuoso.

2.1 Connect To The VDI Workstation

If you are using your own computer, go to this link [VMware Horizon](#), and login with your gaspar credentials.

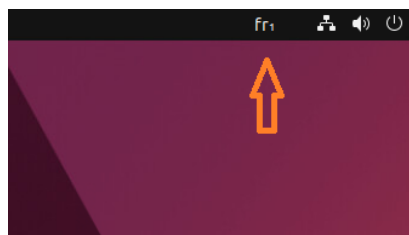


If you are outside of EPFL, you may need to use VPN (Cisco Secure Client) to connect EPFL infrastructure. Once you logged in, connect to the STI-EDA-LABS-RTX.



Now, you are in the linux (ubuntu) environment. If your keyboard is different then Swiss French keyboard, change it to your own keyboard so that you may get rid of some of the problems that you may face in the next steps. To change your keyboard settings, go to the **Settings** → **Keyboard**, and add your keyboard.

After you add your keyboard, don't forget to choose it from upper right corner, otherwise it will not work.



2.2 Connect To The EDA Servers

- Use keyboard shortcut **CTRL+ALT+T**, this will pop up a terminal.
- Type this: `ssh -X edauserN@selsrv1.epfl.ch`

Here, the N is the number that is attributed to you. You can find this number from the document which is available in Moodle named **Server credentials for Cadence simulations**. If you cannot find your name into this list, please contact us.

To balance the workload over the two different servers equally:

- If your edauser number is odd, use **selsrv1**
- If your edauser number is even, use **selsrv2**

The default password is: **24user_eda!**

2.3 Update Your Password

We advise you to update your password so that no one else can intervene with your work.

```
edauserX@selsrv1 ~]$ yppasswd
Changing NIS account information for edauserX on selsrv1.epfl.ch.
Please enter old password:
Changing NIS password for edauserX on selsrv1.epfl.ch.
Please enter new password:
Please retype new password:
The NIS password has been changed on selsrv1.epfl.ch.
```

2.4 Setting Up Your Working Environment

You will create a folder in your home directory to setup your environment.

```
> cd
> mkdir EE426
> cd EE426
```

Now, we will copy and extract an already configured working directory to our own directory.

```
> tar -xvf /softs/classroom/tutorials/2024-2025/EE429/EE429_FULLLCUSTOM.tar.gz
> cd EE429_FULLCUSTOM
```

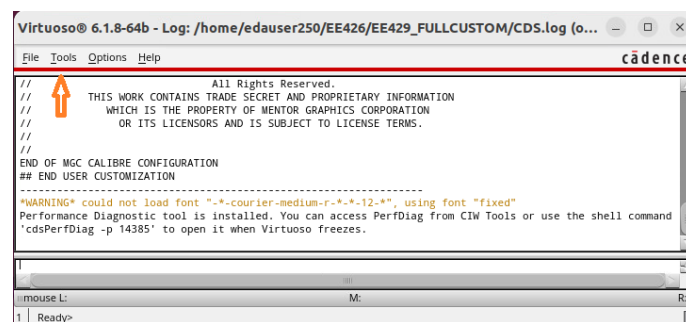
Since we use the same configuration file with EE429 course, the name of the file is EE429_FULLLCUSTOM, this should not confuse you.

```
> virtuoso &
```

The & symbol enables us to use the terminal after we launch the virtuoso.

2.5 Creating the Library

You should see the CIW

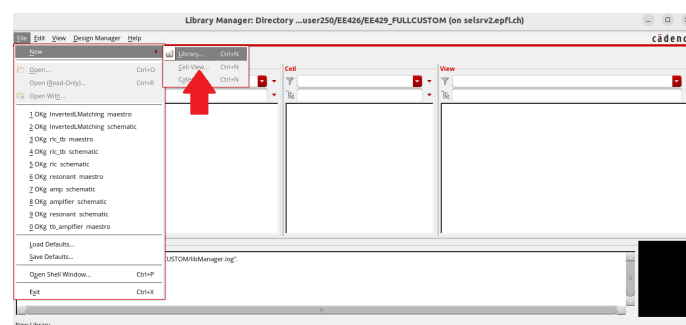


Normally, the library manager is not popped out automatically. To start it: Tools → Library Manager

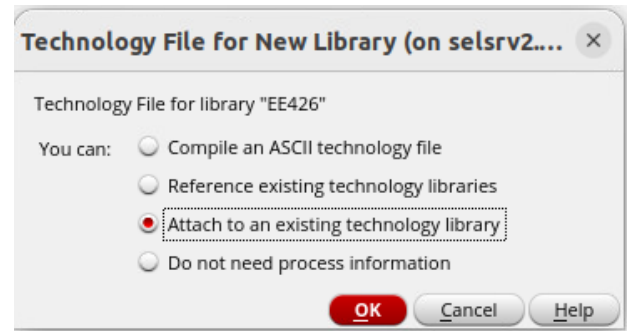
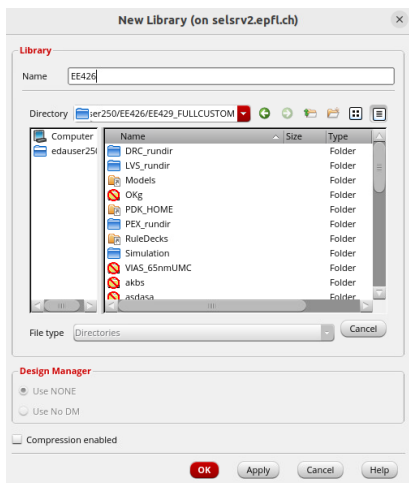
Just for the first time, you need to create your own library where you can store all of your designs and testbenches.

To create your own library:

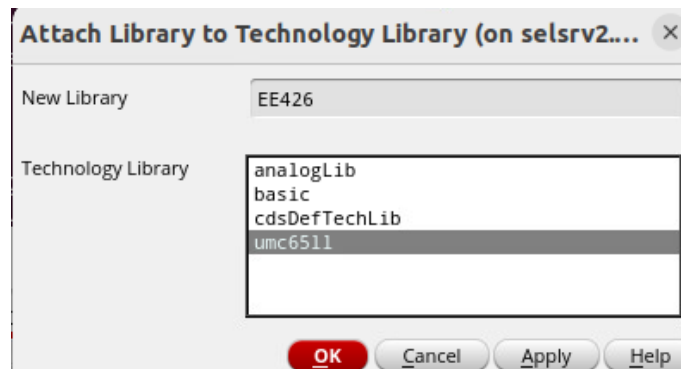
- From **Library Manager** window (not CIW window) go to File→New→Library



- Give a name to your library (EE426 in the example), you don't have to change anything else here, click OK.



- Select "Attach to an existing technology library".
- Choose **umc651l**, and click OK. Now you can see your library in the Library Tab of Library Manager.



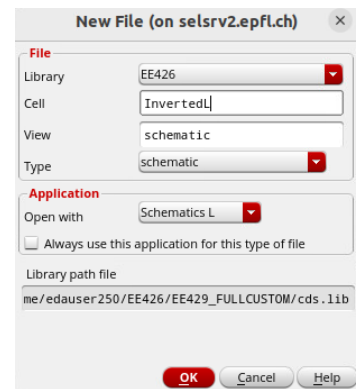
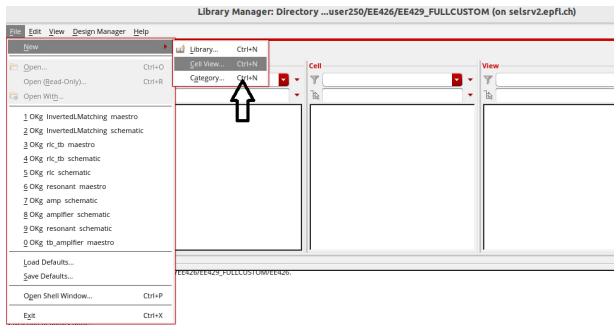
3 Generating Schematics

We can now create our first schematic to test **Inverted L Matching** technique. We will apply the example which is given in the lecture "LC resonant circuits, equivalence, impedance matching" lecture, on slide 14.

To create your first schematic, follow the procedure:

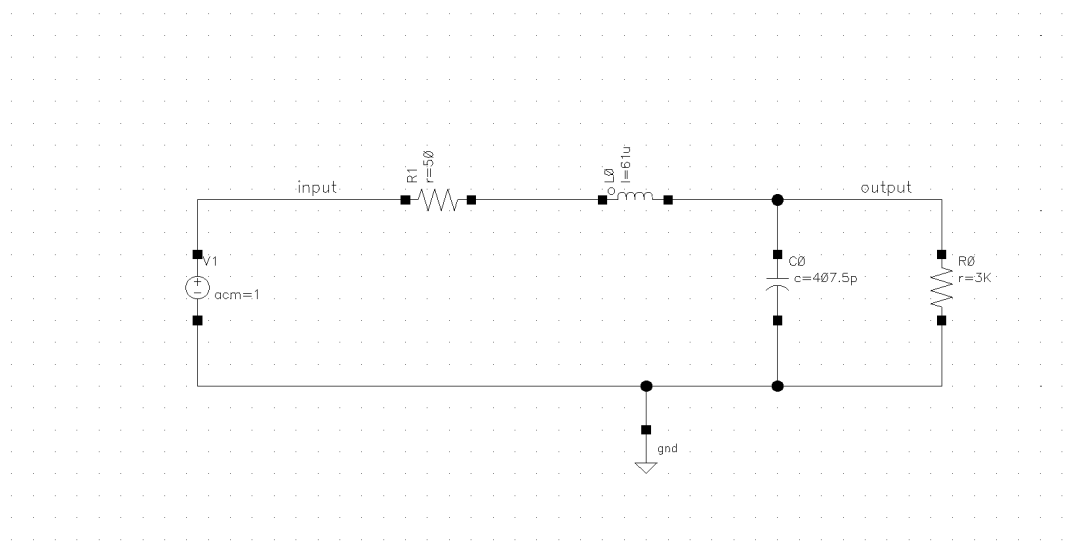
- Go to File → New → Cell View
- Give a name to your cell (**InvertedL** in the example). Make the Type → schematic

You should see a blank schematic view where you will add your instances.



Normally, what we do is to use different schematics for design and testbench. In this case, we generate a symbol for our design and insert it to the testbench as an instance. However, for the sake of simplicity, we will use the same schematic for both the design and testbench as the circuits we will use will not be too complex.

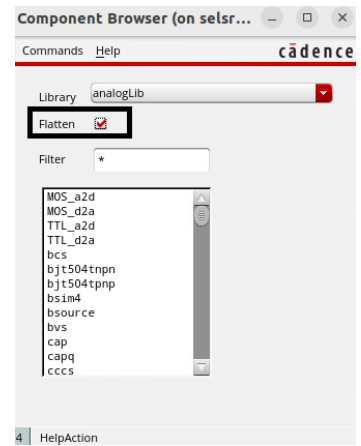
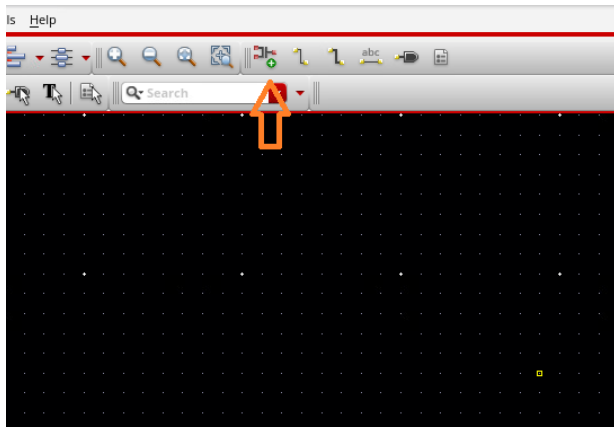
Here, you can see the final state of the schematic that you are going to get. If you are already familiar how to create schematics, just implement this schematic and pass to the simulation part.



To add instances to your design, press the button which is located at the top of the screen.

At the beginning of this course we will not need any active circuit elements, so we will mostly use analogLib, where we can find the ideal resistors, capacitors and inductor. But if you need any active element you can use umc65ll library. Here are some useful components and where you can find them:

- analogLib → res → Resistor
- analogLib → cap → Capacitor
- analogLib → ind → Inductor
- analogLib → vdc → DC Voltage Source
- analogLib → gnd → Ground
- umc65ll → N_12_LLRTV → NMOS
- umc65ll → P_12_LLRTV → PMOS



To add instances you can also use the bindkey **i**.

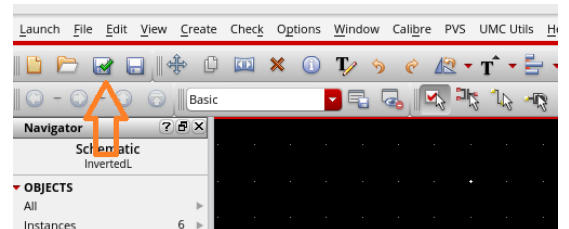
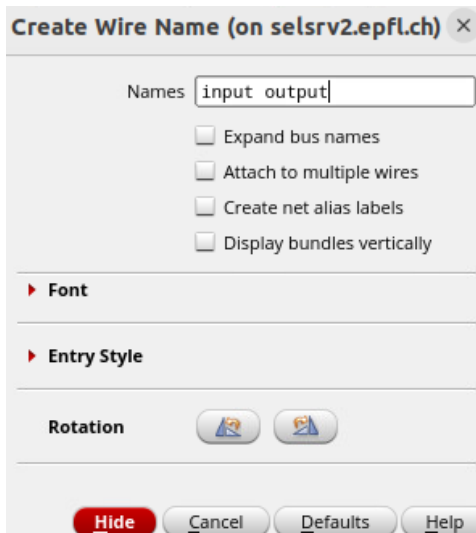
To get the given schematic, add all the required elements to your cell. Then, to edit the properties of an instance you can first choose the instance that you want add a property and use bindkey **q**. You will see properties window where you can edit various features.

For example, for the vdc in the schematic, when you press **q** you will see this window:

Here you should set AC magnitude to 1, since we are going to make an AC analysis, it will ease the computations after simulation.

For the sake of readability, you may want to add labels to some wires. To create labels you can use bindkey **l**. After that, a window will pop up and then you can give the names as given in the reference schematic.

Then, you are ready for the simulation. Before you continue don't forget to **Check and Save** your design.

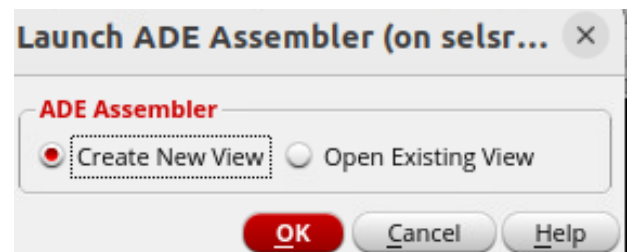
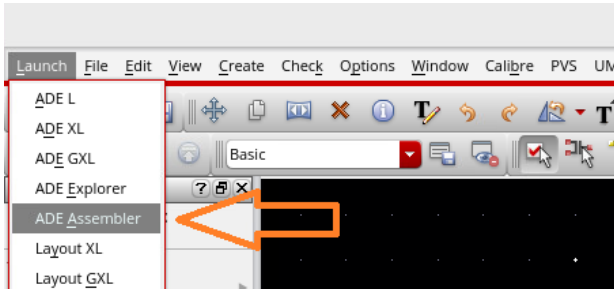


4 Go for the Simulation

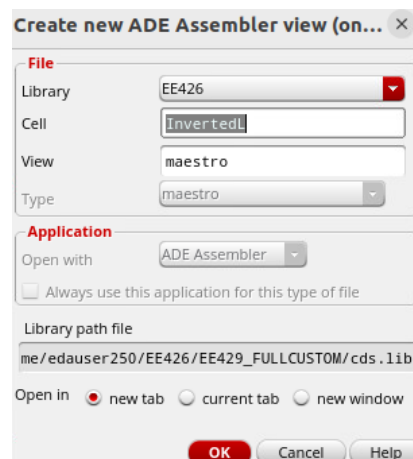
Now, we will simulate our circuit and see whether we were able to succeed impedance matching at the given frequency (1MHz) with the given load (3k Ohm) and source (50 Ohm) impedance.

There are different ways of running the simulations with different tools, but here we will use ADE Assembler. To launch to ADE Assembler;

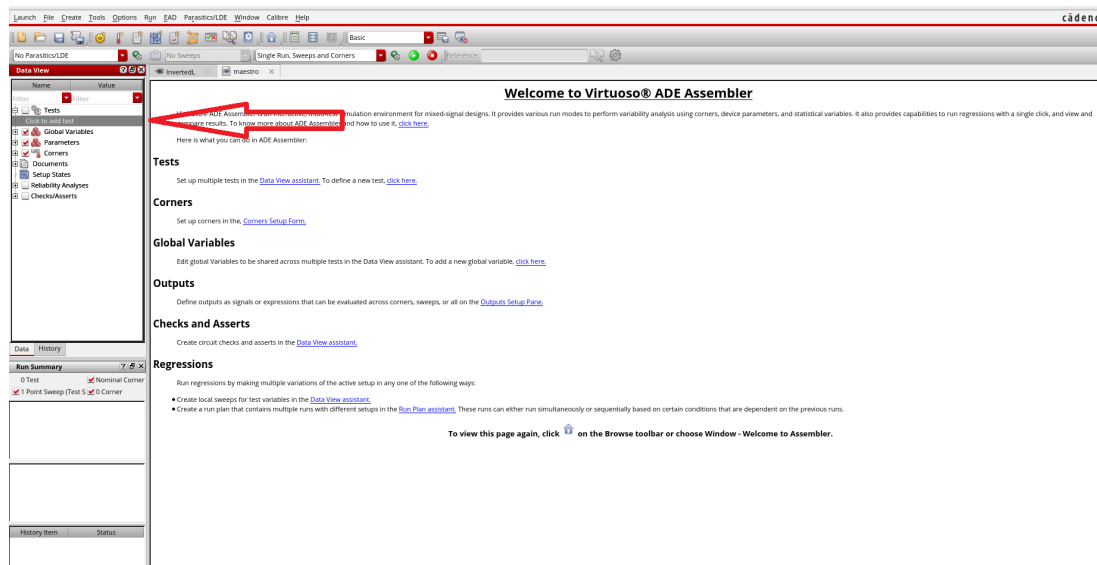
- Go with Launch → ADE Assembler
- Since this is the first time we launch ADE Assembler, you should choose Create New View.



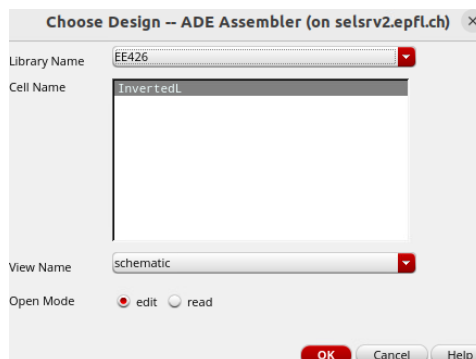
- You don't have to change anything in the next window, the view name should be **maestro** as can be seen in the figure below.



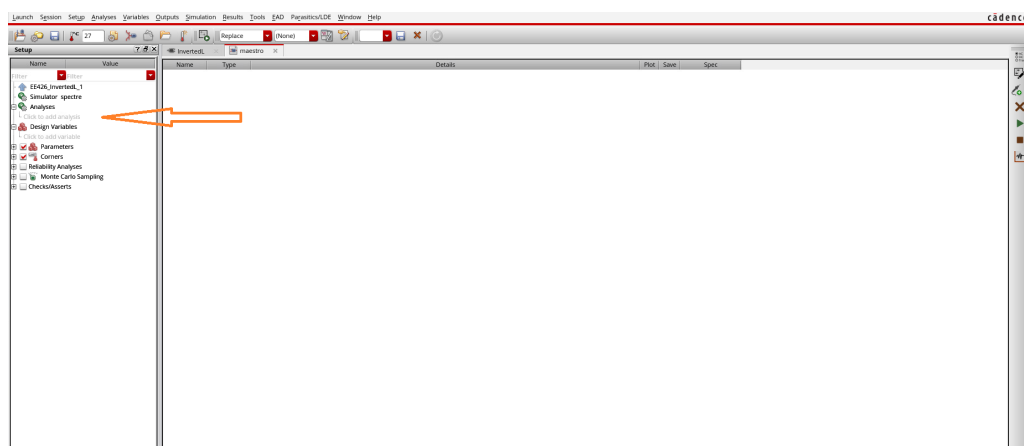
- After you press **OK**, you will see the window below. Now, we need to add tests to our simulation. For this, go to the **Tests** (shown with an arrow) and press **[+]** to expand it. Then, you will see **Click to add test** option.



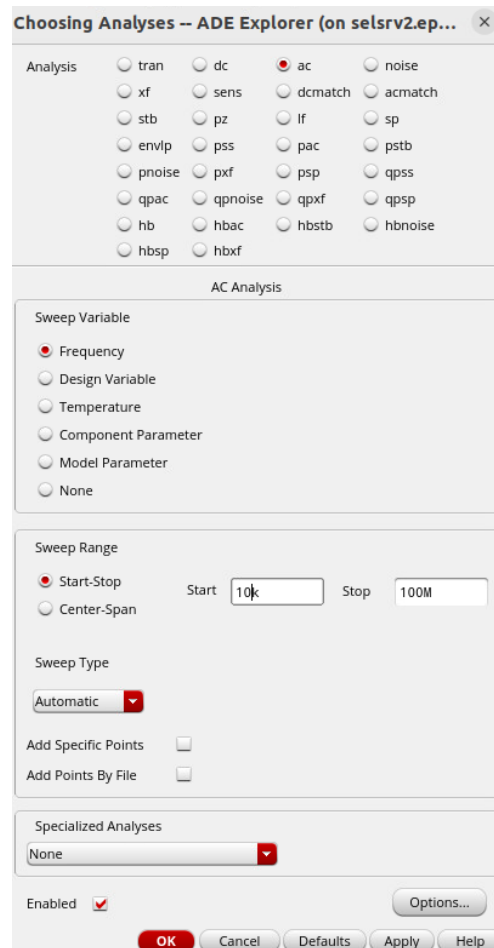
- At the next window, in general, you don't have to change anything. Choose the schematic that you want to work with. Then press **OK**.



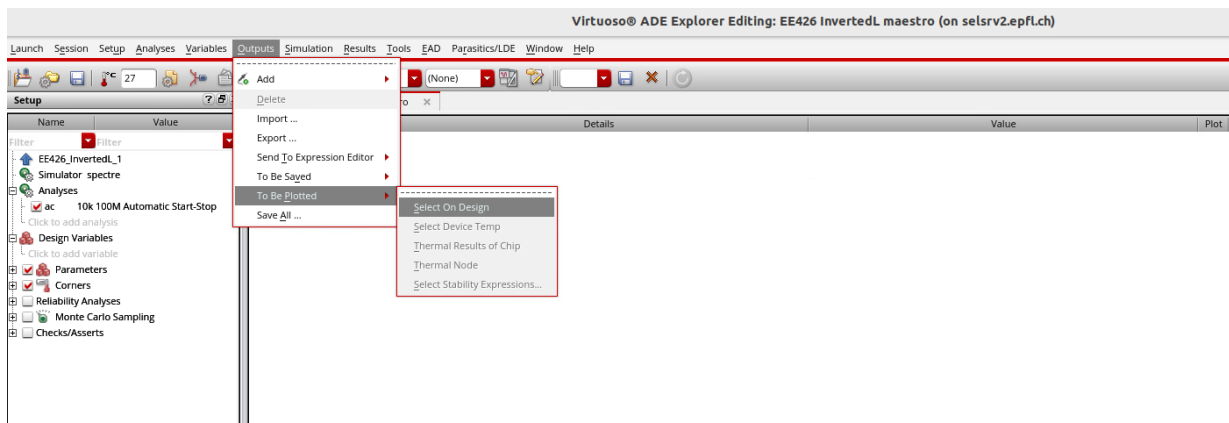
- You will face with the window below. You can choose **Click to add analysis**.



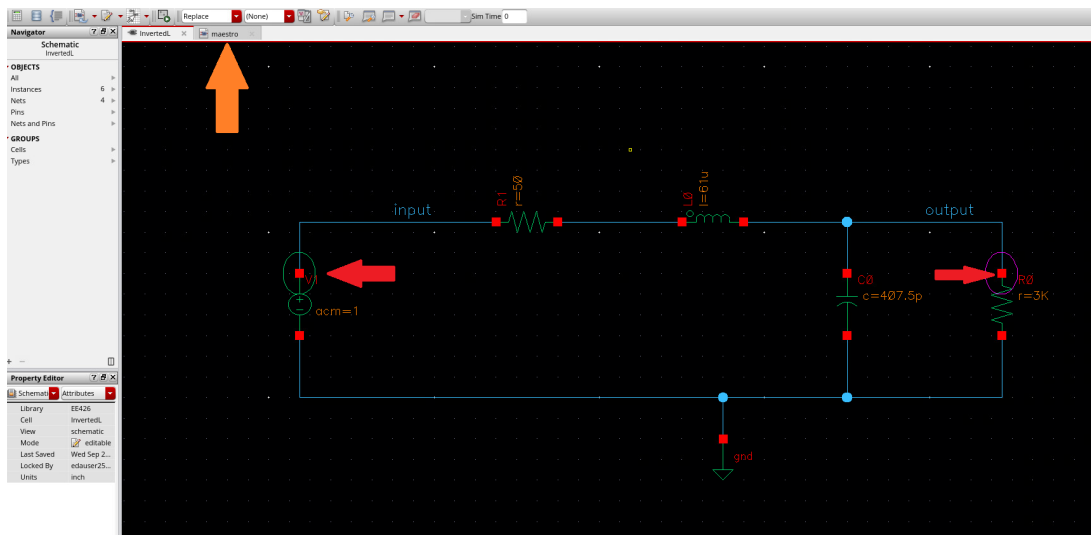
- You can make all the necessary changes to get the window below. You need to choose an analysis, and then for the **Sweep Range**, you can put 10k and 100M. This is the frequency range that we are going to analyze our circuit.



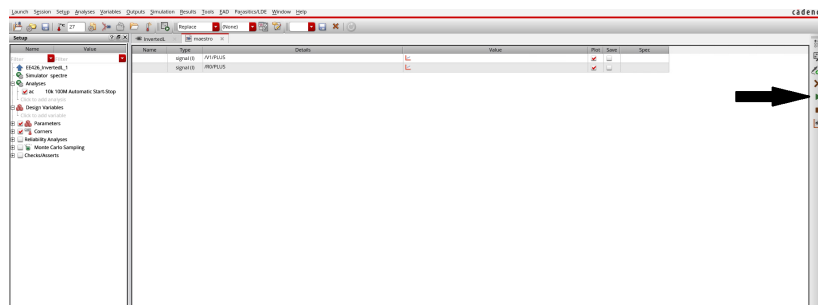
- Now, we want to observe the change in the current to see how much power we deliver to the load. For this, we will plot the currents of the voltage source and the load. At the best case we will be able to deliver half of the power to the load. To plot these currents, you should choose **Outputs → To be Plotted → Select on Design**.



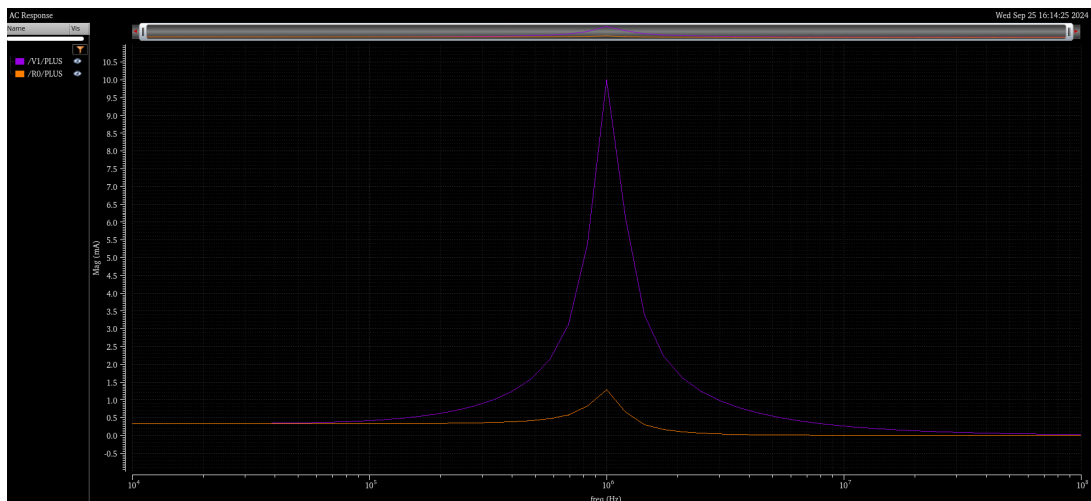
- This will direct you to the schematic. You should choose the upper terminal of **vdc** and the load of the circuit (3k Ohm in this case). After you choose both, a colorful rings will appear around them. Here, you should note that you will **NOT** choose the blue lines but the red boxes to attribute currents (not voltages). After you choose the terminal you can go back to maestro view by choosing the maestro as shown with an arrow in the figure below.



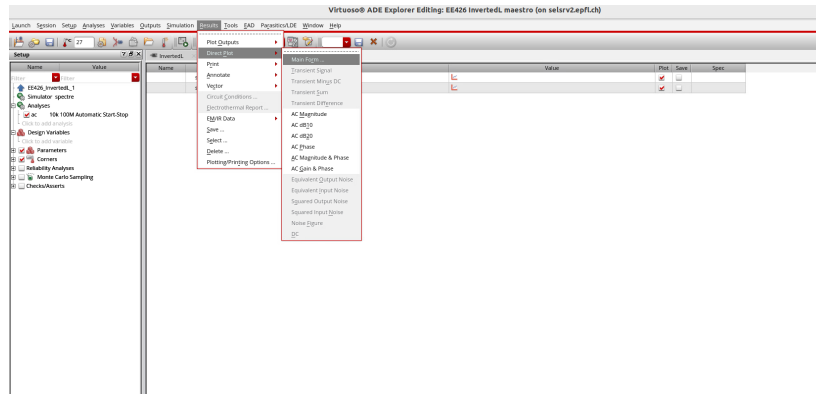
- After you get back to maestro view, you can run your simulation by clicking on the green button on the screen.



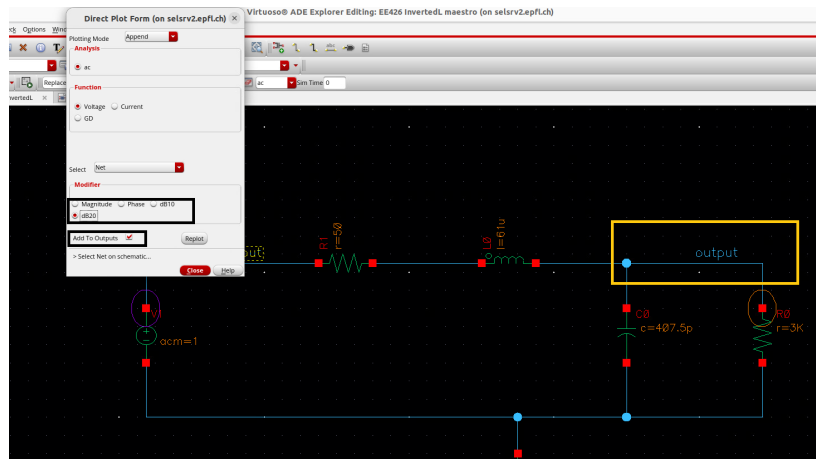
- Once the simulation finishes, you will see the output in your screen, (if you can't see, look for the other windows, it may hide sometimes). You can keep this window open, we will come back to it later.



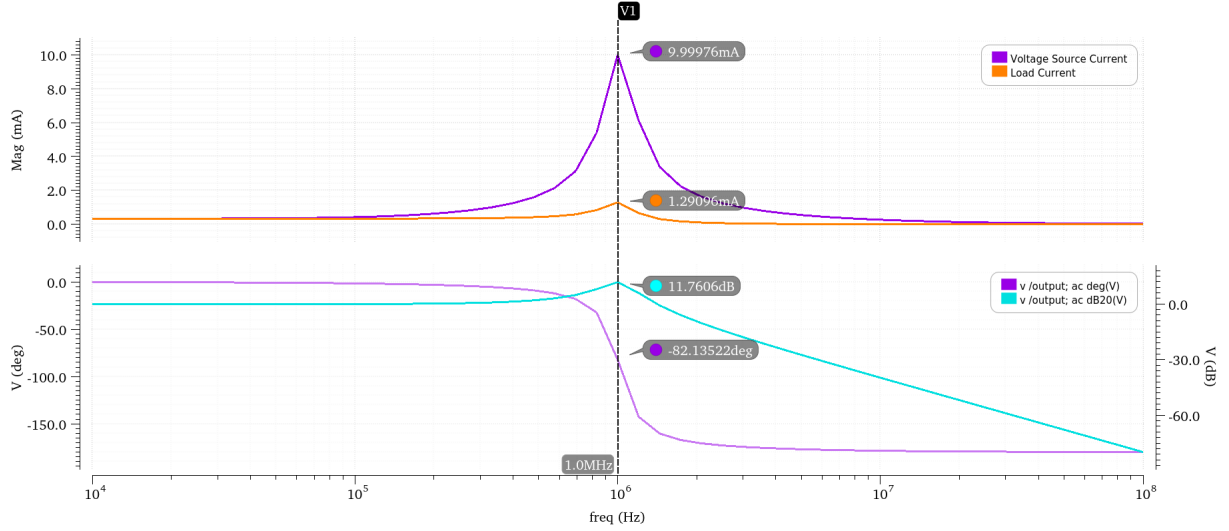
- Switch back to maestro view. Here, choose **Results** → **Direct Plot** → **Main Form**.



- This will direct you to the screen below. Choose **dB20**, and tick **Add To Outputs**. After that, just choose the output node (blue line this time). This will add the output voltage magnitude in dB to the graphs that we saw before.



- Switch back to the maestro view. Apply the same procedure as before, this time choose **Phase** instead of **dB20**.
- Now, we are done with the simulation. We can analyze the results. You can switch to the graphs. You should see something similar to the image below. (You can add a vertical line to see the values by using the bindkey **v**).



Now we can analyze the results. The current at the output is $I_{load} = 1.29096 \text{ mA}$, and at the voltage source side, it is $I_{source} = 9.99976 \text{ mA}$. Since we connected ideal voltage source at the input and put the AC amplitude as 1V, we have 1V at the input of the circuit, so $V_{source} = 1 \text{ V}$. However at the output we see 11.7606dB, $V_{load} = 11.7606 \text{ dB} = 3.87284 \text{ V}$.

The power dissipated can be given as:

$$P = VI$$

The power dissipated by the voltage source is:

$$P = 1 \text{ V} \times 9.99976 \text{ mA} \approx 10 \text{ mW}$$

The power dissipated at the output is:

$$P = 3.87284 \text{ V} \times 1.29096 \text{ mA} \approx 5 \text{ mW}$$

As demonstrated by the calculations, half of the power is successfully dissipated in the load as expected. Therefore, impedance matching is achieved with the given inductor and capacitor values at a frequency of 1 MHz.