Fundamentals of Analog & Mixed Signal VLSI Design
Exercise 8 (13.11.2024)

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Problem 1 Design of the Symmetrical OTA

Current mirrors current gains defined as:
$A_1=\beta_{2c}/\beta_{2a}$
$A_2=\beta_{3b}/\beta_{3a}$
$A_3=\beta_{2d}/\beta_{2b}$
with
$A_3=A_1 \cdot A_2$

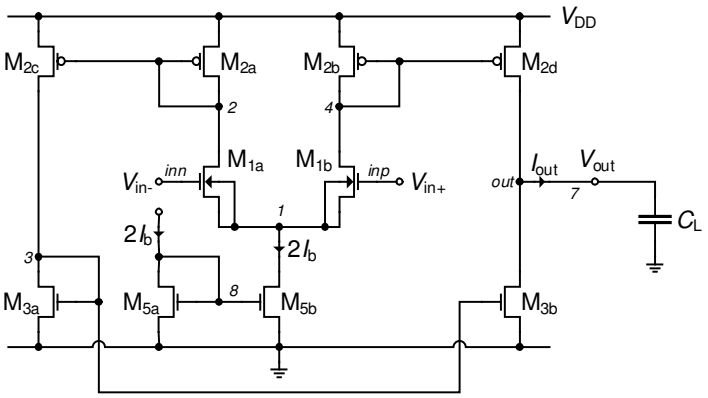

Figure 1: Schematic of the symmetrical OTA.

Design the symmetrical OTA shown in Fig. 1 for the following specifications:

$$A_{dc} \geq 100\,dB \quad GBW \geq 1\,MHz \quad V_{os} \leq 10\,mV$$

for a load capacitance $C_L = 1\,pF$ and for the process parameters corresponding to a 180nm CMOS process given in Table 1. In this design we assume that $A_1 = A_2 = A_3 = 1$. Try to minimize the power consumption and the input-referred noise.

Problem 2 Design of the Miller OTA

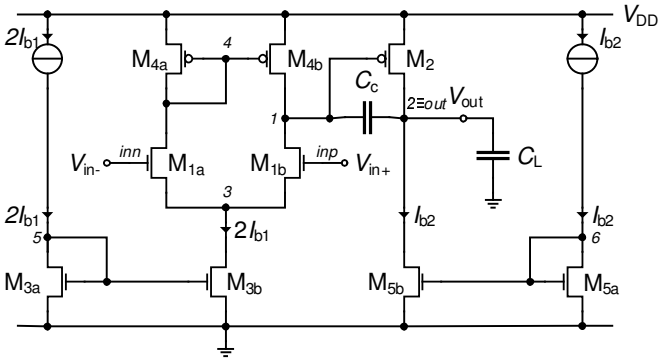

Figure 2: Schematic of the Miller OTA.

Design the Miller OTA shown in Fig. 2 for the following specifications:

$$A_{dc} \geq 100\,dB \quad GBW \geq 1\,MHz \quad V_{os} \leq 10\,mV$$

for a load capacitance $C_L = 1\,pF$ and for the process parameters corresponding to a 180nm CMOS process given in Table 1. Try to minimize the power consumption and the input-referred noise. Compare your design to the design of the symmetrical OTA.

Process Parameters			
Parameter	Value		Unit
V_{DD}	1.8		V
C_{ox}	8.443		$\frac{fF}{\mu m^2}$
W_{min}	200		nm
L_{min}	180		nm
Device Parameters			
Parameter	nMOS	pMOS	Unit
sEKV Parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	455	445	mV
L_{sat}	26	36	nm
λ	20	20	$\frac{V}{\mu m}$
Extrinsic Capacitance Parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker Noise Parameters			
ρ	5.794×10^{-2}	4.828×10^{-1}	$\frac{V \cdot m^2}{A \cdot s}$
Matching Parameters			
$A_{V_{T0}}$	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$

Table 1: Parameters for a 180 nm bulk CMOS process.