

Fundamentals of Analog & Mixed Signal VLSI Design

Exercise 6 (30.10.2024)

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Problem 1 Design of the Simple OTA

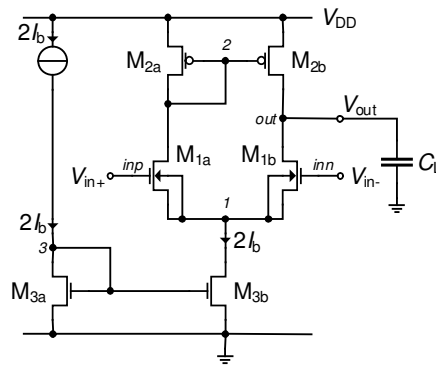


Figure 1: Schematic of the simple OTA.

Design the simple OTA shown in Fig. 1 for the following specifications:

$$A_{dc} \geq 60 \text{ dB} \quad GBW \geq 1 \text{ MHz} \quad V_{os} \leq 10 \text{ mV}$$

for a load capacitance $C_L = 1 \text{ pF}$ and for the process parameters corresponding to a 180nm CMOS process given in the next slide

Process Parameters			
Parameter	Value		Unit
V_{DD}	1.8		V
C_{ox}	8.443		$\frac{fF}{\mu m^2}$
W_{min}	200		nm
L_{min}	180		nm
Device Parameters			
Parameter	nMOS	pMOS	Unit
<i>sEKV Parameters</i>			
n	1.27	1.31	-
$I_{spec\Box}$	715	173	nA
V_{T0}	455	445	mV
L_{sat}	26	36	nm
λ	20	20	$\frac{V}{\mu m}$
<i>Extrinsic Capacitance Parameters</i>			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
<i>Flicker Noise Parameters</i>			
ρ	5.794×10^{-2}	4.828×10^{-1}	$\frac{V \cdot m^2}{A \cdot s}$
<i>Matching Parameters</i>			
$A_{V_{T0}}$	5	5	$mV \cdot \mu m$
A_{β}	1	1	$\% \cdot \mu m$

Table 1: Parameters for a 180 nm bulk CMOS process.